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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

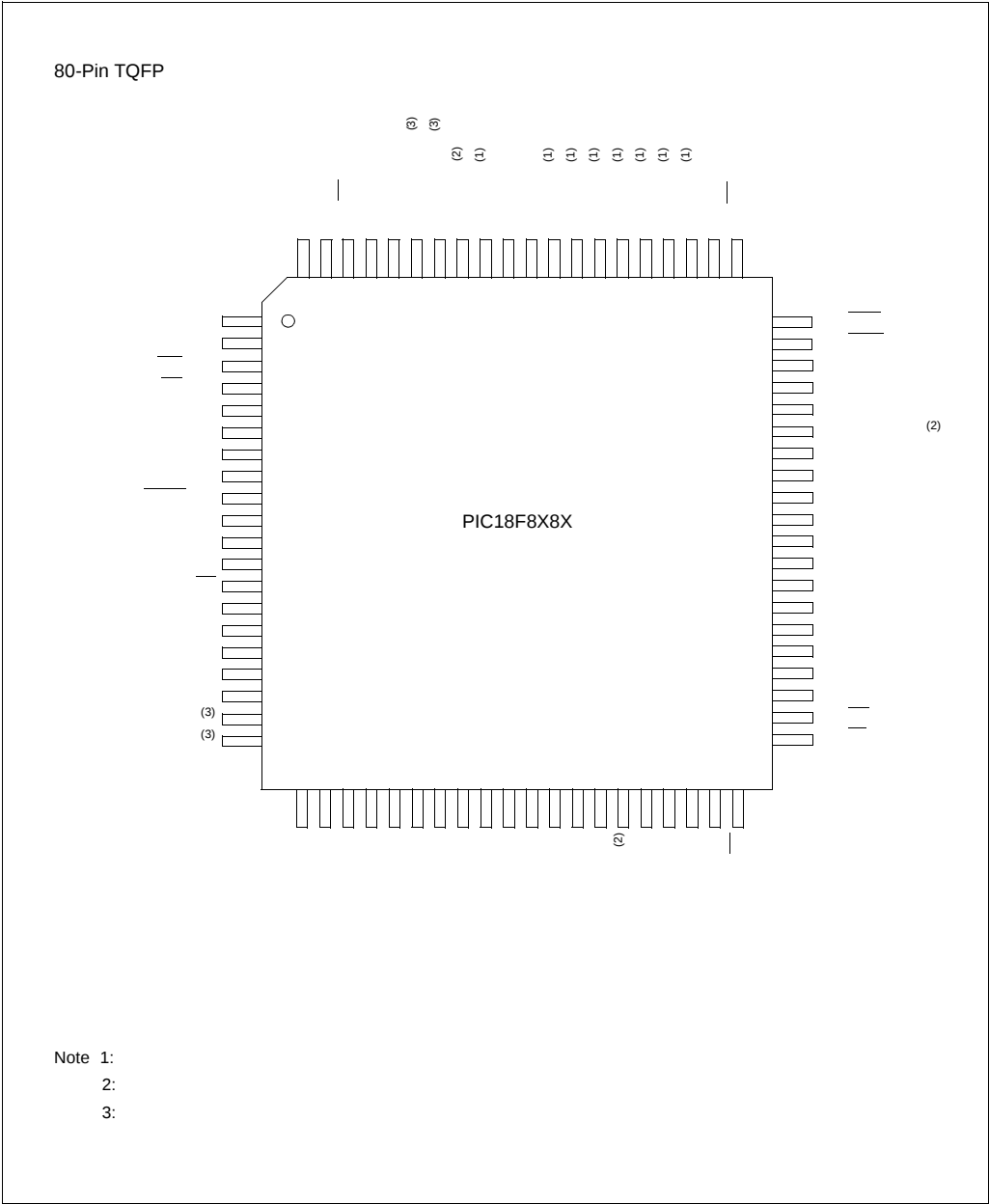
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |                                                                                                                                                                 |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Active                                                                                                                                                          |
| Core Processor             | PIC                                                                                                                                                             |
| Core Size                  | 8-Bit                                                                                                                                                           |
| Speed                      | 40MHz                                                                                                                                                           |
| Connectivity               | CANbus, I <sup>2</sup> C, SPI, UART/USART                                                                                                                       |
| Peripherals                | Brown-out Detect/Reset, LVD, POR, PWM, WDT                                                                                                                      |
| Number of I/O              | 52                                                                                                                                                              |
| Program Memory Size        | 64KB (32K x 16)                                                                                                                                                 |
| Program Memory Type        | FLASH                                                                                                                                                           |
| EEPROM Size                | 1K x 8                                                                                                                                                          |
| RAM Size                   | 3.25K x 8                                                                                                                                                       |
| Voltage - Supply (Vcc/Vdd) | 4.2V ~ 5.5V                                                                                                                                                     |
| Data Converters            | A/D 16x10b                                                                                                                                                      |
| Oscillator Type            | External                                                                                                                                                        |
| Operating Temperature      | -40°C ~ 85°C (TA)                                                                                                                                               |
| Mounting Type              | Surface Mount                                                                                                                                                   |
| Package / Case             | 68-LCC (J-Lead)                                                                                                                                                 |
| Supplier Device Package    | 68-PLCC (24.23x24.23)                                                                                                                                           |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/microchip-technology/pic18f6680-i-l">https://www.e-xfl.com/product-detail/microchip-technology/pic18f6680-i-l</a> |

# PIC18F6585/8585/6680/8680

## Pin Diagrams (Continued)



# PIC18F6585/8585/6680/8680

TABLE 3-3: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

| Register | Applicable Devices |  | Power-on Reset,<br>Brown-out Reset | MCLR Resets<br>WDT Reset<br>RESET Instruction<br>Stack Resets | Wake-up via WDT<br>or Interrupt |
|----------|--------------------|--|------------------------------------|---------------------------------------------------------------|---------------------------------|
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | xxxx x-xx                          | uuuu u-uu                                                     | uuuu u-uu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | 000- 0000                          | 000- 0000                                                     | uuu- uuuu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | -xxx xxxx                          | -uuu uuuu                                                     | -uuu uuuu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | xxxx x-xx                          | uuuu u-uu                                                     | uuuu u-uu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | 000- 0000                          | 000- 0000                                                     | uuu- uuuu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | -x- - xxxx                         | -u- - uuuu                                                    | -u- - uuuu                      |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | uuuu uuuu                       |
|          |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | -uuu uuuu                       |
|          |                    |  | xxx- x-xx                          | uuu- u-uu                                                     | uuu- u-uu                       |

Legend: u x 0 q

Note 1:

2:

3:

4:

5:

0

6:

0

7:

0

---

| Register | Applicable Devices |  | Power-on Reset,<br>Brown-out Reset | MCLR Resets<br>WDT Reset<br>RESET Instruction<br>Stack Resets | Wake-up via WDT<br>or Interrupt |
|----------|--------------------|--|------------------------------------|---------------------------------------------------------------|---------------------------------|
| (7)      |                    |  | xxx- x-xx                          | uuu- u-uu                                                     | -uuu uuuu                       |
| (7)      |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | -uuu uuuu                       |
| (7)      |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | -uuu uuuu                       |
| (7)      |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | -uuu uuuu                       |
| (7)      |                    |  | xxx- x-xx                          | uuu- u-uu                                                     | -uuu uuuu                       |
| (7)      |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | -uuu uuuu                       |
| (7)      |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | -uuu uuuu                       |
| (7)      |                    |  | xxx- x-xx                          | uuu- u-uu                                                     | -uuu uuuu                       |
| (7)      |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | -uuu uuuu                       |
| (7)      |                    |  | xxx- x-xx                          | uuu- u-uu                                                     | -uuu uuuu                       |
| (7)      |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | -uuu uuuu                       |
| (7)      |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | -uuu uuuu                       |
| (7)      |                    |  | xxx- x-xx                          | uuu- u-uu                                                     | -uuu uuuu                       |
| (7)      |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | -uuu uuuu                       |
| (7)      |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | -uuu uuuu                       |
| (7)      |                    |  | xxx- x-xx                          | uuu- u-uu                                                     | -uuu uuuu                       |
| (7)      |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | -uuu uuuu                       |
| (7)      |                    |  | xxx- x-xx                          | uuu- u-uu                                                     | -uuu uuuu                       |
| (7)      |                    |  | xxxx xxxx                          | uuuu uuuu                                                     | -uuu uuuu                       |

Legend: u x 0 q

Note 1:

4.12 Indirect Addressing, INDF and FSR Registers

0

NOP

0

EXAMPLE 4-4: HOW TO CLEAR RAM (BANK 1) USING INDIRECT ADDRESSING

|          |       |            |                  |
|----------|-------|------------|------------------|
|          | LFSR  | FSR0, 100h | ;                |
| NEXT     | CLRF  | POSTINC0   | ; Clear INDF     |
|          |       |            | ; register and   |
|          |       |            | ; inc pointer    |
|          | BTFSS | FSR0H, 1   | ; All done with  |
|          |       |            | ; Bank1?         |
|          | BRA   | NEXT       | ; NO, clear next |
| CONTINUE |       |            | ; YES, continue  |

0

NOP

# PIC18F6585/8585/6680/8680

REGISTER 6-1: MEMCON REGISTER

|     |  |  |  |  |  |  |  |
|-----|--|--|--|--|--|--|--|
| (1) |  |  |  |  |  |  |  |
|-----|--|--|--|--|--|--|--|

EBDIS (1)  
1  
0

Note 1: TBLRD/TBLWT

Unimplemented 0  
WAIT<1:0>  
11  
10  
01  
00

Unimplemented 0  
WM<1:0> TBLWT  
1x  
01  
00

Legend:

Note:



# PIC18F6585/8585/6680/8680

FIGURE 10-20: RG4/P1D PIN BLOCK DIAGRAM

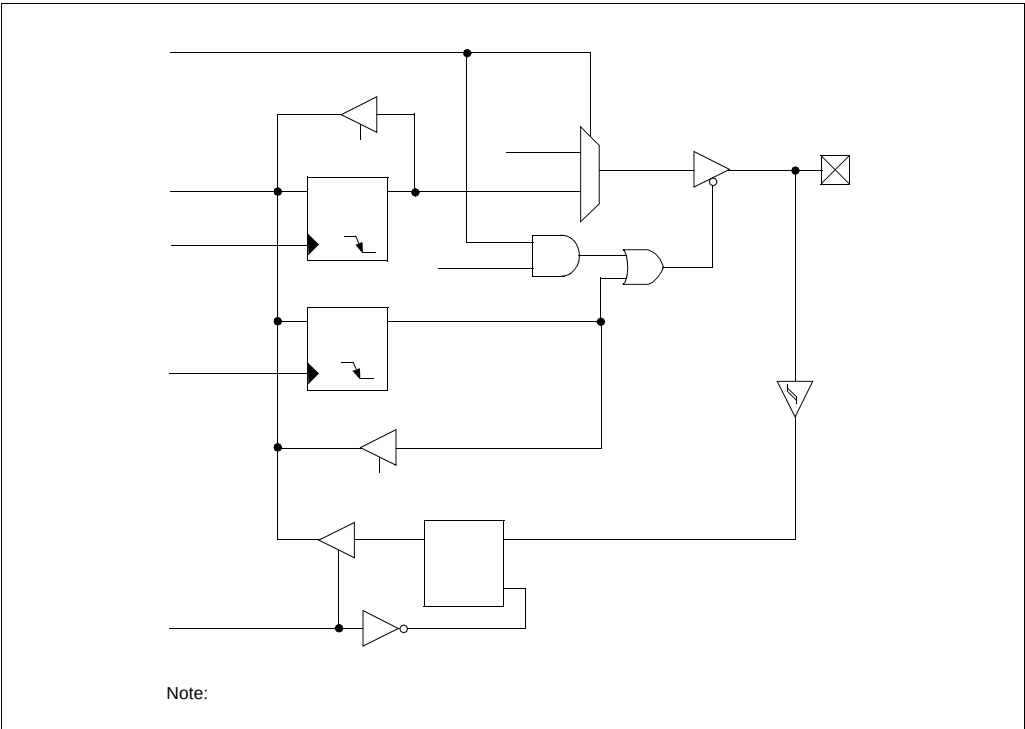
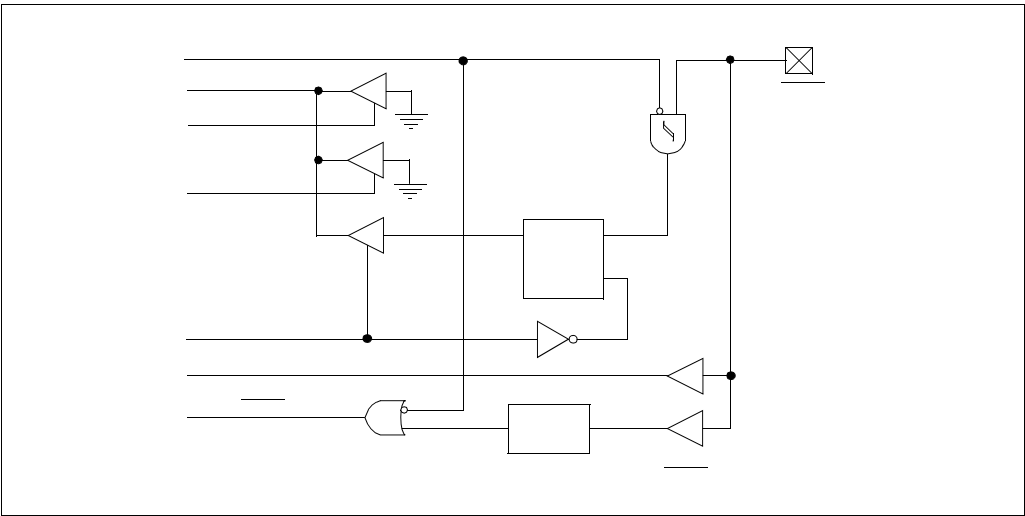


FIGURE 10-21: RG5/MCLR/VPP PIN BLOCK DIAGRAM



# PIC18F6585/8585/6680/8680

FIGURE 10-30: PARALLEL SLAVE PORT READ WAVEFORMS

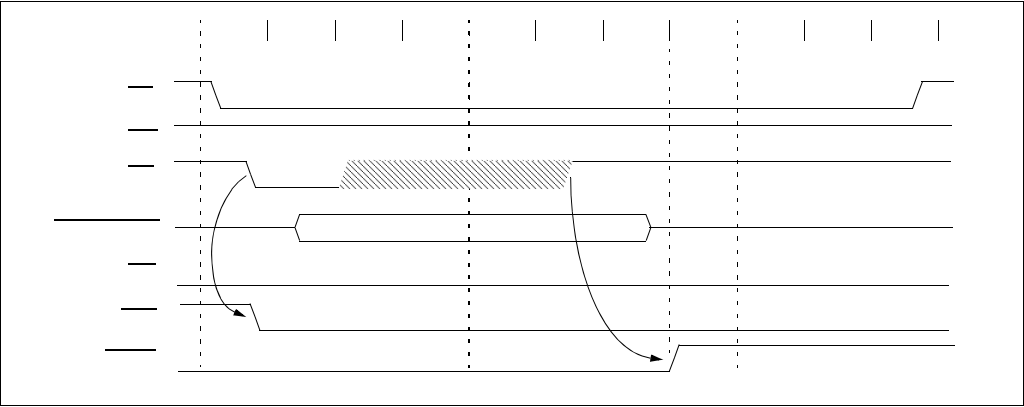


TABLE 10-19: REGISTERS ASSOCIATED WITH PARALLEL SLAVE PORT

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|------|-------|-------|-------|-------|-------|-------|-------|-------|-------------------|---------------------------|
|      |       |       |       |       |       |       |       |       | xxxx xxxx         | uuuu uuuu                 |
|      |       |       |       |       |       |       |       |       | xxxx xxxx         | uuuu uuuu                 |
|      |       |       |       |       |       |       |       |       | 1111 1111         | 1111 1111                 |
|      |       |       |       |       |       | (1)   | (1)   | (1)   | xxxx xxxx         | uuuu uuuu                 |
|      |       |       |       |       |       |       |       |       | xxxx xxxx         | uuuu uuuu                 |
|      |       |       |       |       |       |       |       |       | 1111 1111         | 1111 1111                 |
|      |       |       |       |       |       |       |       |       | 0000 ----         | 0000 ----                 |
|      |       |       |       |       |       |       |       |       | 0000 0000         | 0000 0000                 |
|      | (1)   |       |       |       |       |       |       |       | 0000 0000         | 0000 0000                 |
|      | (1)   |       |       |       |       |       |       |       | 0000 0000         | 0000 0000                 |
|      | (1)   |       |       |       |       |       |       |       | 1111 1111         | 1111 1111                 |

Legend: x      u      0

Note 1:



# PIC18F6585/8585/6680/8680

TABLE 19-2: SUMMARY OF A/D REGISTERS

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|------|-------|-------|-------|-------|-------|-------|-------|-------|-------------------|---------------------------|
|      |       |       |       |       |       |       |       |       | 0000 0000         | 0000 0000                 |
|      |       |       |       |       |       |       |       |       | 0000 0000         | 0000 0000                 |
|      |       |       |       |       |       |       |       |       | 0000 0000         | 0000 0000                 |
|      |       |       |       |       |       |       |       |       | 1111 1111         | 1111 1111                 |
|      |       |       |       |       |       |       |       |       | -0-0 0000         | -0-0 0000                 |
|      |       |       |       |       |       |       |       |       | -0-0 0000         | -0-0 0000                 |
|      |       |       |       |       |       |       |       |       | -1-1 1111         | -1-1 1111                 |
|      |       |       |       |       |       |       |       |       | xxxx xxxx         | uuuu uuuu                 |
|      |       |       |       |       |       |       |       |       | xxxx xxxx         | uuuu uuuu                 |
|      |       |       |       |       |       |       |       |       | --00 0000         | --00 0000                 |
|      |       |       |       |       |       |       |       |       | --00 0000         | --00 0000                 |
|      |       |       |       |       |       |       |       |       | 0--- -000         | 0--- -000                 |
|      |       |       |       |       |       |       |       |       | --xx xxxx         | --uu uuuu                 |
|      |       |       |       |       |       |       |       |       | --11 1111         | --11 1111                 |
|      |       |       |       |       |       |       |       |       | xxxx xxxx         | uuuu uuuu                 |
|      |       |       |       |       |       |       |       |       | xxxx xxxx         | uuuu uuuu                 |
|      |       |       |       |       |       |       |       |       | 1111 1111         | 1111 1111                 |
| (1)  |       |       |       |       |       |       |       |       | xxxx xxxx         | uuuu uuuu                 |
| (1)  |       |       |       |       |       |       |       |       | xxxx xxxx         | uuuu uuuu                 |
| (1)  |       |       |       |       |       |       |       |       | 1111 1111         | 1111 1111                 |

Legend: x u - 0

Note 1:









# PIC18F6585/8585/6680/8680

## COMF Complement f

Syntax: [label] COMF f[,d[,a]]

Operands:  $0 \leq f \leq 255$   
 $d \in [0,1]$   
 $a \in [0,1]$

Operation:  $(\bar{f}) \rightarrow \text{dest}$

Status Affected: N, Z

Encoding: 

|      |      |      |      |
|------|------|------|------|
| 0001 | 11da | ffff | ffff |
|------|------|------|------|

Description: The contents of register 'f' are complemented. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f' (default). If 'a' is '0', the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1     | Q2                | Q3           | Q4                   |
|--------|-------------------|--------------|----------------------|
| Decode | Read register 'f' | Process Data | Write to destination |

**Example:** COMF REG, 0, 0

Before Instruction

REG = 0x13

After Instruction

REG = 0x13

W = 0xEC

## CPFSEQ Compare f with W, skip if f = W

Syntax: [label] CPFSEQ f[,a]

Operands:  $0 \leq f \leq 255$   
 $a \in [0,1]$

Operation:  $(f) - (W)$ ,  
skip if  $(f) = (W)$   
(unsigned comparison)

Status Affected: None

Encoding: 

|      |      |      |      |
|------|------|------|------|
| 0110 | 001a | ffff | ffff |
|------|------|------|------|

Description: Compares the contents of data memory location 'f' to the contents of W by performing an unsigned subtraction. If 'f' = W, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is '0', the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).

Words: 1

Cycles: 1(2)

**Note:** 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

| Q1     | Q2                | Q3           | Q4           |
|--------|-------------------|--------------|--------------|
| Decode | Read register 'f' | Process Data | No operation |

If skip:

| Q1           | Q2           | Q3           | Q4           |
|--------------|--------------|--------------|--------------|
| No operation | No operation | No operation | No operation |

If skip and followed by 2-word instruction:

| Q1           | Q2           | Q3           | Q4           |
|--------------|--------------|--------------|--------------|
| No operation | No operation | No operation | No operation |
| No operation | No operation | No operation | No operation |

**Example:** HERE CPFSEQ REG, 0  
NEQUAL :  
EQUAL :

Before Instruction

PC Address = HERE

W = ?

REG = ?

After Instruction

If REG = W;

PC = Address (EQUAL)

If REG  $\neq$  W;

PC = Address (NEQUAL)

# PIC18F6585/8585/6680/8680

## MOVFF Move f to f

Syntax: [ label ] MOVFF  $f_s, f_d$

Operands:  $0 \leq f_s \leq 4095$   
 $0 \leq f_d \leq 4095$

Operation:  $(f_s) \rightarrow f_d$

Status Affected: None

Encoding:

1st word (source)

2nd word (destin.)

|      |      |      |            |
|------|------|------|------------|
| 1100 | ffff | ffff | ffff $f_s$ |
| 1111 | ffff | ffff | ffff $f_d$ |

Description: The contents of source register ' $f_s$ ' are moved to destination register ' $f_d$ '. Location of source ' $f_s$ ' can be anywhere in the 4096-byte data space (000h to FFFh) and location of destination ' $f_d$ ' can also be anywhere from 000h to FFFh. Either source or destination can be W (a useful special situation). MOVFF is particularly useful for transferring a data memory location to a peripheral register (such as the transmit buffer or an I/O port). The MOVFF instruction cannot use the PCL, TOSU, TOSH or TOSL as the destination register

Words: 2

Cycles: 2 (3)

Q Cycle Activity:

| Q1     | Q2                            | Q3           | Q4                        |
|--------|-------------------------------|--------------|---------------------------|
| Decode | Read register 'f' (src)       | Process Data | No operation              |
| Decode | No operation<br>No dummy read | No operation | Write register 'f' (dest) |

**Example:** MOVFF REG1, REG2

Before Instruction

REG1 = 0x33

REG2 = 0x11

After Instruction

REG1 = 0x33,

REG2 = 0x33

## MOVLB Move literal to low nibble in BSR

Syntax: [ label ] MOVLB k

Operands:  $0 \leq k \leq 255$

Operation:  $k \rightarrow \text{BSR}$

Status Affected: None

Encoding:

|      |      |      |      |
|------|------|------|------|
| 0000 | 0001 | kkkk | kkkk |
|------|------|------|------|

Description: The 8-bit literal 'k' is loaded into the Bank Select Register (BSR).

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1     | Q2               | Q3           | Q4                       |
|--------|------------------|--------------|--------------------------|
| Decode | Read literal 'k' | Process Data | Write literal 'k' to BSR |

**Example:** MOVLB 5

Before Instruction

BSR register = 0x02

After Instruction

BSR register = 0x05

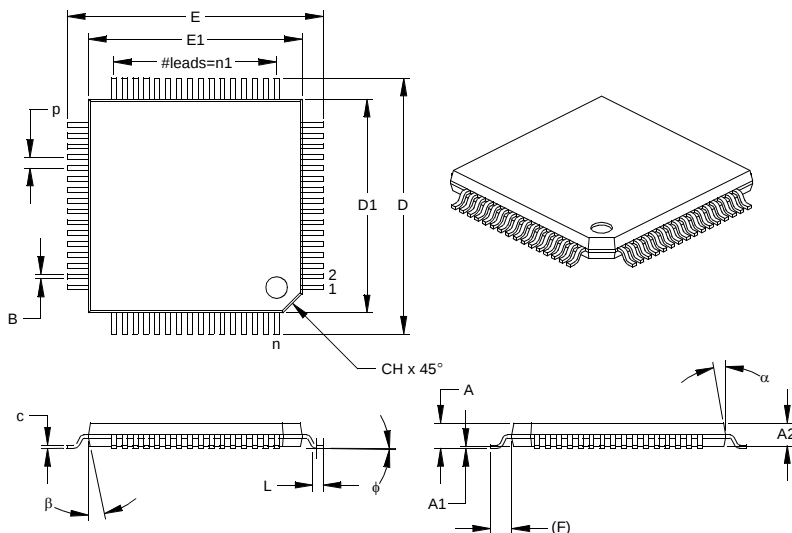
# PIC18F6585/8585/6680/8680

## 29.2 Package Details

The following sections give the technical details of the packages.

### 64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 1.0/0.10 mm Lead Form (TQFP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units                    |     | INCHES |      |      | MILLIMETERS* |       |       |
|--------------------------|-----|--------|------|------|--------------|-------|-------|
| Dimension Limits         |     | MIN    | NOM  | MAX  | MIN          | NOM   | MAX   |
| Number of Pins           | n   |        | 64   |      |              | 64    |       |
| Pitch                    | p   |        | .020 |      |              | 0.50  |       |
| Pins per Side            | n1  |        | 16   |      |              | 16    |       |
| Overall Height           | A   | .039   | .043 | .047 | 1.00         | 1.10  | 1.20  |
| Molded Package Thickness | A2  | .037   | .039 | .041 | 0.95         | 1.00  | 1.05  |
| Standoff §               | A1  | .002   | .006 | .010 | 0.05         | 0.15  | 0.25  |
| Foot Length              | L   | .018   | .024 | .030 | 0.45         | 0.60  | 0.75  |
| Footprint (Reference)    | (F) |        | .039 |      |              | 1.00  |       |
| Foot Angle               | φ   | 0      | 3.5  | 7    | 0            | 3.5   | 7     |
| Overall Width            | E   | .463   | .472 | .482 | 11.75        | 12.00 | 12.25 |
| Overall Length           | D   | .463   | .472 | .482 | 11.75        | 12.00 | 12.25 |
| Molded Package Width     | E1  | .390   | .394 | .398 | 9.90         | 10.00 | 10.10 |
| Molded Package Length    | D1  | .390   | .394 | .398 | 9.90         | 10.00 | 10.10 |
| Lead Thickness           | c   | .005   | .007 | .009 | 0.13         | 0.18  | 0.23  |
| Lead Width               | B   | .007   | .009 | .011 | 0.17         | 0.22  | 0.27  |
| Pin 1 Corner Chamfer     | CH  | .025   | .035 | .045 | 0.64         | 0.89  | 1.14  |
| Mold Draft Angle Top     | α   | 5      | 10   | 15   | 5            | 10    | 15    |
| Mold Draft Angle Bottom  | β   | 5      | 10   | 15   | 5            | 10    | 15    |

\* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-026

Drawing No. C04-085

28.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

Note:

V q V V

FIGURE 28-1: TYPICAL I<sub>DD</sub> vs. F<sub>OSC</sub> OVER V<sub>DD</sub> (HS MODE)

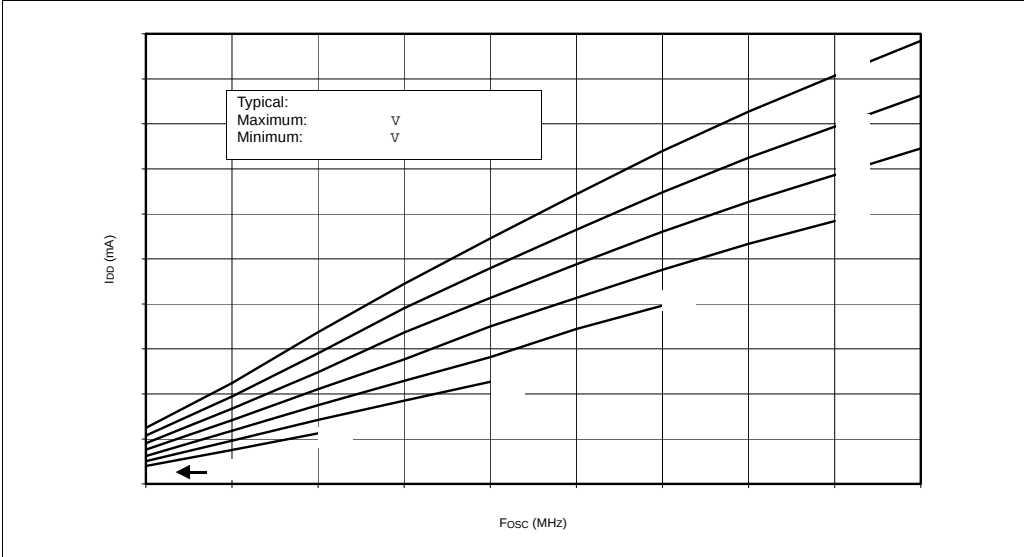
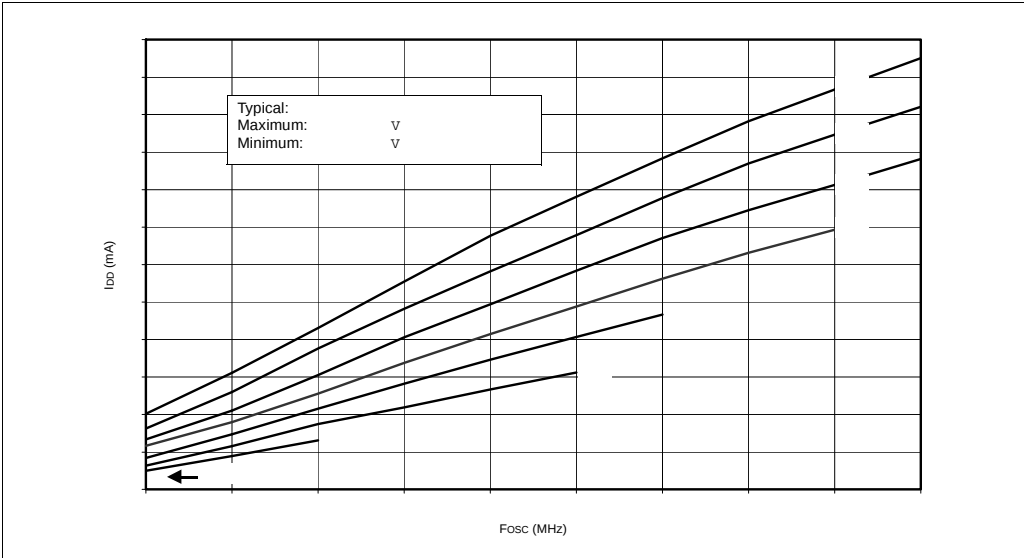


FIGURE 28-2: MAXIMUM I<sub>DD</sub> vs. F<sub>OSC</sub> OVER V<sub>DD</sub> (HS MODE)



# PIC18F6585/8585/6680/8680

FIGURE 28-19: TYPICAL, MINIMUM AND MAXIMUM WDT PERIOD vs. V<sub>DD</sub>

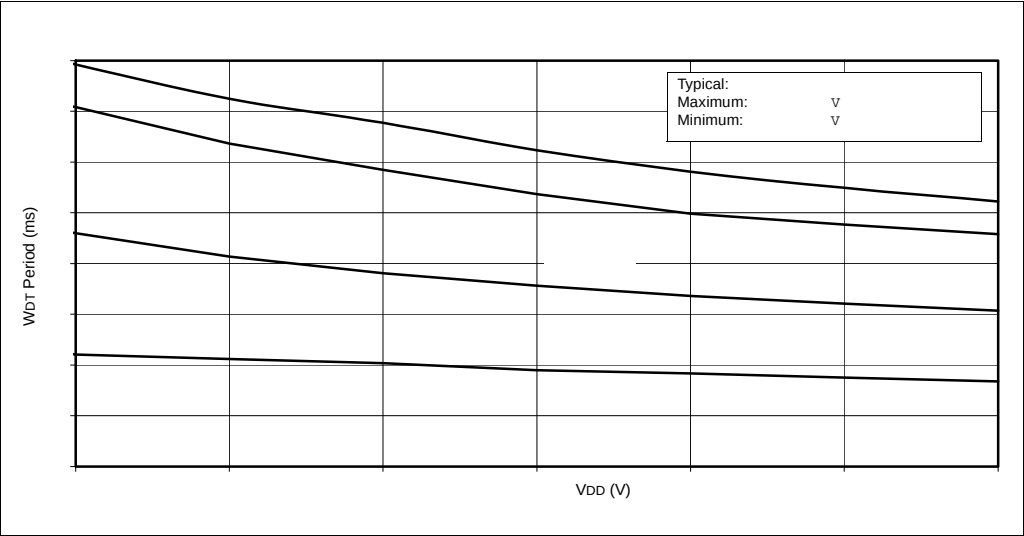


FIGURE 28-20: I<sub>LVD</sub> vs. V<sub>DD</sub> OVER TEMPERATURE, V<sub>LVD</sub> = 4.5-4.78V

