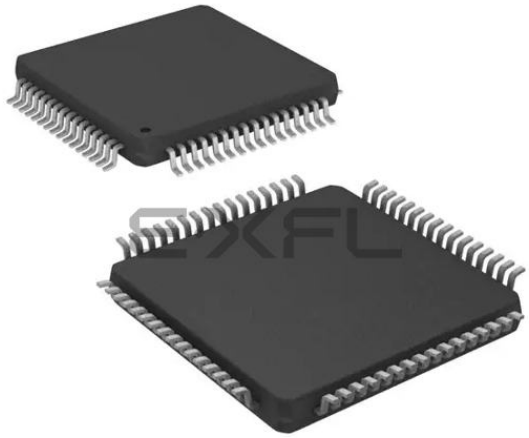

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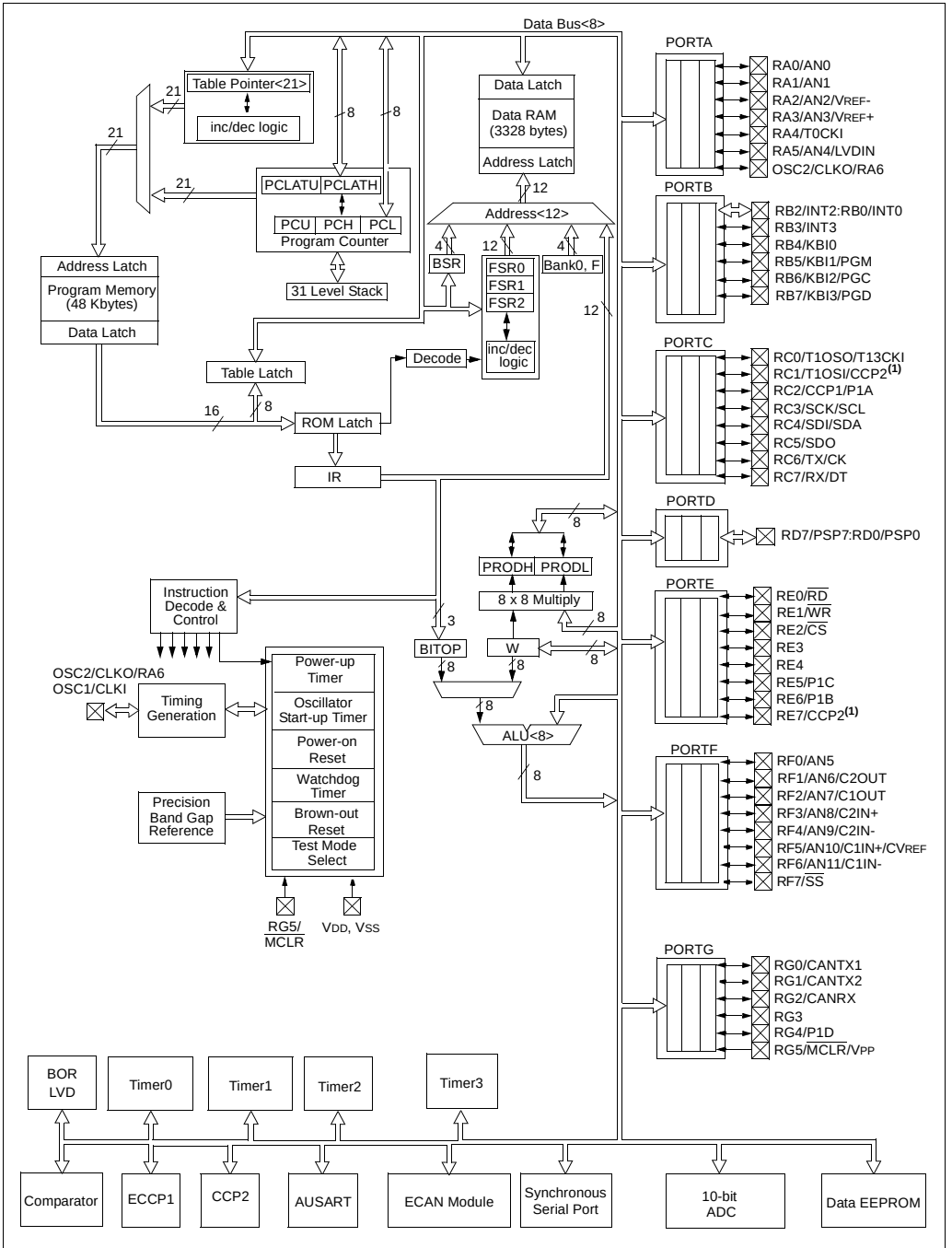
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 40MHz |
| Connectivity | CANbus, I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, LVD, POR, PWM, WDT |
| Number of I/O | 52 |
| Program Memory Size | 64KB (32K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 3.25K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.2V ~ 5.5V |
| Data Converters | A/D 16x10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TQFP |
| Supplier Device Package | 64-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic18f6680-i-pt |

**FIGURE 1-1: PIC18F6X8X BLOCK DIAGRAM**




**Note 1:** The CCP2 pin placement depends on the CCP2MX and Processor mode settings.

**TABLE 1-2: PIC18F6585/8585/6680/8680 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| | PIC18F6X8X | | PIC18F8X8X | | | |
| | TQFP | PLCC | TQFP | | | |
| | | | | | | PORTJ is a bidirectional I/O port(5). |
| RJ0/ALE | — | — | 62 | | | |
| RJ0 | | | | I/O | ST | Digital I/O. |
| ALE | | | | O | TTL | External memory address latch enable. |
| RJ1/$\overline{OE}$ | — | — | 61 | | | |
| RJ1 | | | | I/O | ST | Digital I/O. |
| $\overline{OE}$ | | | | O | TTL | External memory output enable. |
| RJ2/$\overline{WRL}$ | — | — | 60 | | | |
| RJ2 | | | | I/O | ST | Digital I/O. |
| $\overline{WRL}$ | | | | O | TTL | External memory write low control. |
| RJ3/$\overline{WRH}$ | — | — | 59 | | | |
| RJ3 | | | | I/O | ST | Digital I/O. |
| $\overline{WRH}$ | | | | O | TTL | External memory write high control. |
| RJ4/BA0 | — | — | 39 | | | |
| RJ4 | | | | I/O | ST | Digital I/O. |
| BA0 | | | | O | TTL | System bus byte address 0 control. |
| RJ5/$\overline{CE}$ | — | — | 40 | I/O | ST | Digital I/O |
| $\overline{CE}$ | | | | O | TTL | External memory chip enable. |
| RJ6/$\overline{LB}$ | — | — | 42 | | | |
| RJ6 | | | | I/O | ST | Digital I/O. |
| $\overline{LB}$ | | | | O | TTL | External memory low byte select. |
| RJ7/$\overline{UB}$ | — | — | 41 | | | |
| RJ7 | | | | I/O | ST | Digital I/O. |
| $\overline{UB}$ | | | | O | TTL | External memory high byte select. |
| VSS | 9, 25, 41, 56 | 19, 36, 53, 68 | 11, 31, 51, 70 | P | — | Ground reference for logic and I/O pins. |
| VDD | 10, 26, 38, 57 | 2, 20, 37, 49 | 12, 32, 48, 71 | P | — | Positive supply for logic and I/O pins. |
| AVSS | 20 | 30 | 26 | P | — | Ground reference for analog modules. |
| AVDD | 19 | 29 | 25 | P | — | Positive supply for analog modules. |
| NC | — | 1, 18, 35, 52 | — | — | — | No connect. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD)

**Note 1:** Alternate assignment for CCP2 in all operating modes except Microcontroller – applies to PIC18F8X8X only.

**2:** Default assignment when CCP2MX is set.

**3:** External memory interface functions are only available on PIC18F8X8X devices.

**4:** CCP2 is multiplexed with this pin by default when configured in Microcontroller mode; otherwise, it is multiplexed with either RB3 or RC1.

**5:** PORTH and PORTJ are only available on PIC18F8X8X (80-pin) devices.

**6:** PSP is available in Microcontroller mode only.

**7:** On PIC18F8X8X devices, these pins can be multiplexed with RH7/RH6 by changing the ECCPMX configuration bit.

**TABLE 3-3: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)**

| Register | Applicable Devices | | Power-on Reset, Brown-out Reset | $\overline{\text{MCLR}}$ Resets WDT Reset RESET Instruction Stack Resets | Wake-up via WDT or Interrupt |
|---|---|---|---|---|---|
| PORTJ | PIC18F6X8X | PIC18F8X8X | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PORTH | PIC18F6X8X | PIC18F8X8X | 0000 xxxx | 0000 uuuu | uuuu uuuu |
| PORTG | PIC18F6X8X | PIC18F8X8X | --xx xxxx | --uu uuuu | --uu uuuu |
| PORTF | PIC18F6X8X | PIC18F8X8X | x000 0000 | u000 0000 | u000 0000 |
| PORTE | PIC18F6X8X | PIC18F8X8X | ---- -000 | ---- -000 | ---- -uuu |
| PORTD | PIC18F6X8X | PIC18F8X8X | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PORTC | PIC18F6X8X | PIC18F8X8X | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PORTB | PIC18F6X8X | PIC18F8X8X | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PORTA(5,6) | PIC18F6X8X | PIC18F8X8X | -x0x 0000(5) | -u0u 0000(5) | -uuu uuuu(5) |
| SPBRGH | PIC18F6X8X | PIC18F8X8X | 0000 0000 | 0000 0000 | uuuu uuuu |
| BAUDCON | PIC18F6X8X | PIC18F8X8X | -1-0 0-00 | -1-0 0-00 | -u-u u-uu |
| ECCP1DEL | PIC18F6X8X | PIC18F8X8X | 0000 0000 | 0000 0000 | uuuu uuuu |
| ECANCON | PIC18F6X8X | PIC18F8X8X | 0001 0000 | 0001 0000 | uuuu uuuu |
| TXERRCNT | PIC18F6X8X | PIC18F8X8X | 0000 0000 | 0000 0000 | uuuu uuuu |
| RXERRCNT | PIC18F6X8X | PIC18F8X8X | 0000 0000 | 0000 0000 | uuuu uuuu |
| COMSTAT | PIC18F6X8X | PIC18F8X8X | 0000 0000 | 0000 0000 | uuuu uuuu |
| CIOCON | PIC18F6X8X | PIC18F8X8X | 0000 ---- | 0000 ---- | uuuu ---- |
| BRGCON3 | PIC18F6X8X | PIC18F8X8X | 00-- -000 | 00-- -000 | uu-- -uuu |
| BRGCON2 | PIC18F6X8X | PIC18F8X8X | 0000 0000 | 0000 0000 | uuuu uuuu |
| BRGCON1 | PIC18F6X8X | PIC18F8X8X | 0000 0000 | 0000 0000 | uuuu uuuu |
| CANCON | PIC18F6X8X | PIC18F8X8X | 1000 000- | 1000 000- | uuuu uuu- |
| CANSTAT | PIC18F6X8X | PIC18F8X8X | 100- 000- | 100- 000- | uuu- uuu- |
| RXB0D7 | PIC18F6X8X | PIC18F8X8X | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| RXB0D6 | PIC18F6X8X | PIC18F8X8X | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| RXB0D5 | PIC18F6X8X | PIC18F8X8X | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| RXB0D4 | PIC18F6X8X | PIC18F8X8X | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| RXB0D3 | PIC18F6X8X | PIC18F8X8X | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| RXB0D2 | PIC18F6X8X | PIC18F8X8X | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| RXB0D1 | PIC18F6X8X | PIC18F8X8X | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| RXB0D0 | PIC18F6X8X | PIC18F8X8X | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| RXB0DLC | PIC18F6X8X | PIC18F8X8X | -xxx xxxx | -uuu uuuu | -uuu uuuu |

**Legend:** u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

**Note 1:** One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

**2:** When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

**3:** When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

**4:** See Table 3-2 for Reset value for specific condition.

**5:** Bit 6 of PORTA, LATA, and TRISA are enabled in ECIO and RCIO Oscillator modes only. In all other oscillator modes, they are disabled and read '0'.

**6:** Bit 6 of PORTA, LATA and TRISA are not available on all devices. When unimplemented, they read '0'.

**7:** This register reads all '0's until ECAN is set up in Mode 1 or Mode 2.

**REGISTER 9-2: INTCON2 REGISTER**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| $\overline{\text{RBPU}}$ | INTEDG0 | INTEDG1 | INTEDG2 | INTEDG3 | TMR0IP | INT3IP | RBIP |
| bit 7 | | | | | | | bit 0 |

bit 7 **$\overline{\text{RBPU}}$**: PORTB Pull-up Enable bit
1 = All PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

bit 6 **INTEDG0**: External Interrupt 0 Edge Select bit
1 = Interrupt on rising edge
0 = Interrupt on falling edge

bit 5 **INTEDG1**: External Interrupt 1 Edge Select bit
1 = Interrupt on rising edge
0 = Interrupt on falling edge

bit 4 **INTEDG2**: External Interrupt 2 Edge Select bit
1 = Interrupt on rising edge
0 = Interrupt on falling edge

bit 3 **INTEDG3**: External Interrupt 3 Edge Select bit
1 = Interrupt on rising edge
0 = Interrupt on falling edge

bit 2 **TMR0IP**: TMR0 Overflow Interrupt Priority bit
1 = High priority
0 = Low priority

bit 1 **INT3IP:** INT3 External Interrupt Priority bit
1 = High priority
0 = Low priority

bit 0 **RBIP**: RB Port Change Interrupt Priority bit
1 = High priority
0 = Low priority

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| - n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

**Note:** Interrupt flag bits are set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. This feature allows for software polling.

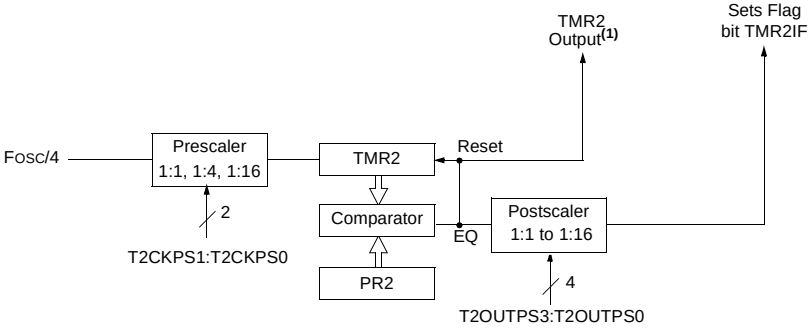
## 13.2 Timer2 Interrupt

The Timer2 module has an 8-bit period register, PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to 0FFh upon Reset.

## 13.3 Output of TMR2

The output of TMR2 (before the postscaler) is fed to the synchronous serial port module which optionally uses it to generate the shift clock.

**FIGURE 13-1: TIMER2 BLOCK DIAGRAM**




**Note 1:** TMR2 register output can be software selected by the SSP module as a baud clock.

**TABLE 13-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| INTCON | GIE/GIEH | PEIE/GIEL | TMR0IE | INT0IE | RBIE | TMR0IF | INT0IF | RBIF | 0000 0000 | 0000 0000 |
| PIR1 | PSPIF | ADIF | RCIF | TXIF | SSPIF | CCP1IF | TMR2IF | TMR1IF | 0000 0000 | 0000 0000 |
| PIE1 | PSPIE | ADIE | RCIE | TXIE | SSPIE | CCP1IE | TMR2IE | TMR1IE | 0000 0000 | 0000 0000 |
| IPR1 | PSPIP | ADIP | RCIP | TXIP | SSPIP | CCP1IP | TMR2IP | TMR1IP | 1111 1111 | 1111 1111 |
| TMR2 | Timer2 Module Register | | | | | | | | 0000 0000 | 0000 0000 |
| T2CON | — | T2OUTPS3 | T2OUTPS2 | T2OUTPS1 | T2OUTPS0 | TMR2ON | T2CKPS1 | T2CKPS0 | -000 0000 | -000 0000 |
| PR2 | Timer2 Period Register | | | | | | | | 1111 1111 | 1111 1111 |

**Legend:** x = unknown, u = unchanged, – = unimplemented, read as '0'. Shaded cells are not used by the Timer2 module.

### 16.2.6 PROGRAMMABLE DEAD-BAND DELAY

In half-bridge applications where all power switches are modulated at the PWM frequency at all times, the power switches normally require more time to turn off than to turn on. If both the upper and lower power switches are switched at the same time (one turned on and the other turned off), both switches may be on for a short period of time until one switch completely turns off. During this brief interval, a very high current (shoot-through current) may flow through both power switches, shorting the bridge supply. To avoid this potentially destructive shoot-through current from flowing during switching, turning on either of the power switches is normally delayed to allow the other switch to completely turn off.

In the Half-Bridge Output mode, a digitally programmable dead-band delay is available to avoid shoot-through current from destroying the bridge power switches. The delay occurs at the signal transition from the non-active state to the active state. See Figure 16-5 for an illustration. The lower seven bits of the ECCP1DEL register (Register 16-2) set the delay period in terms of microcontroller instruction cycles (TCY or 4 TOSC).

### 16.2.7 ENHANCED PWM AUTO-SHUTDOWN

When the CCP1 is programmed for any of the enhanced PWM modes, the active output pins may be configured for auto-shutdown. Auto-shutdown immediately places the enhanced PWM output pins into a defined shutdown state when a shutdown event occurs.

A shutdown event can be caused by either of the two comparator modules or a low level on the RB0 pin (or any combination of these three sources). The comparators may be used to monitor a voltage input proportional to a current being monitored in the bridge circuit. If the voltage exceeds a threshold, the comparator switches state and triggers a shutdown. Alternatively, a low digital signal on the RB0 pin can also trigger a shutdown. The auto-shutdown feature can be disabled by not selecting any auto-shutdown sources. The auto-shutdown sources to be used are selected using the ECCPAS2:ECCPAS0 bits (bits <6:4> of the ECCP1AS register).

When a shutdown occurs, the output pins are asynchronously placed in their shutdown states, specified by the PSSAC1:PSSAC0 and PSSBD1:PSSBD0 bits (ECCP1AS<3:0>). Each pin pair (P1A/P1C and P1B/P1D) may be set to drive high, drive low, or be tri-stated (not driving). The ECCPASE bit (ECCP1AS<7>) is also set to hold the enhanced PWM outputs in their shutdown states.

The ECCPASE bit is set by hardware when a shutdown event occurs. If automatic restarts are not enabled, the ECCPASE bit is cleared by firmware when the cause of the shutdown clears. If automatic restarts are enabled, the ECCPASE bit is automatically cleared when the cause of the auto-shutdown has cleared.

If the ECCPASE bit is set when a PWM period begins, the PWM outputs remain in their shutdown state for that entire PWM period. When the ECCPASE bit is cleared, the PWM outputs will return to normal operation at the beginning of the next PWM period.

| **Note:** | Writing to the ECCPASE bit is disabled while a shutdown condition is active. |
|---|---|

**REGISTER 16-2: ECCP1DEL: ECCP1 DELAY REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PRSEN | PDC6 | PDC5 | PDC4 | PDC3 | PDC2 | PDC1 | PDC0 |
| bit 7 | | | | | | | bit 0 |

bit 7 **PRSEN:** PWM Restart Enable bit

1 = Upon auto-shutdown, the ECCPASE bit clears automatically once the shutdown event goes away; the PWM restarts automatically

0 = Upon auto-shutdown, ECCPASE must be cleared in software to restart the PWM

bit 6-0 **PDC<6:0>:** PWM Delay Count bits

Number of FOSC/4 (4 * TOSC) cycles between the scheduled time when a PWM signal should transition active and the actual time it transitions active.

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| - n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

**FIGURE 17-21: $I^2C$ MASTER MODE WAVEFORM (TRANSMISSION, 7 OR 10-BIT ADDRESS)**

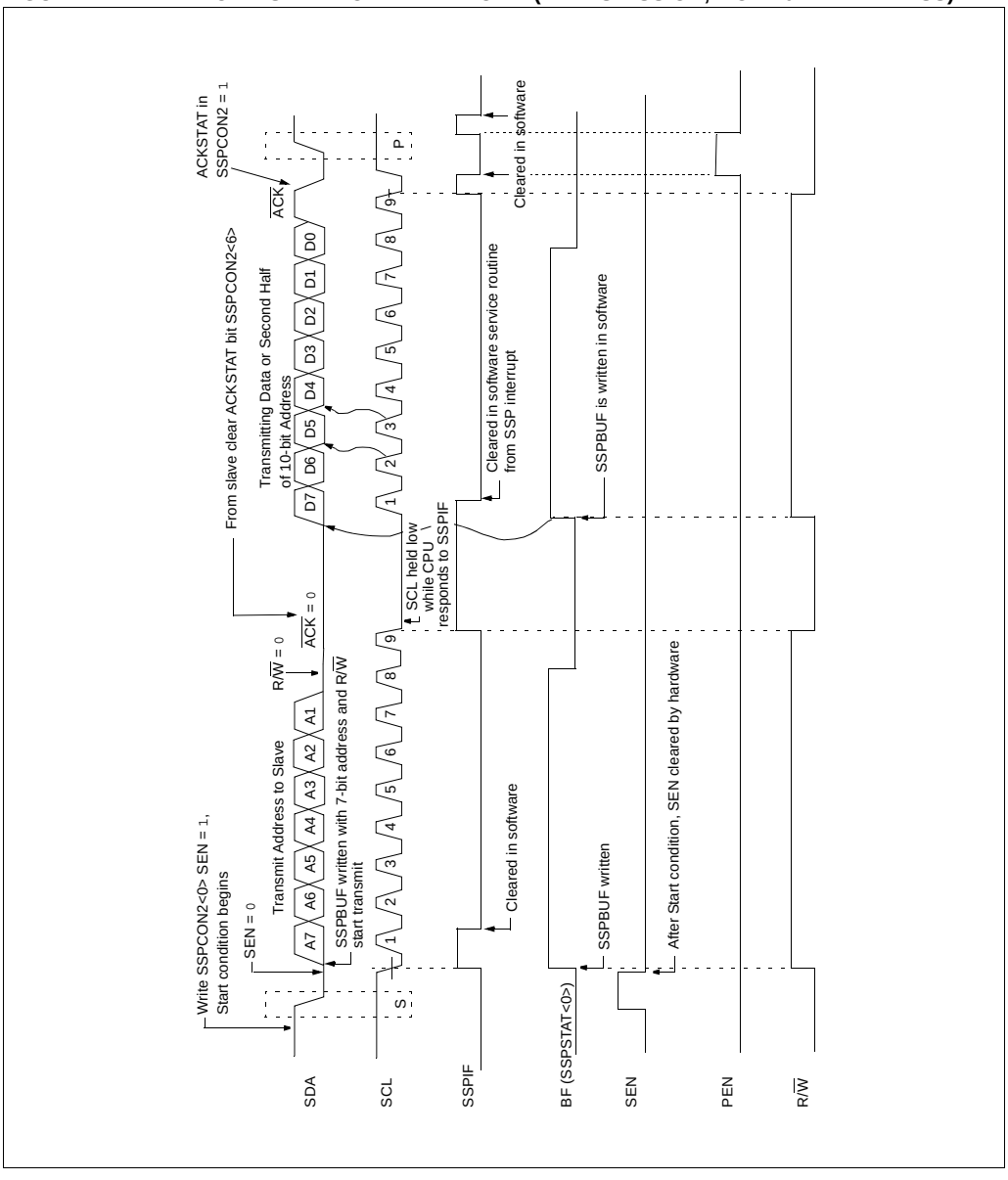


**FIGURE 18-2: USART TRANSMIT BLOCK DIAGRAM**

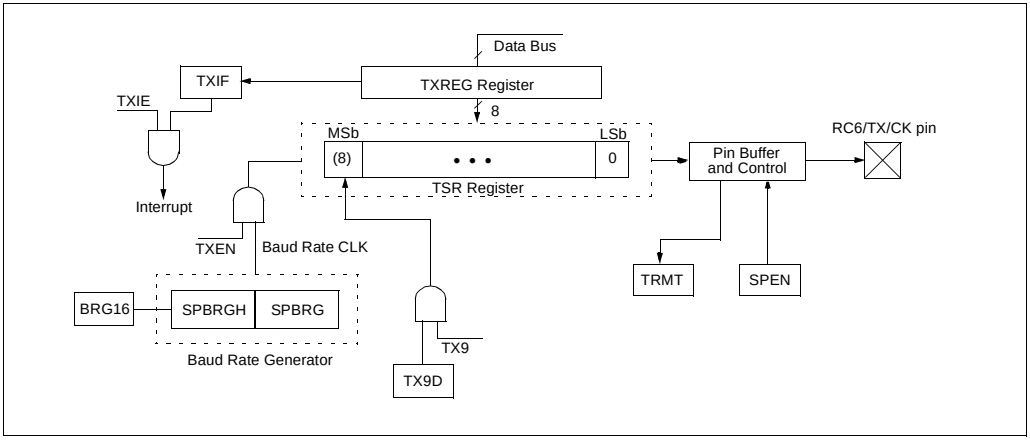



**FIGURE 18-3: ASYNCHRONOUS TRANSMISSION**

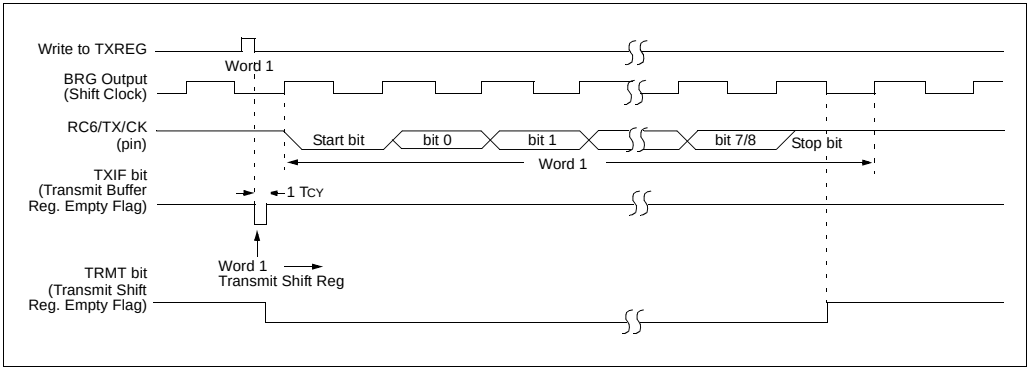
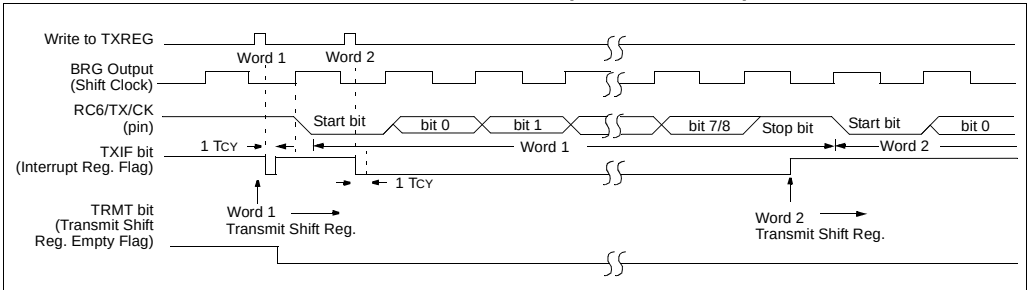



**FIGURE 18-4: ASYNCHRONOUS TRANSMISSION (BACK TO BACK)**




**Note:** This timing diagram shows two consecutive transmissions.

**TABLE 19-2: SUMMARY OF A/D REGISTERS**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| INTCON | GIE/GIEH | PEIE/GIEL | TMR0IE | INT0IE | RBIE | TMR0IF | INT0IF | RBIF | 0000 0000 | 0000 0000 |
| PIR1 | PSPIF | ADIF | RCIF | TXIF | SSPIF | CCP1IF | TMR2IF | TMR1IF | 0000 0000 | 0000 0000 |
| PIE1 | PSPIE | ADIE | RCIE | TXIE | SSPIE | CCP1IE | TMR2IE | TMR1IE | 0000 0000 | 0000 0000 |
| IPR1 | PSPIP | ADIP | RCIP | TXIP | SSPIP | CCP1IP | TMR2IP | TMR1IP | 1111 1111 | 1111 1111 |
| PIR2 | — | CMIF | — | EEIF | BCLIF | LVDIF | TMR3IF | CCP2IF | -0-0 0000 | -0-0 0000 |
| PIE2 | — | CMIE | — | EEIE | BCLIE | LVDIE | TMR3IE | CCP2IE | -0-0 0000 | -0-0 0000 |
| IPR2 | — | CMIP | — | EEIP | BCLIP | LVDIP | TMR3IP | CCP2IP | -1-1 1111 | -1-1 1111 |
| ADRESH | A/D Result Register High Byte | | | | | | | | xxxx xxxx | uuuu uuuu |
| ADRESL | A/D Result Register Low Byte | | | | | | | | xxxx xxxx | uuuu uuuu |
| ADCON0 | — | — | CHS3 | CHS3 | CHS1 | CHS0 | GO/$\overline{\text{DONE}}$ | ADON | --00 0000 | --00 0000 |
| ADCON1 | — | — | VCFG1 | VCFG0 | PCFG3 | PCFG2 | PCFG1 | PCFG0 | --00 0000 | --00 0000 |
| ADCON2 | ADFM | — | — | — | — | ADCS2 | ADCS1 | ADCS0 | 0--- -000 | 0--- -000 |
| PORTA | — | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | --xx xxxx | --uu uuuu |
| TRISA | — | PORTA Data Direction Register | | | | | | | --11 1111 | --11 1111 |
| PORTF | RF7 | RF6 | RF5 | RF4 | RF3 | RF2 | RF1 | RF0 | xxxx xxxx | uuuu uuuu |
| LATF | LATF7 | LATF6 | LATF5 | LATF4 | LATF3 | LATF2 | LATF1 | LATF0 | xxxx xxxx | uuuu uuuu |
| TRISF | PORTF Data Direction Control Register | | | | | | | | 1111 1111 | 1111 1111 |
| PORTH(1) | RH7 | RH6 | RH5 | RH4 | RH3 | RH2 | RH1 | RH0 | xxxx xxxx | uuuu uuuu |
| LATH(1) | LATH7 | LATH6 | LATH5 | LATH4 | LATH3 | LATH2 | LATH1 | LATH0 | xxxx xxxx | uuuu uuuu |
| TRISH(1) | PORTH Data Direction Control Register | | | | | | | | 1111 1111 | 1111 1111 |

**Legend:** x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

**Note 1:** Only available on PIC18F8X8X devices.

**REGISTER 23-47: RXFBCONn: RECEIVE FILTER BUFFER CONTROL REGISTER n(1)**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **RXFBCON0** | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | F1BP_3 | F1BP_2 | F1BP_1 | F1BP_0 | F0BP_3 | F0BP_2 | F0BP_1 | F0BP_0 |
| **RXFBCON1** | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-1 |
| | F3BP_3 | F3BP_2 | F3BP_1 | F3BP_0 | F2BP_3 | F2BP_2 | F2BP_1 | F2BP_0 |
| **RXFBCON2** | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-1 |
| | F5BP_3 | F5BP_2 | F5BP_1 | F5BP_0 | F4BP_3 | F4BP_2 | F4BP_1 | F4BP_0 |
| **RXFBCON3** | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | F7BP_3 | F7BP_2 | F7BP_1 | F7BP_0 | F6BP_3 | F6BP_2 | F6BP_1 | F6BP_0 |
| **RXFBCON4** | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | F9BP_3 | F9BP_2 | F9BP_1 | F9BP_0 | F8BP_3 | F8BP_2 | F8BP_1 | F8BP_0 |
| **RXFBCON5** | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | F11BP_3 | F11BP_2 | F11BP_1 | F11BP_0 | F10BP_3 | F10BP_2 | F10BP_1 | F10BP_0 |
| **RXFBCON6** | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | F13BP_3 | F13BP_2 | F13BP_1 | F13BP_0 | F12BP_3 | F12BP_2 | F12BP_1 | F12BP_0 |
| **RXFBCON7** | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | F15BP_3 | F15BP_2 | F15BP_1 | F15BP_0 | F14BP_3 | F14BP_2 | F14BP_1 | F14BP_0 |
| | bit 7 | | | | | | | bit 0 |

bit 7-0 **FnBP_3:FnBP_0:** Filter n Buffer Pointer Nibble bits

0000 = Filter n is associated with RXB0
0001 = Filter n is associated with RXB1
0010 = Filter n is associated with B0
0011 = Filter n is associated with B1
.
.
.
0111 = Filter n is associated with B5
1111:1000 = Reserved

**Note 1:** This register is available in Mode 1 and 2 only.

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

### 23.2.6 CAN INTERRUPT REGISTERS

The registers in this section are the same as described in **Section 9.0 "Interrupts"**. They are duplicated here for convenience.

**REGISTER 23-56: PIR3: PERIPHERAL INTERRUPT FLAG REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IRXIF | WAKIF | ERRIF | TXB2IF/ TXBnIF | TXB1IF(1) | TXB0IF(1) | RXB1IF/ RXBnIF | RXB0IF/ FIFOWMIF |
| bit 7 | | | | | | | bit 0 |

bit 7 **IRXIF:** CAN Invalid Received Message Interrupt Flag bit
1 = An invalid message has occurred on the CAN bus
0 = No invalid message on CAN bus

bit 6 **WAKIF:** CAN bus Activity Wake-up Interrupt Flag bit
1 = Activity on CAN bus has occurred
0 = No activity on CAN bus

bit 5 **ERRIF:** CAN bus Error Interrupt Flag bit
1 = An error has occurred in the CAN module (multiple sources)
0 = No CAN module errors

bit 4 When CAN is in Mode 0:
**TXB2IF:** CAN Transmit Buffer 2 Interrupt Flag bit
1 = Transmit Buffer 2 has completed transmission of a message and may be reloaded
0 = Transmit Buffer 2 has not completed transmission of a message
When CAN is in Mode 1 or 2:
**TXBnIF:** Any Transmit Buffer Interrupt Flag bit
1 = One or more transmit buffers has completed transmission of a message and may be reloaded
0 = No transmit buffer is ready for reload

bit 3 **TXB1IF:** CAN Transmit Buffer 1 Interrupt Flag bit(1)
1 = Transmit Buffer 1 has completed transmission of a message and may be reloaded
0 = Transmit Buffer 1 has not completed transmission of a message

bit 2 **TXB0IF:** CAN Transmit Buffer 0 Interrupt Flag bit(1)
1 = Transmit Buffer 0 has completed transmission of a message and may be reloaded
0 = Transmit Buffer 0 has not completed transmission of a message

bit 1 When CAN is in Mode 0:
**RXB1IF:** CAN Receive Buffer 1 Interrupt Flag bit
1 = Receive Buffer 1 has received a new message
0 = Receive Buffer 1 has not received a new message
When CAN is in Mode 1 or 2:
**RXBnIF:** Any Receive Buffer Interrupt Flag bit
1 = One or more receive buffers has received a new message
0 = No receive buffer has received a new message

bit 0 When CAN is in Mode 0:
**RXB0IF:** CAN Receive Buffer 0 Interrupt Flag bit
1 = Receive Buffer 0 has received a new message
0 = Receive Buffer 0 has not received a new message
When CAN is in Mode 1:
**Unimplemented:** Read as '0'
When CAN is in Mode 2:
**FIFOWMIF:** FIFO Watermark Interrupt Flag bit
1 = FIFO high watermark is reached
0 = FIFO high watermark is not reached

**Note 1:** In CAN Mode 1 and 2, this bit is forced to '0'.

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

**REGISTER 23-59: TXBIE: TRANSMIT BUFFERS INTERRUPT ENABLE REGISTER(1)**

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | TXB2IE | TXB1IE | TXB0IE | — | — |
| bit 7 | | | | | | | bit 0 |

bit 7-5 **Unimplemented:** Read as '0'

bit 4-2 **TX2BIE:TXB0IE:** Transmit Buffer 2-0 Interrupt Enable bit(2)

1 = Transmit buffer interrupt is enabled
0 = Transmit buffer interrupt is disabled

bit 1-0 **Unimplemented:** Read as '0'

**Note 1:** This register is available in Mode 1 and 2 only.

**2:** TXBIE in PIE3 register must be set to get an interrupt.

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

**REGISTER 23-60: BIE0: BUFFER INTERRUPT ENABLE REGISTER 0(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| B5IE | B4IE | B3IE | B2IE | B1IE | B0IE | RXB1IE | RXB0IE |
| bit 7 | | | | | | | bit 0 |

bit 7-2 **B5IE:B0IE:** Programmable Transmit/Receive Buffer 5-0 Interrupt Enable bit(2)

1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1-0 **RXB1IE:RXB0IE:** Dedicated Receive Buffer 1-0 Interrupt Enable bit(2)

1 = Interrupt is enabled
0 = Interrupt is disabled

**Note 1:** This register is available in Mode 1 and 2 only.

**2:** Either TXBIE or RXBIE in PIE3 register must be set to get an interrupt.

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

**BTG** **Bit Toggle f**

Syntax: [ *label* ] BTG f,b[,a]

Operands: $0 \le f \le 255$
$0 \le b < 7$
$a \in [0,1]$

Operation: $(\overline{f<b>}) \rightarrow f<b>$

Status Affected: None

Encoding:

| | | | |
|---|---|---|---|
| 0111 | bbba | ffff | ffff |

Description: Bit 'b' in data memory location 'f' is inverted. If 'a' is '0', the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Process Data | Write register 'f' |

Example:
```
BTG     PORTC,  4, 0
```
Before Instruction:
PORTC = 0111 0101 [0x75]
After Instruction:
PORTC = 0110 0101 [0x65]

**BOV** **Branch if Overflow**

Syntax: [ *label* ] BOV n

Operands: $-128 \le n \le 127$

Operation: if overflow bit is '1'
(PC) + 2 + 2n → PC

Status Affected: None

Encoding:

| | | | |
|---|---|---|---|
| 1110 | 0100 | nnnn | nnnn |

Description: If the Overflow bit is '1', then the program will branch.
The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is then a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:
If Jump:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read literal 'n' | Process Data | Write to PC |
| No operation | No operation | No operation | No operation |

If No Jump:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read literal 'n' | Process Data | No operation |

Example:
```
HERE    BOV  Jump
```
Before Instruction
PC = address (HERE)
After Instruction
If Overflow = 1;
PC = address (Jump)
If Overflow = 0;
PC = address (HERE+2)

## 26.20 PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. A programmed sample is included. The PRO MATE II device programmer, or the PICSTART Plus development programmer, can be used to reprogram the device for user tailored application development. The PICDEM 17 demonstration board supports program download and execution from external on-board Flash memory. A generous prototype area is available for user hardware expansion.

## 26.21 PICDEM 18R PIC18C601/801 Demonstration Board

The PICDEM 18R demonstration board serves to assist development of the PIC18C601/801 family of Microchip microcontrollers. It provides hardware implementation of both 8-bit Multiplexed/Demultiplexed and 16-bit Memory modes. The board includes 2 Mb external Flash memory and 128 Kb SRAM memory, as well as serial EEPROM, allowing access to the wide range of memory types supported by the PIC18C601/801.

## 26.22 PICDEM LIN PIC16C43X Demonstration Board

The powerful LIN hardware and software kit includes a series of boards and three PIC microcontrollers. The small footprint PIC16C432 and PIC16C433 are used as slaves in the LIN communication and feature on-board LIN transceivers. A PIC16F874 Flash microcontroller serves as the master. All three microcontrollers are programmed with firmware to provide LIN bus communication.

## 26.23 PICkit™ 1 Flash Starter Kit

A complete “development system in a box”, the PICkit Flash Starter Kit includes a convenient multi-section board for programming, evaluation and development of 8/14-pin Flash PIC® microcontrollers. Powered via USB, the board operates under a simple Windows GUI. The PICkit 1 Starter Kit includes the User’s Guide (on CD ROM), PICkit 1 tutorial software and code for various applications. Also included are MPLAB® IDE (Integrated Development Environment) software, software and hardware “Tips 'n Tricks for 8-pin Flash PIC® Microcontrollers” Handbook and a USB interface cable. Supports all current 8/14-pin Flash PIC microcontrollers, as well as many future planned devices.

## 26.24 PICDEM USB PIC16C7X5 Demonstration Board

The PICDEM USB Demonstration Board shows off the capabilities of the PIC16C745 and PIC16C765 USB microcontrollers. This board provides the basis for future USB products.

## 26.25 Evaluation and Programming Tools

In addition to the PICDEM series of circuits, Microchip has a line of evaluation kits and demonstration software for these products.

- KEELOQ evaluation and programming tools for Microchip’s HCS Secure Data Products
- CAN developers kit for automotive network applications
- Analog design boards and filter design software
- PowerSmart battery charging evaluation/ calibration kits
- IrDA® development kit
- microID development and rfLab™ development software
- SEEVAL® designer kit for memory evaluation and endurance calculations
- PICDEM MSC demo boards for Switching mode power supply, high-power IR driver, delta sigma ADC and flow rate sensor

Check the Microchip web page and the latest Product Selector Guide for the complete list of demonstration and evaluation kits.

27.4.3 TIMING DIAGRAMS AND SPECIFICATIONS

**FIGURE 27-6: EXTERNAL CLOCK TIMING (ALL MODES EXCEPT PLL)**

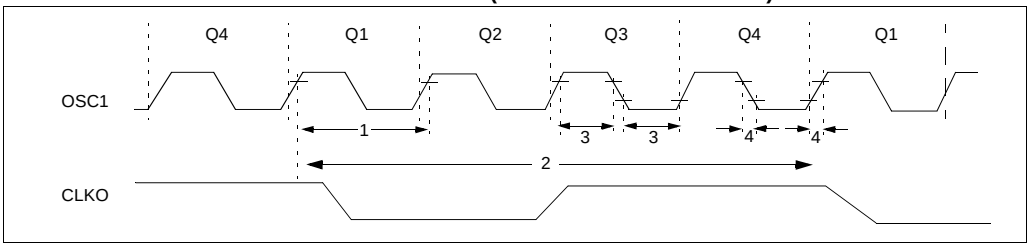



**TABLE 27-6: EXTERNAL CLOCK TIMING REQUIREMENTS**

| Param. No. | Symbol | Characteristic | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| 1A | FOSC | External CLKI Frequency(1) | DC | 40 | MHz | EC, ECIO, -40°C to +85°C |
| | | | DC | 25 | MHz | EC,ECIO, -40°C to +85°C, EMA |
| | | Oscillator Frequency(1) | DC | 25 | MHz | EC, ECIO, +85°C to +125°C |
| | | | DC | 16 | MHz | EC, ECIO, +85°C to +125°C, EMA |
| | | | DC | 4 | MHz | RC oscillator |
| | | | 0.1 | 4 | MHz | XT oscillator |
| | | | 4 | 25 | MHz | HS oscillator, -40°C to +85°C |
| | | | 4 | 25 | MHz | HS oscillator, -40°C to +85°C, EMA |
| | | | 4 | 25 | MHz | HS oscillator, +85°C to +125°C |
| | | | 4 | 16 | MHz | HS oscillator, +85°C to +125°C, EMA |
| | | | 4 | 10 | MHz | HS + PLL oscillator, -40°C to +85°C |
| | | | 4 | 6.25 | MHz | HS + PLL oscillator, +85°C to +125°C |
| | | | DC | 200 | kHz | LP oscillator |
| 1 | TOSC | External CLKI Period(1) | 25 | — | ns | EC, ECIO, -40°C to +85°C |
| | | Oscillator Period(1) | 40 | — | ns | EC,ECIO, -40°C to +85°C, EMA |
| | | | 40 | — | ns | EC, ECIO, +85°C to +125°C |
| | | | 62.5 | — | ns | EC, ECIO, +85°C to +125°C, EMA |
| | | | 250 | — | ns | RC oscillator |
| | | | 250 | 10,000 | ns | XT oscillator |
| | | | 40 | — | ns | HS oscillator, -40°C to +85°C |
| | | | 40 | — | ns | HS oscillator, -40°C to +85°C, EMA |
| | | | 40 | — | ns | HS oscillator, +85°C to +125°C |
| | | | 62.5 | — | ns | HS oscillator, +85°C to +125°C, EMA |
| | | | 100 | 250 | ns | HS + PLL oscillator, -40°C to +85°C |
| | | | 160 | 250 | ns | HS + PLL oscillator, +85°C to +125°C |
| | | | 5 | 200 | µs | LP oscillator |
| 2 | TCY | Instruction Cycle Time(1) | 100 | — | ns | TCY = 4/FOSC, -40°C to +85°C |
| | | | 160 | — | ns | TCY = 4/FOSC, +85°C to +125°C |
| 3 | TOSL, TOSH | External Clock in (OSC1) High or Low Time | 30 | — | ns | XT oscillator |
| | | | 2.5 | — | µs | LP oscillator |
| | | | 10 | — | ns | HS oscillator |
| 4 | TOSR, TOSF | External Clock in (OSC1) Rise or Fall Time | — | 20 | ns | XT oscillator |
| | | | — | 50 | ns | LP oscillator |
| | | | — | 7.5 | ns | HS oscillator |

**Note 1:** Instruction cycle period (TCY) equals four times the input oscillator time base period for all configurations except PLL. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min.” values with an external clock applied to the OSC1/CLKI pin. When an external clock input is used, the “max.” cycle time limit is “DC” (no clock) for all devices.

**FIGURE 27-18: EXAMPLE SPI SLAVE MODE TIMING (CKE = 1)**

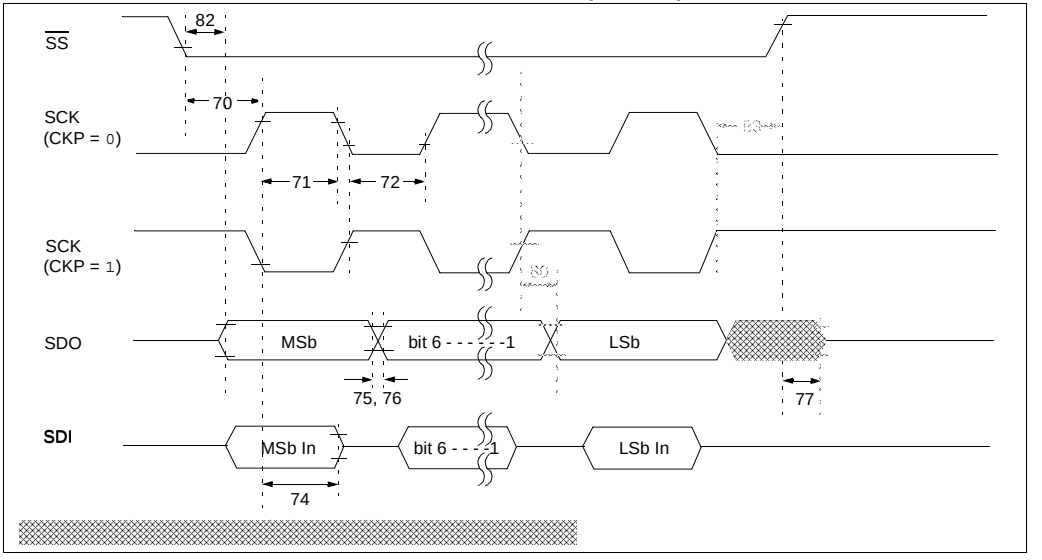


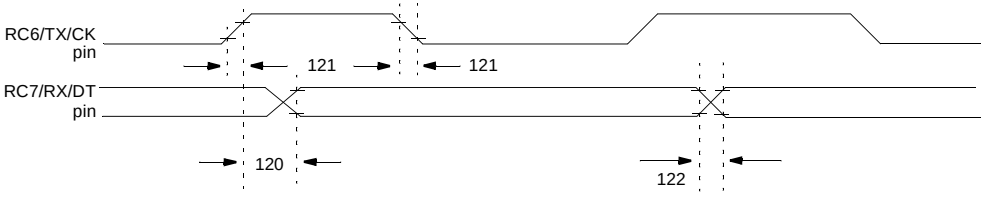

**TABLE 27-18: EXAMPLE SPI SLAVE MODE REQUIREMENTS (CKE = 1)**

| Param. No. | Symbol | Characteristic | | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 70 | TssL2scH, TssL2scL | $\overline{SS}$ ↓ to SCK ↓ or SCK ↑ Input | | TCY | — | ns | |
| 71 | TscH | SCK Input High Time (Slave mode) | Continuous | 1.25 TCY + 30 | — | ns | |
| 71A | | | Single Byte | 40 | — | ns | **(Note 1)** |
| 72 | TscL | SCK Input Low Time (Slave mode) | Continuous | 1.25 TCY + 30 | — | ns | |
| 72A | | | Single Byte | 40 | — | ns | **(Note 1)** |
| 73A | TB2B | Last Clock Edge of Byte 1 to the First Clock Edge of Byte 2 | | 1.5 TCY + 40 | — | ns | **(Note 2)** |
| 74 | TscH2diL, TscL2diL | Hold Time of SDI Data Input to SCK Edge | | 100 | — | ns | |
| 75 | TdoR | SDO Data Output Rise Time | PIC18FXX8X | — | 25 | ns | |
| | | | PIC18LFXX8X | | 45 | ns | |
| 76 | TdoF | SDO Data Output Fall Time | | — | 25 | ns | |
| 77 | TssH2doZ | $\overline{SS}$ ↑ to SDO Output High-Impedance | | 10 | 50 | ns | |
| 78 | TscR | SCK Output Rise Time (Master mode) | PIC18FXX8X | — | 25 | ns | |
| | | | PIC18LFXX8X | — | 45 | ns | |
| 79 | TscF | SCK Output Fall Time (Master mode) | | — | 25 | ns | |
| 80 | TscH2doV, TscL2doV | SDO Data Output Valid after SCK Edge | PIC18FXX8X | — | 50 | ns | |
| | | | PIC18LFXX8X | — | 100 | ns | |
| 82 | TssL2doV | SDO Data Output Valid after $\overline{SS}$ ↓ Edge | PIC18FXX8X | — | 50 | ns | |
| | | | PIC18LFXX8X | — | 100 | ns | |
| 83 | TscH2ssH, TscL2ssH | $\overline{SS}$ ↑ after SCK Edge | | 1.5 TCY + 40 | — | ns | |

**Note 1:** Requires the use of Parameter #73A.

**2:** Only if Parameter #71A and #72A are used.

**FIGURE 27-23: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING**

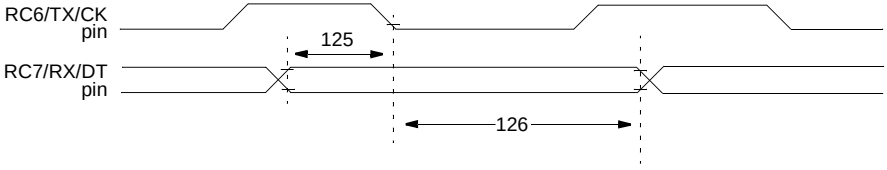



**Note:** Refer to Figure 27-5 for load conditions.

**TABLE 27-23: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS**

| Param. No. | Symbol | Characteristic | | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 120 | TCKH2DTV | SYNC XMIT (MASTER & SLAVE)<br>Clock High to Data Out Valid | PIC18FXX8X | — | 40 | ns | |
| | | | PIC18LFXX8X | — | 100 | ns | |
| 121 | TCKRF | Clock Out Rise Time and Fall Time (Master mode) | PIC18FXX8X | — | 20 | ns | |
| | | | PIC18LFXX8X | — | 50 | ns | |
| 122 | TDTRF | Data Out Rise Time and Fall Time | PIC18FXX8X | — | 20 | ns | |
| | | | PIC18LFXX8X | — | 50 | ns | |

**FIGURE 27-24: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING**




**Note:** Refer to Figure 27-5 for load conditions.

**TABLE 27-24: USART SYNCHRONOUS RECEIVE REQUIREMENTS**

| Param. No. | Symbol | Characteristic | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| 125 | TDTV2CKL | SYNC RCV (MASTER & SLAVE)<br>Data Hold before CK ↓ (DT hold time) | 10 | — | ns | |
| 126 | TCKL2DTL | Data Hold after CK ↓ (DT hold time) | 15 | — | ns | |

**TABLE 27-25: A/D CONVERTER CHARACTERISTICS: PIC18F6585/8585/6680/8680 (INDUSTRIAL, EXTENDED) PIC18LF6585/8585/6680/8680 (INDUSTRIAL)**

| Param No. | Symbol | Characteristic | | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| A01 | NR | Resolution | | — | — | 10 | bit | VREF = VDD ≥ 3.0V |
| | | | | — | — | TBD | bit | VREF = VDD < 3.0V |
| A03 | EIL | Integral Linearity Error | | — | — | <±1 | LSb | VREF = VDD ≥ 3.0V |
| | | | | — | — | TBD | LSb | VREF = VDD < 3.0V |
| A04 | EDL | Differential Linearity Error | | — | — | <±1 | LSb | VREF = VDD ≥ 3.0V |
| | | | | — | — | TBD | LSb | VREF = VDD < 3.0V |
| A05 | EFS | Full-Scale Error | | — | — | <±1 | LSb | VREF = VDD ≥ 3.0V |
| | | | | — | — | TBD | LSb | VREF = VDD < 3.0V |
| A06 | EOFF | Offset Error | | — | — | <±1 | LSb | VREF = VDD ≥ 3.0V |
| | | | | — | — | TBD | LSb | VREF = VDD < 3.0V |
| A10 | — | Monotonicity | | guaranteed(3) | | | — | VSS ≤ VAIN ≤ VREF |
| A20 | VREF | Reference Voltage (VREFH – VREFL) | | 0V | — | — | V | |
| A20A | | | | 3V | — | — | V | For 10-bit resolution |
| A21 | VREFH | Reference Voltage High | | AVss | — | AVDD + 0.3V | V | |
| A22 | VREFL | Reference Voltage Low | | AVss – 0.3V | — | AVDD | V | |
| A25 | VAIN | Analog Input Voltage | | AVSS – 0.3V | — | VREF + 0.3V | V | |
| A30 | ZAIN | Recommended Impedance of Analog Voltage Source | | — | — | 10.0 | kΩ | |
| A40 | IAD | A/D Conversion Current (VDD) | PIC18FXX8X | — | 180 | — | μA | Average current consumption when A/D is on **(Note 1)** |
| | | | PIC18LFXX8X | — | 90 | — | μA | |
| A50 | IREF | VREF Input Current **(Note 2)** | | — | — | 5 | μA | During VAIN acquisition. |
| | | | | — | — | 150 | μA | During A/D conversion cycle. |

**Note 1:** When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.
VREF current is from RA2/AN2/VREF- and RA3/AN3/VREF+ pins or AVDD and AVSS pins, whichever is selected as reference input.

**2:** VSS ≤ VAIN ≤ VREF

**3:** The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

**FIGURE 28-9: TYPICAL IDD vs. FOSC OVER VDD (EC MODE)**

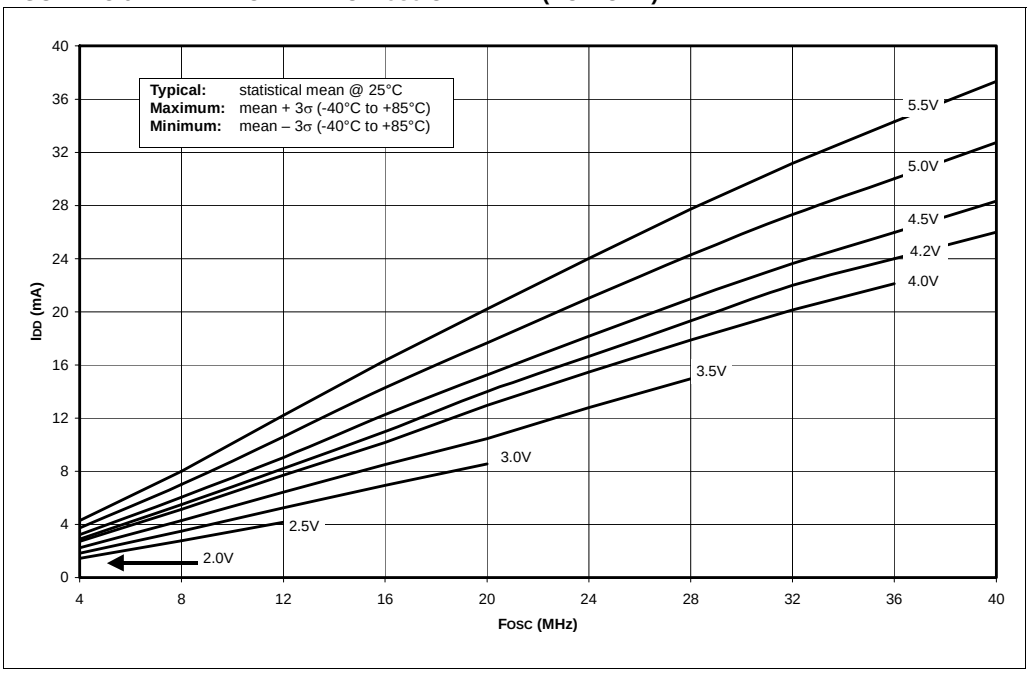
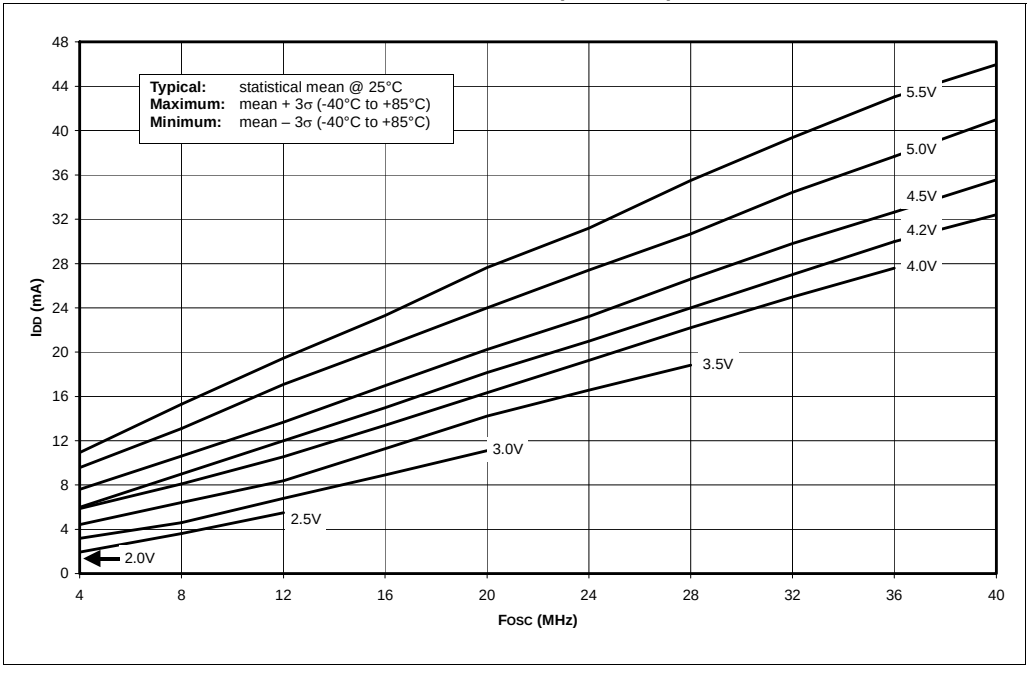



**FIGURE 28-10: MAXIMUM IDD vs. FOSC OVER VDD (EC MODE)**



**NOTES:**