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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	68
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f8680t-i-pt

PIC18F6585/8585/6680/8680

TABLE 4-2: SPECIAL FUNCTION REGISTER MAP (CONTINUED)

Address	Name	Address	Name	Address	Name	Address	Name
DDFh	—(1)	DDFh	—(1)	DBFh	—(1)	D9Fh	—(1)
DDEh	—(1)	DDEh	—(1)	DDEh	—(1)	D9Eh	—(1)
DDCh	—(1)	DDCh	—(1)	DBDh	—(1)	D9Dh	—(1)
DFCh	TXBIE	DDCh	—(1)	DBCh	—(1)	D9Ch	—(1)
DFBh	—(1)	DDCh	—(1)	DBBh	—(1)	D9Bh	—(1)
DFAh	BIE0	DDCh	—(1)	DBAh	—(1)	D9Ah	—(1)
DF9h	—(1)	DDCh	—(1)	DB9h	—(1)	D99h	—(1)
DF8h	BSEL0	DDCh	—(1)	DB8h	—(1)	D98h	—(1)
DF7h	—(1)	DDCh	—(1)	DB7h	—(1)	D97h	—(1)
DF6h	—(1)	DDCh	—(1)	DB6h	—(1)	D96h	—(1)
DF5h	—(1)	DDCh	—(1)	DB5h	—(1)	D95h	—(1)
DF4h	—(1)	DDCh	—(1)	DB4h	—(1)	D94h	—(1)
DF3h	MSEL3	DDCh	—(1)	DB3h	—(1)	D93h	RXF15EIDL
DF2h	MSEL2	DDCh	—(1)	DB2h	—(1)	D92h	RXF15EIDH
DF1h	MSEL1	DDCh	—(1)	DB1h	—(1)	D91h	RXF15SIDL
DF0h	MSEL0	DDCh	—(1)	DB0h	—(1)	D90h	RXF15SIDH
DEFh	—(1)	DDCh	—(1)	DAFh	—(1)	D8Fh	—(1)
DEEh	—(1)	DDCh	—(1)	DAEh	—(1)	D8Eh	—(1)
DEDh	—(1)	DDCh	—(1)	DADh	—(1)	D8Dh	—(1)
DECh	—(1)	DDCh	—(1)	DACH	—(1)	D8Ch	—(1)
DEBh	—(1)	DDCh	—(1)	DABh	—(1)	D8Bh	RXF14EIDL
DEAh	—(1)	DDCh	—(1)	DAAh	—(1)	D8Ah	RXF14EIDH
DE9h	—(1)	DDCh	—(1)	DA9h	—(1)	D89h	RXF14SIDL
DE8h	—(1)	DDCh	—(1)	DA8h	—(1)	D88h	RXF14SIDH
DE7h	RXFBCON7	DDCh	—(1)	DA7h	—(1)	D87h	RXF13EIDL
DE6h	RXFBCON6	DDCh	—(1)	DA6h	—(1)	D86h	RXF13EIDH
DE5h	RXFBCON5	DDCh	—(1)	DA5h	—(1)	D85h	RXF13SIDL
DE4h	RXFBCON4	DDCh	—(1)	DA4h	—(1)	D84h	RXF13SIDH
DE3h	RXFBCON3	DDCh	—(1)	DA3h	—(1)	D83h	RXF12EIDL
DE2h	RXFBCON2	DDCh	—(1)	DA2h	—(1)	D82h	RXF12EIDH
DE1h	RXFBCON1	DDCh	—(1)	DA1h	—(1)	D81h	RXF12SIDL
DE0h	RXFBCON0	DDCh	—(1)	DA0h	—(1)	D80h	RXF12SIDH

Note 1: Unimplemented registers are read as '0'.

2: This register is not available on PIC18F6X8X devices.

3: This is not a physical register.

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TABLE 4-3: REGISTER FILE SUMMARY (CONTINUED)

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:
RXF5SIDL	SID2	SID1	SID0	—	EXIDEN	—	EID17	EID16	xx-x x-xx	43, 230
RXF5SIDH	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	xxxx xxxx	43, 230
RXF4EIDL	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	xxxx xxxx	43, 230
RXF4EIDH	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	xxxx xxxx	43, 230
RXF4SIDL	SID2	SID1	SID0	—	EXIDEN	—	EID17	EID16	xx-x x-xx	43, 230
RXF4SIDH	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	xxxx xxxx	43, 230
RXF3EIDL	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	xxxx xxxx	43, 230
RXF3EIDH	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	xxxx xxxx	43, 230
RXF3SIDL	SID2	SID1	SID0	—	EXIDEN	—	EID17	EID16	xx-x x-xx	43, 230
RXF3SIDH	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	xxxx xxxx	43, 230
RXF2EIDL	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	xxxx xxxx	43, 230
RXF2EIDH	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	xxxx xxxx	43, 230
RXF2SIDL	SID2	SID1	SID0	—	EXIDEN	—	EID17	EID16	xx-x x-xx	43, 230
RXF2SIDH	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	xxxx xxxx	43, 230
RXF1EIDL	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	xxxx xxxx	43, 230
RXF1EIDH	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	xxxx xxxx	43, 230
RXF1SIDL	SID2	SID1	SID0	—	EXIDEN	—	EID17	EID16	xx-x x-xx	43, 230
RXF1SIDH	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	xxxx xxxx	43, 230
RXF0EIDL	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	xxxx xxxx	43, 230
RXF0EIDH	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	xxxx xxxx	43, 230
RXF0SIDL	SID2	SID1	SID0	—	EXIDEN	—	EID17	EID16	xx-x x-xx	43, 230
RXF0SIDH	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	xxxx xxxx	43, 230
B5D7 ⁽⁷⁾	B5D77	B5D76	B5D75	B5D74	B5D73	B5D72	B5D71	B5D70	xxxx xxxx	44, 230
B5D6 ⁽⁷⁾	B5D67	B5D66	B5D65	B5D64	B5D63	B5D62	B5D61	B5D60	xxxx xxxx	44, 230
B5D5 ⁽⁷⁾	B5D57	B5D56	B5D55	B5D54	B5D53	B5D52	B5D51	B5D50	xxxx xxxx	44, 230
B5D4 ⁽⁷⁾	B5D47	B5D46	B5D45	B5D44	B5D43	B5D42	B5D41	B5D40	xxxx xxxx	44, 230
B5D3 ⁽⁷⁾	B5D37	B5D36	B5D35	B5D34	B5D33	B5D32	B5D31	B5D30	xxxx xxxx	44, 230
B5D2 ⁽⁷⁾	B5D27	B5D26	B5D25	B5D24	B5D23	B5D22	B5D21	B5D20	xxxx xxxx	44, 230
B5D1 ⁽⁷⁾	B5D17	B5D16	B5D15	B5D14	B5D13	B5D12	B5D11	B5D10	xxxx xxxx	44, 230
B5D0 ⁽⁷⁾	B5D07	B5D06	B5D05	B5D04	B5D03	B5D02	B5D01	B5D00	xxxx xxxx	44, 230
B5DLC ⁽⁷⁾	—	RXRTR	RB1	RB0	DLC3	DLC2	DLC1	DLC0	-xxxx xxxx	44, 230
B5EIDL ⁽⁷⁾	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	xxxx xxxx	44, 230
B5EIDH ⁽⁷⁾	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	xxxx xxxx	44, 230
B5SIDL ⁽⁷⁾	SID2	SID1	SID0	SRR	EXID/ EXIDE ⁽⁵⁾	—	EID17	EID16	xxxx x-xx	44, 230
B5SIDH ⁽⁷⁾	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	xxxx xxxx	44, 230
B5CON ^(5, 7)	RXFUL/ TXBIF	RXM1/ TXABT	RTRRO/ TXLARB	FILHIT4/ TXERR	FILHIT3/ TXREQ	FILHIT2/ RTREN	FILHIT1/ TXPR1	FILHIT0/ TXPR0	0000 0000	44, 230
B4D7 ⁽⁷⁾	B4D77	B4D76	B4D75	B4D74	B4D73	B4D72	B4D71	B4D70	xxxx xxxx	44, 230
B4D6 ⁽⁷⁾	B4D67	B4D66	B4D65	B4D64	B4D63	B4D62	B4D61	B4D60	xxxx xxxx	44, 230
B4D5 ⁽⁷⁾	B4D57	B4D56	B4D55	B4D54	B4D53	B4D52	B4D51	B4D50	xxxx xxxx	44, 230
B4D4 ⁽⁷⁾	B4D47	B4D46	B4D45	B4D44	B4D43	B4D42	B4D41	B4D40	xxxx xxxx	44, 230

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition

- Note** 1: RA6 and associated bits are configured as port pins in RCIO and ECIO Oscillator mode only and read '0' in all other oscillator modes.
- 2: Bit 21 of the TBLPTRU allows access to the device configuration bits.
- 3: These registers are unused on PIC18F6X80 devices; always maintain these clear.
- 4: These bits have multiple functions depending on the CAN module mode selection.
- 5: Meaning of this register depends on whether this buffer is configured as transmit or receive.
- 6: RG5 is available as an input when MCLR is disabled.
- 7: This register reads all '0's until the ECAN module is set up in Mode 1 or Mode 2.

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REGISTER 9-3: INTCON3 REGISTER

R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INT2IP	INT1IP	INT3IE	INT2IE	INT1IE	INT3IF	INT2IF	INT1IF
bit 7						bit 0	

- bit 7 **INT2IP:** INT2 External Interrupt Priority bit
1 = High priority
0 = Low priority
- bit 6 **INT1IP:** INT1 External Interrupt Priority bit
1 = High priority
0 = Low priority
- bit 5 **INT3IE:** INT3 External Interrupt Enable bit
1 = Enables the INT3 external interrupt
0 = Disables the INT3 external interrupt
- bit 4 **INT2IE:** INT2 External Interrupt Enable bit
1 = Enables the INT2 external interrupt
0 = Disables the INT2 external interrupt
- bit 3 **INT1IE:** INT1 External Interrupt Enable bit
1 = Enables the INT1 external interrupt
0 = Disables the INT1 external interrupt
- bit 2 **INT3IF:** INT3 External Interrupt Flag bit
1 = The INT3 external interrupt occurred (must be cleared in software)
0 = The INT3 external interrupt did not occur
- bit 1 **INT2IF:** INT2 External Interrupt Flag bit
1 = The INT2 external interrupt occurred (must be cleared in software)
0 = The INT2 external interrupt did not occur
- bit 0 **INT1IF:** INT1 External Interrupt Flag bit
1 = The INT1 external interrupt occurred (must be cleared in software)
0 = The INT1 external interrupt did not occur

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

Note: Interrupt flag bits are set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. This feature allows for software polling.

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REGISTER 9-8: **PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2**

	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	CMIE	—	EEIE	BCLIE	LVDIE	TMR3IE	CCP2IE
bit 7								bit 0
bit 7	Unimplemented: Read as '0'							
bit 6	CMIE: Comparator Interrupt Enable bit							
	1 = Enables the comparator interrupt							
	0 = Disables the comparator interrupt							
bit 5	Unimplemented: Read as '0'							
bit 4	EEIE: Data EEPROM/Flash Write Operation Interrupt Enable bit							
	1 = Enables the write operation interrupt							
	0 = Disables the write operation interrupt							
bit 3	BCLIE: Bus Collision Interrupt Enable bit							
	1 = Enables the bus collision interrupt							
	0 = Disables the bus collision interrupt							
bit 2	LVDIE: Low-Voltage Detect Interrupt Enable bit							
	1 = Enables the Low-Voltage Detect interrupt							
	0 = Disables the Low-Voltage Detect interrupt							
bit 1	TMR3IE: TMR3 Overflow Interrupt Enable bit							
	1 = Enables the TMR3 overflow interrupt							
	0 = Disables the TMR3 overflow interrupt							
bit 0	CCP2IE: CCP2 Interrupt Enable bit							
	1 = Enables the CCP2 interrupt							
	0 = Disables the CCP2 interrupt							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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9.4 IPR Registers

The IPR registers contain the individual priority bits for the peripheral interrupts. Due to the number of peripheral interrupt sources, there are three Peripheral Interrupt Priority registers (IPR1, IPR2 and IPR3). The operation of the priority bits requires that the Interrupt Priority Enable (IPEN) bit be set.

REGISTER 9-10: IPR1: PERIPHERAL INTERRUPT PRIORITY REGISTER 1

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSIP	CCP1IP	TMR2IP	TMR1IP
bit 7							bit 0

bit 7 **PSPIP:** Parallel Slave Port Read/Write Interrupt Priority bit⁽¹⁾
1 = High priority
0 = Low priority

Note 1: Available in Microcontroller mode only.

bit 6 **ADIP:** A/D Converter Interrupt Priority bit
1 = High priority
0 = Low priority

bit 5 **RCIP:** USART Receive Interrupt Priority bit
1 = High priority
0 = Low priority

bit 4 **TXIP:** USART Transmit Interrupt Priority bit
1 = High priority
0 = Low priority

bit 3 **SSIP:** Master Synchronous Serial Port Interrupt Priority bit
1 = High priority
0 = Low priority

bit 2 **CCP1IP:** CCP1 Interrupt Priority bit
1 = High priority
0 = Low priority

bit 1 **TMR2IP:** TMR2 to PR2 Match Interrupt Priority bit
1 = High priority
0 = Low priority

bit 0 **TMR1IP:** TMR1 Overflow Interrupt Priority bit
1 = High priority
0 = Low priority

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

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FIGURE 10-11: PORTE BLOCK DIAGRAM IN I/O MODE

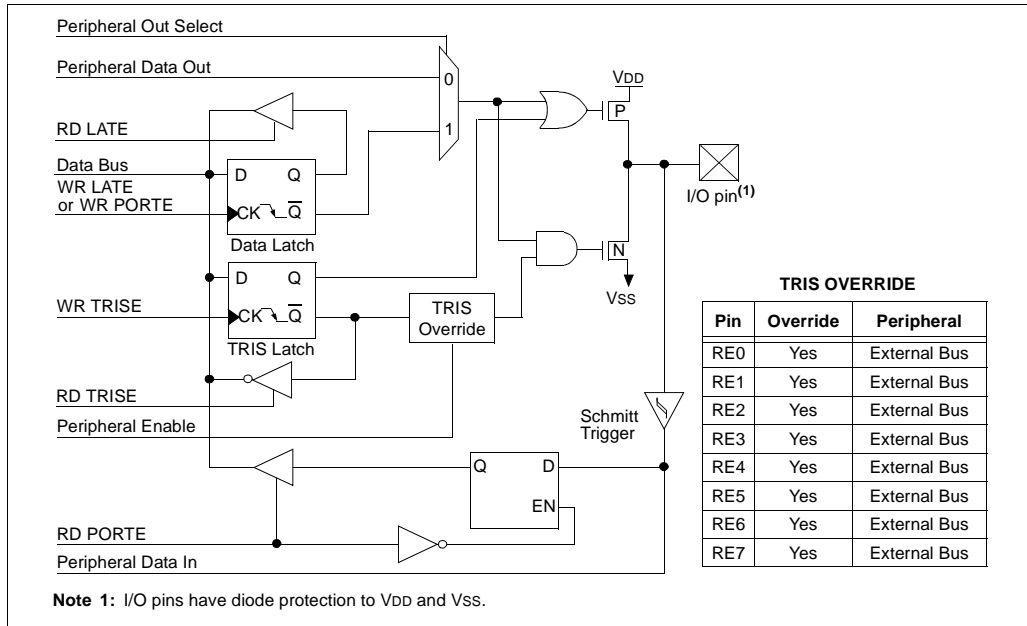
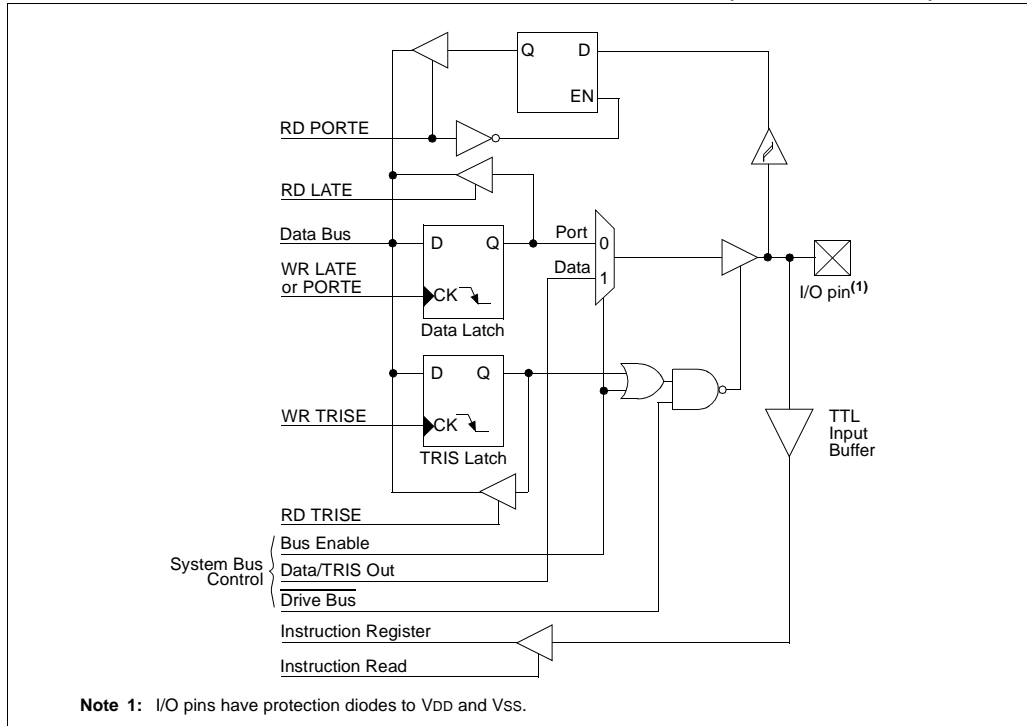


FIGURE 10-12: PORTE BLOCK DIAGRAM IN SYSTEM BUS MODE (PIC18F8X8X ONLY)



17.3.6 SLAVE MODE

In Slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched, the SSPIF interrupt flag bit is set.

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in Sleep mode, the slave can transmit/receive data. When a byte is received, the device will wake-up from Sleep.

17.3.7 SLAVE SELECT SYNCHRONIZATION

The \overline{SS} pin allows a Synchronous Slave mode. The SPI must be in Slave mode with \overline{SS} pin control enabled (SSPCON1<3:0> = 04h). The pin must not be driven low for the \overline{SS} pin to function as an input. The data latch must be high. When the \overline{SS} pin is low, transmission and reception are enabled and the SDO pin is driven. When

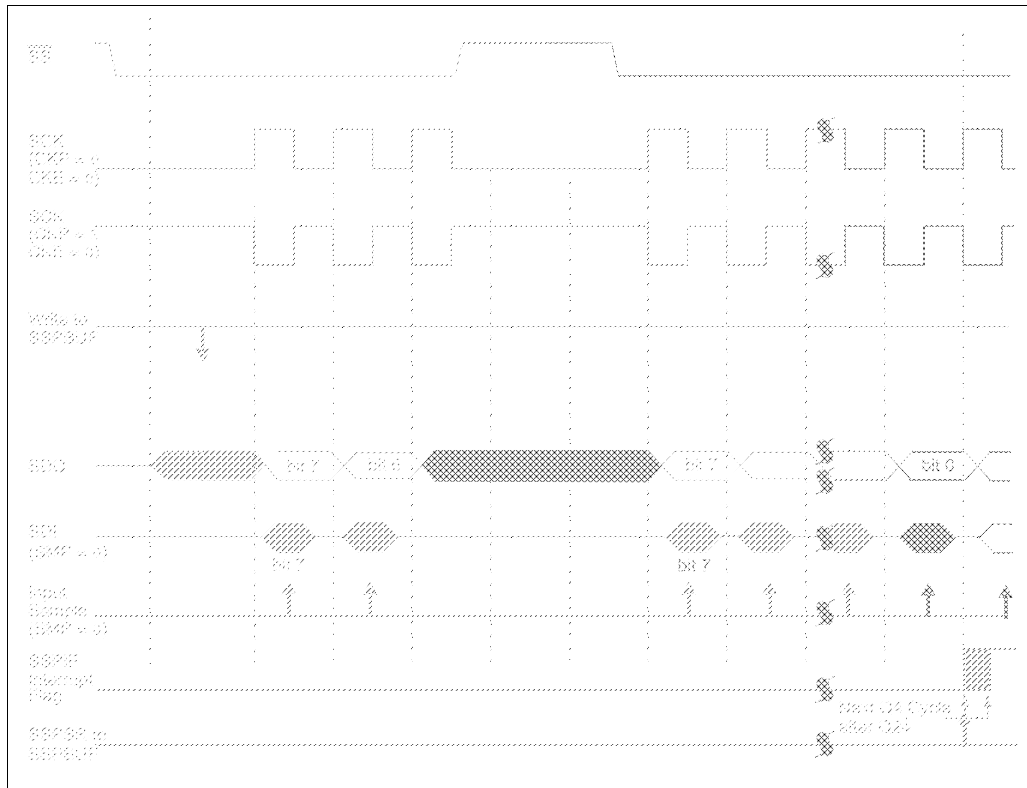
the \overline{SS} pin goes high, the SDO pin is no longer driven even if in the middle of a transmitted byte and becomes a floating output. External pull-up/pull-down resistors may be desirable depending on the application.

- Note 1:** When the SPI is in Slave mode with \overline{SS} pin control enabled (SSPCON1<3:0> = 0100), the SPI module will reset if the \overline{SS} pin is set to VDD.
- 2:** If the SPI is used in Slave mode with CKE set, then the \overline{SS} pin control must be enabled.

When the SPI module resets, the bit counter is forced to '0'. This can be done by either forcing the \overline{SS} pin to a high level or clearing the SSPEN bit.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver, the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function) since it cannot create a bus conflict.

FIGURE 17-4: SLAVE SYNCHRONIZATION WAVEFORM



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FIGURE 18-2: USART TRANSMIT BLOCK DIAGRAM

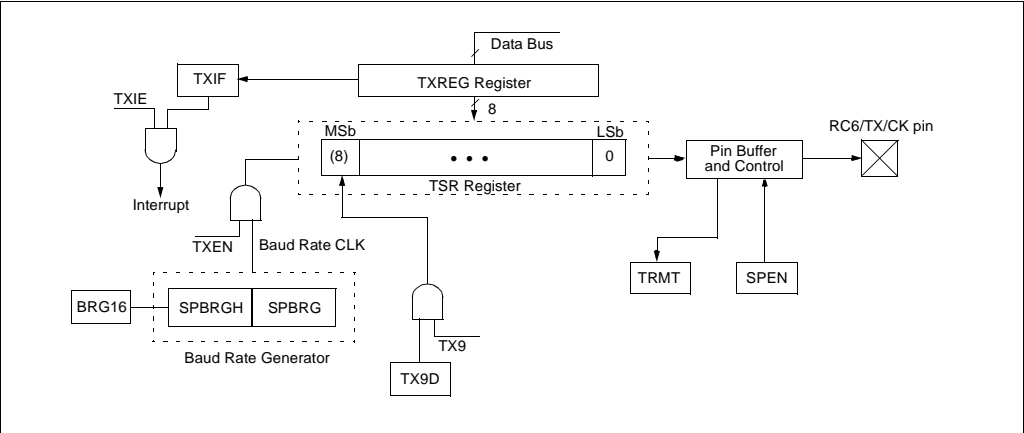


FIGURE 18-3: ASYNCHRONOUS TRANSMISSION

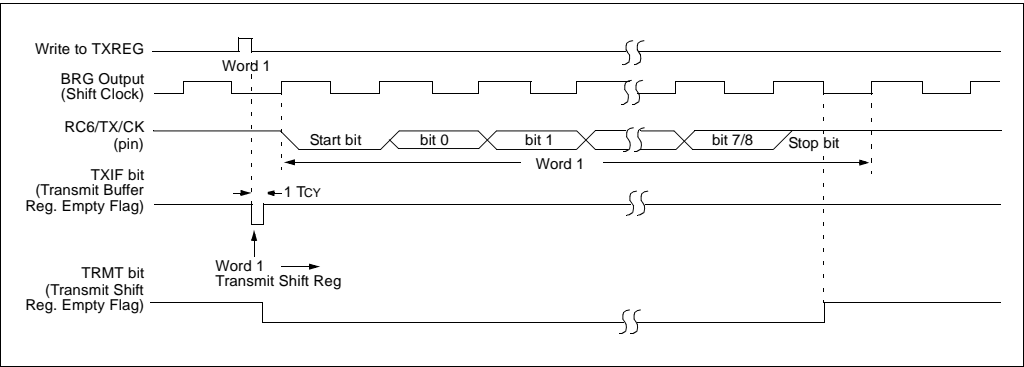
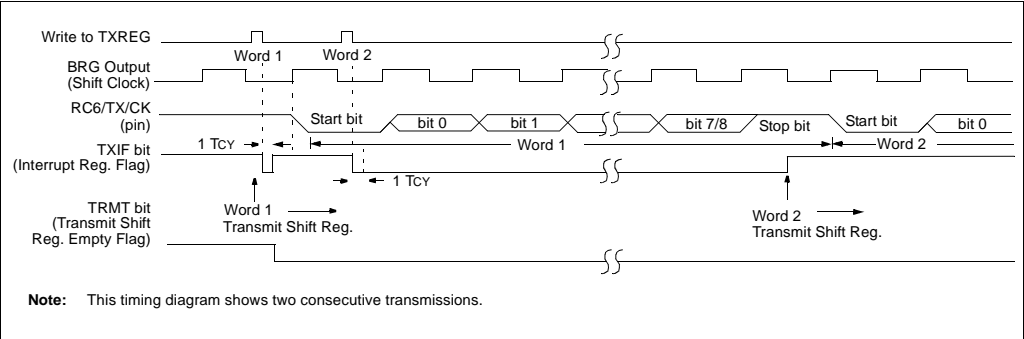


FIGURE 18-4: ASYNCHRONOUS TRANSMISSION (BACK TO BACK)



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REGISTER 23-20: RXBnDm: RECEIVE BUFFER n DATA FIELD BYTE m REGISTERS

[$0 \leq n \leq 1$, $0 \leq m \leq 7$]

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
RXBnDm7	RXBnDm6	RXBnDm5	RXBnDm4	RXBnDm3	RXBnDm2	RXBnDm1	RXBnDm0
bit 7							bit 0

bit 7-0 **RXBnDm7:RXBnDm0:** Receive Buffer n Data Field Byte m bits (where $0 \leq n < 1$ and $0 < m < 7$)
Each receive buffer has an array of registers. For example, Receive Buffer 0 has 8 registers: RXB0D0 to RXB0D7.

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
- n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 23-21: RXERRCNT: RECEIVE ERROR COUNT REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
REC7	REC6	REC5	REC4	REC3	REC2	REC1	REC0
bit 7							bit 0

bit 7-0 **REC7:REC0:** Receive Error Counter bits
This register contains the receive error value as defined by the CAN specifications.
When RXERRCNT > 127, the module will go into an error-passive state. RXERRCNT does not have the ability to put the module in "bus-off" state.

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
- n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

EXAMPLE 23-5: READING A CAN MESSAGE

```
; Need to read a pending message from RXB0 buffer.
; To receive any message, filter, mask and RXM1:RXM0 bits in RXB0CON registers must be
; programmed correctly.
;
; Make sure that there is a message pending in RXB0.
BTFSS  RXB0CON, RXFUL          ; Does RXB0 contain a message?
BRA    NoMessage              ; No. Handle this situation...
; We have verified that a message is pending in RXB0 buffer.
; If this buffer can receive both Standard or Extended Identifier messages,
; identify type of message received.
BTFSS  RXB0SIDL, EXID          ; Is this Extended Identifier?
BRA    StandardMessage        ; No. This is Standard Identifier message.
                                ; Yes. This is Extended Identifier message.
; Read all 29-bits of Extended Identifier message.
...
; Now read all data bytes
MOVFF  RXB0D0, MY_DATA_BYTE1
...
; Once entire message is read, mark the RXB0 that it is read and no longer FULL.
BCF    RXB0CON, RXFUL          ; This will allow CAN Module to load new messages
                                ; into this buffer.
...
```

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REGISTER 23-28: BnEIDH: TX/RX BUFFER n EXTENDED IDENTIFIER REGISTERS, HIGH BYTE IN RECEIVE MODE [$0 \leq n \leq 5$, TXnEN (BSEL0<n>) = 0]⁽¹⁾

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8

bit 7 bit 0

bit 7-0 **EID15:EID8:** Extended Identifier bits

Note 1: These registers are available in Mode 1 and 2 only.

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
- n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 23-29: BnEIDH: TX/RX BUFFER n EXTENDED IDENTIFIER REGISTERS, HIGH BYTE IN TRANSMIT MODE [$0 \leq n \leq 5$, TXnEN (BSEL0<n>) = 1]⁽¹⁾

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8

bit 7 bit 0

bit 7-0 **EID15:EID8:** Extended Identifier bits

Note 1: These registers are available in Mode 1 and 2 only.

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
- n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

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23.2.3.2 Message Acceptance Filters and Masks

This subsection describes the message acceptance filters and masks for the CAN receive buffers.

Note: These registers are writable in Configuration mode only.

REGISTER 23-37: RXFnSIDH: RECEIVE ACCEPTANCE FILTER n STANDARD IDENTIFIER FILTER REGISTERS, HIGH BYTE [0 ≤ n ≤ 15]⁽¹⁾

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3

bit 7

bit 0

bit 7-0

SID10:SID3: Standard Identifier Filter bits, if EXIDEN = 0;
Extended Identifier Filter bits EID28:EID21, if EXIDEN = 1.

Note 1: Registers RXF6SIDH:RXF15SIDH are available in Mode 1 and 2 only.

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
- n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 23-38: RXFnSIDL: RECEIVE ACCEPTANCE FILTER n STANDARD IDENTIFIER FILTER REGISTERS, LOW BYTE [0 ≤ n ≤ 15]⁽¹⁾

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	EXIDEN	—	EID17	EID16

bit 7

bit 0

bit 7-5

SID2:SID0: Standard Identifier Filter bits, if EXIDEN = 0;
Extended Identifier Filter bits EID20:EID18, if EXIDEN = 1.

bit 4

Unimplemented: Read as '0'

bit 3

EXIDEN: Extended Identifier Filter Enable bit

1 = Filter will only accept extended ID messages

0 = Filter will only accept standard ID messages

Note: In Mode 0, this bit must be set/cleared as required, irrespective of corresponding mask register value.

bit 2

Unimplemented: Read as '0'

bit 1-0

EID17:EID16: Extended Identifier Filter bits

Note 1: Registers RXF6SIDL:RXF15SIDL are available in Mode 1 and 2 only.

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
- n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

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REGISTER 23-57: PIE3: PERIPHERAL INTERRUPT ENABLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRXIE	WAKIE	ERRIE	TXB2IE/ TXBnIE	TXB1IE ⁽¹⁾	TXB0IE ⁽¹⁾	RXB1IE/ RXBnIE	RXB0IE/ FIFOWMIE

bit 7

bit 0

- bit 7 **IRXIE:** CAN Invalid Received Message Interrupt Enable bit
 1 = Enable invalid message received interrupt
 0 = Disable invalid message received interrupt
- bit 6 **WAKIE:** CAN bus Activity Wake-up Interrupt Enable bit
 1 = Enable bus activity wake-up interrupt
 0 = Disable bus activity wake-up interrupt
- bit 5 **ERRIE:** CAN bus Error Interrupt Enable bit
 1 = Enable CAN bus error interrupt
 0 = Disable CAN bus error interrupt
- bit 4 When CAN is in Mode 0:
TXB2IE: CAN Transmit Buffer 2 Interrupt Enable bit
 1 = Enable Transmit Buffer 2 interrupt
 0 = Disable Transmit Buffer 2 interrupt
When CAN is in Mode 1 or 2:
TXBnIE: CAN Transmit Buffer Interrupts Enable bit
 1 = Enable transmit buffer interrupt; individual interrupt is enabled by TXBIE and BIE0
 0 = Disable all transmit buffer interrupts
- bit 3 **TXB1IE:** CAN Transmit Buffer 1 Interrupt Enable bit⁽¹⁾
 1 = Enable Transmit Buffer 1 interrupt
 0 = Disable Transmit Buffer 1 interrupt
- bit 2 **TXB0IE:** CAN Transmit Buffer 0 Interrupt Enable bit⁽¹⁾
 1 = Enable Transmit Buffer 0 interrupt
 0 = Disable Transmit Buffer 0 interrupt
- bit 1 When CAN is in Mode 0:
RXB1IE: CAN Receive Buffer 1 Interrupt Enable bit
 1 = Enable Receive Buffer 1 interrupt
 0 = Disable Receive Buffer 1 interrupt
When CAN is in Mode 1 or 2:
RXBnIE: CAN Receive Buffer Interrupts Enable bit
 1 = Enable receive buffer interrupt; individual interrupt is enabled by BIE0
 0 = Disable all receive buffer interrupts
- bit 0 When CAN is in Mode 0:
RXB0IE: CAN Receive Buffer 0 Interrupt Enable bit
 1 = Enable Receive Buffer 0 interrupt
 0 = Disable Receive Buffer 0 interrupt
When CAN is in Mode 1:
Unimplemented: Read as '0'
When CAN is in Mode 2:
FIFOWMIE: FIFO Watermark Interrupt Enable bit
 1 = Enable FIFO watermark interrupt
 0 = Disable FIFO watermark interrupt

Note 1: In CAN Mode 1 and 2, this bit is forced to '0'.

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

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24.4.1 PROGRAM MEMORY CODE PROTECTION

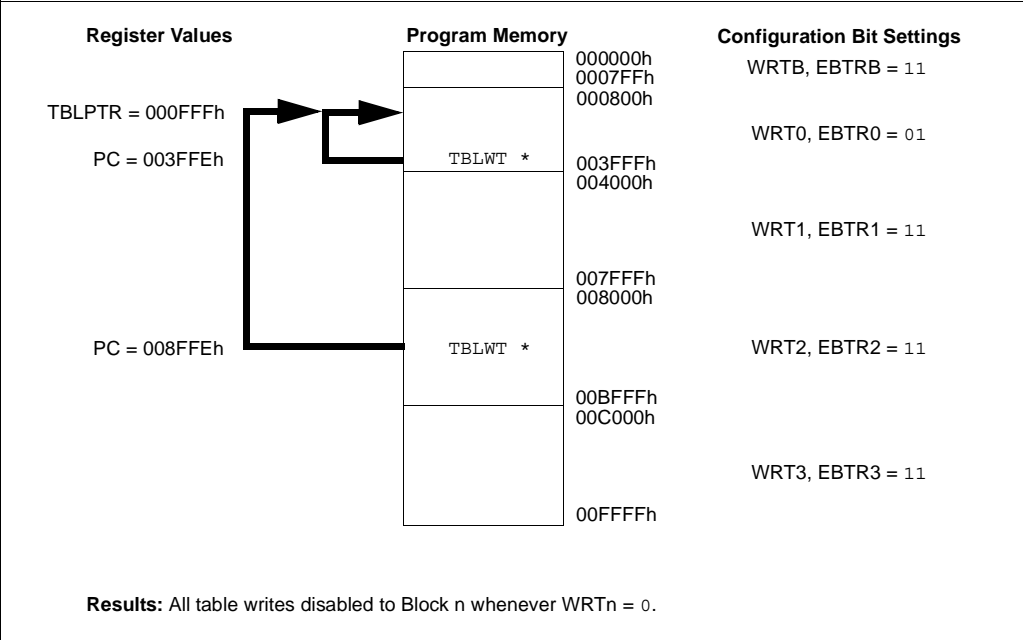
The user memory may be read to or written from any location using the table read and table write instructions. The device ID may be read with table reads. The Configuration registers may be read and written with the table read and table write instructions.

In User mode, the CPn bits have no direct effect. CPn bits inhibit external reads and writes. A block of user memory may be protected from table writes if the WRTn configuration bit is '0'. The EBTRn bits control table reads. For a block of user memory with the EBTRn bit set to '0', a table read instruction that executes from within that block is allowed to read. A table read instruction that executes from a location outside of

that block is not allowed to read and will result in reading '0's. Figures 24-4 through 24-6 illustrate table write and table read protection.

Note: Code protection bits may only be written to a '0' from a '1' state. It is not possible to write a '1' to a bit in the '0' state. Code protection bits are only set to '1' by a full chip erase or block erase function. The full chip erase and block erase functions can only be initiated via ICSP or an external programmer.

FIGURE 24-4: TABLE WRITE (WRTn) DISALLOWED



24.4.2 DATA EEPROM CODE PROTECTION

The entire data EEPROM is protected from external reads and writes by two bits: CPD and WRTD. CPD inhibits external reads and writes of data EEPROM. WRTD inhibits external writes to data EEPROM. The CPU can continue to read and write data EEPROM regardless of the protection bit settings.

24.4.3 CONFIGURATION REGISTER PROTECTION

The Configuration registers can be write-protected. The WRTC bit controls protection of the Configuration registers. In User mode, the WRTC bit is readable only. WRTC can only be written via ICSP or an external programmer.

24.5 ID Locations

Eight memory locations (200000h-200007h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are accessible during normal execution through the TBLRD and TBLWT instructions or during program/verify. The ID locations can be read when the device is code-protected.

24.6 In-Circuit Serial Programming

PIC18FXX80/XX85 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

24.7 In-Circuit Debugger

When the DEBUG bit in Configuration register, CONFIG4L, is programmed to a '0', the in-circuit debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB® IDE. When the microcontroller has this feature enabled, some of the resources are not available for general use. Table 24-4 shows which features are consumed by the background debugger.

TABLE 24-4: DEBUGGER RESOURCES

I/O pins	RB6, RB7
Stack	2 levels
Program Memory	512 bytes
Data Memory	10 bytes

To use the in-circuit debugger function of the microcontroller, the design must implement In-Circuit Serial Programming connections to MCLR/VPP, VDD, GND, RB7 and RB6. This will interface to the in-circuit debugger module available from Microchip or one of the third party development tool companies.

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RRNCF Rotate Right f (no carry)

Syntax: [*label*] RRNCF f [,d [,a]]

Operands: $0 \leq f \leq 255$

$d \in [0,1]$

$a \in [0,1]$

Operation: $(f \ll n) \rightarrow \text{dest} \ll n-1$,
 $(f \ll 0) \rightarrow \text{dest} \ll 7$

Status Affected: N, Z

Encoding:

0100	00da	ffff	ffff
------	------	------	------

Description: The contents of register 'f' are rotated one bit to the right. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f' (default). If 'a' is '0', the Access Bank will be selected, overriding the BSR value. If 'a' is '1', then the bank will be selected as per the BSR value (default).



Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example 1: RRNCF REG, 1, 0

Before Instruction

REG = 1101 0111

After Instruction

REG = 1110 1011

Example 2: RRNCF REG, 0, 0

Before Instruction

W = ?

REG = 1101 0111

After Instruction

W = 1110 1011

REG = 1101 0111

SETF Set f

Syntax: [*label*] SETF f [,a]

Operands: $0 \leq f \leq 255$

$a \in [0,1]$

Operation: FFh \rightarrow f

Status Affected: None

Encoding:

0110	100a	ffff	ffff
------	------	------	------

Description: The contents of the specified register are set to FFh. If 'a' is '0', the Access Bank will be selected, overriding the BSR value. If 'a' is '1', then the bank will be selected as per the BSR value (default).

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write register 'f'

Example: SETF REG, 1

Before Instruction

REG = 0x5A

After Instruction

REG = 0xFF

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SLEEP Enter Sleep mode

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT postscaler,
1 → \overline{TO} ,
0 → PD

Status Affected: \overline{TO} , PD

Encoding:

0000	0000	0000	0011
------	------	------	------

Description: The Power-down status bit (PD) is cleared. The Time-out status bit (\overline{TO}) is set. Watchdog Timer and its postscaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	Process Data	Go to SLEEP

Example: SLEEP

Before Instruction

\overline{TO} = ?
PD = ?

After Instruction

\overline{TO} = 1†
PD = 0

† If WDT causes wake-up, this bit is cleared.

SUBFWP Subtract f from W with borrow

Syntax: [*label*] SUBFWB f [,d [,a]]

Operands: $0 \leq f \leq 255$

$d \in [0,1]$

$a \in [0,1]$

Operation: $(W) - (f) - (\overline{C}) \rightarrow \text{dest}$

Status Affected: N, OV, C, DC, Z

Encoding:

0101	01da	ffff	ffff
------	------	------	------

Description: Subtract register 'f' and carry flag (borrow) from W (2's complement method). If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored in register 'f' (default). If 'a' is '0', the Access Bank will be selected, overriding the BSR value. If 'a' is '1', then the bank will be selected as per the BSR value (default).

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example 1: SUBFWB REG, 1, 0

Before Instruction

REG = 3
W = 2
C = 1

After Instruction

REG = FF
W = 2
C = 0
Z = 0
N = 1 ; result is negative

Example 2: SUBFWB REG, 0, 0

Before Instruction

REG = 2
W = 5
C = 1

After Instruction

REG = 2
W = 3
C = 1
Z = 0
N = 0 ; result is positive

Example 3: SUBFWB REG, 1, 0

Before Instruction

REG = 1
W = 2
C = 0

After Instruction

REG = 0
W = 2
C = 1
Z = 1
N = 0 ; result is zero

27.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

Ambient temperature under bias.....	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to V _{SS} (except V _{DD} , $\overline{\text{MCLR}}$, and RA4)	-0.3V to (V _{DD} + 0.3V)
Voltage on V _{DD} with respect to V _{SS}	-0.3V to +5.5V
Voltage on $\overline{\text{MCLR}}$ with respect to V _{SS} (Note 2)	0V to +13.25V
Voltage on RA4 with respect to V _{SS}	0V to +8.5V
Total power dissipation (Note 1)	1.0W
Maximum current out of V _{SS} pin	300 mA
Maximum current into V _{DD} pin	250 mA
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD})	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD})	±20 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports	200 mA

Note 1: Power dissipation is calculated as follows:

$$P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$$

- 2:** Voltage spikes below V_{SS} at the $\overline{\text{MCLR}}$ /V_{PP} pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a “low” level to the $\overline{\text{MCLR}}$ /V_{PP} pin rather than pulling this pin directly to V_{SS}.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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FIGURE 28-5: TYPICAL I_{DD} vs. F_{OSC} OVER V_{DD} (XT MODE)

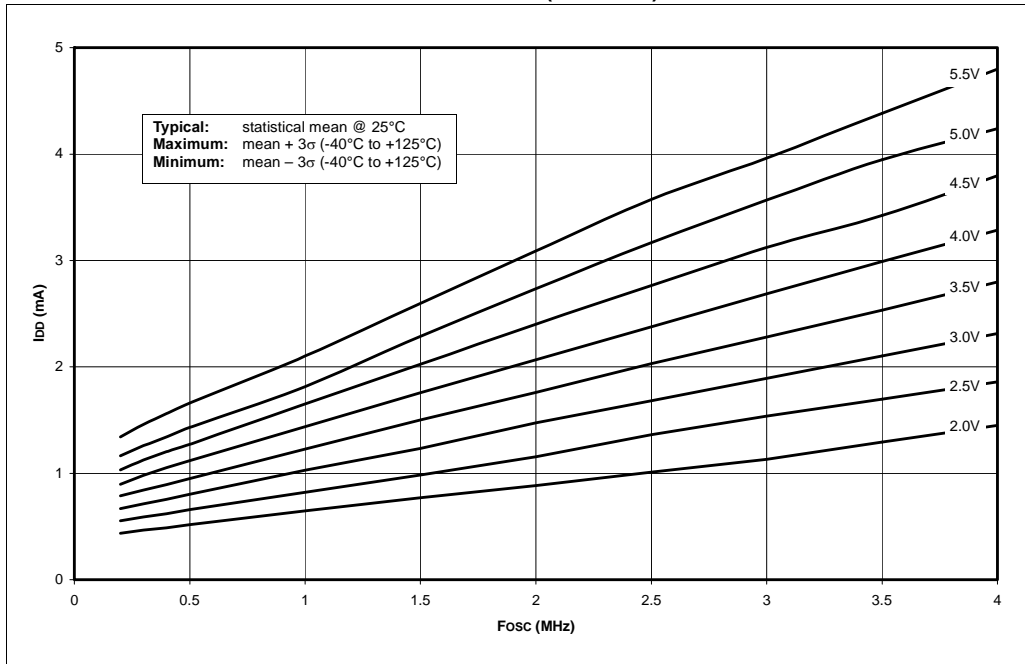
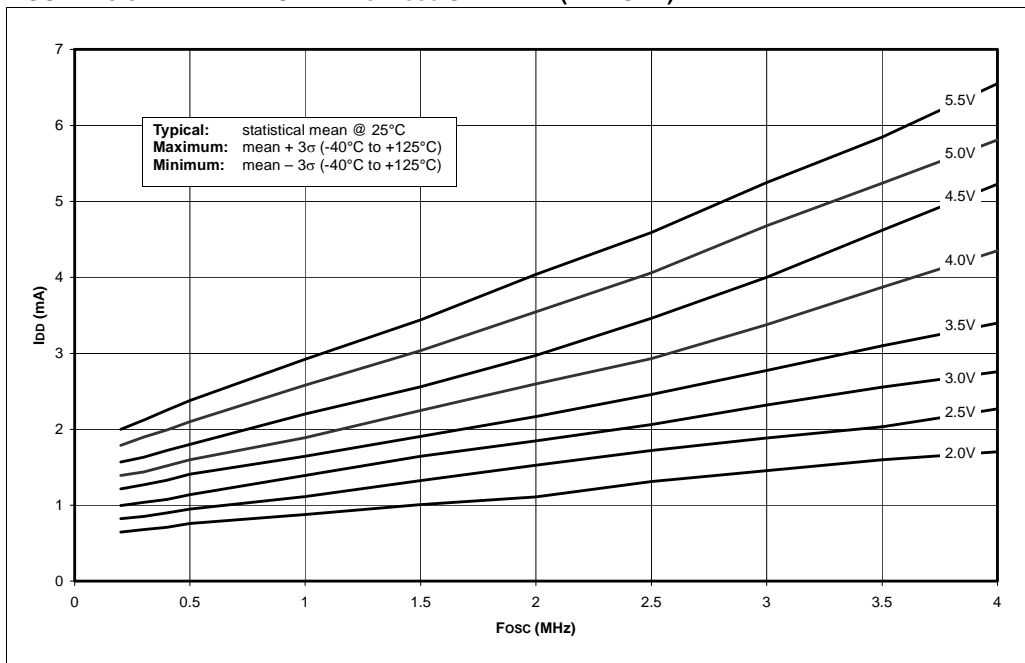


FIGURE 28-6: MAXIMUM I_{DD} vs. F_{OSC} OVER V_{DD} (XT MODE)



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APPENDIX A: REVISION HISTORY

Revision A (February 2003)

Original data sheet for PIC18F6585/8585/6680/8680 family.

Revision B (June 2003)

This revision includes updates to the Special Function Registers in Table 4-2 and Table 23-1 and minor corrections to the data sheet text.

Revision C (February 2004)

This revision includes the DC and AC Characteristics Graphs and Tables. The Electrical Specifications in **Section 27.0 "Electrical Characteristics"** have been updated and there have been minor corrections to the data sheet text.

Revision D (January 2013)

Added a note to each package outline drawing.

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

TABLE B-1: DEVICE DIFFERENCES

Feature	PIC18F6585	PIC18F6680	PIC18F8585	PIC18F8680
On-Chip Program Memory (Kbytes)	48	64	48	64
I/O Ports	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G, H, J	Ports A, B, C, D, E, F, G, H, J
A/D Channels	12	12	16	16
External Memory Interface	No	No	Yes	Yes
Package Types	64-pin TQFP, 68-pin PLCC	64-pin TQFP, 68-pin PLCC	80-pin TQFP	80-pin TQFP

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