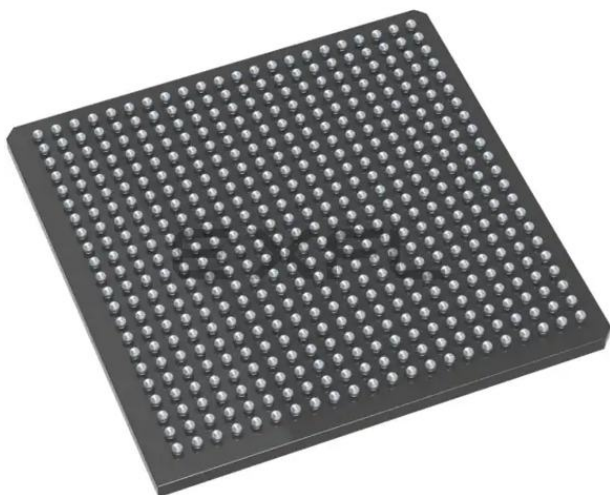




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	75264
Total RAM Bits	516096
Number of I/O	341
Number of Gates	3000000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agle3000v2-fg484i

Calculating Power Dissipation

Quiescent Supply Current

Quiescent supply current (IDD) calculation depends on multiple factors, including operating voltages (VCC, VCCI, and VJTAG), operating temperature, system clock frequency, and power modes usage. Microsemi recommends using the PowerCalculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

Table 2-8 • Power Supply State per Mode

	Power Supply Configurations				
Modes/power supplies	VCC	VCCPLL	VCCI	VJTAG	VPUMP
Flash*Freeze	On	On	On	On	On/off/floating
Sleep	Off	Off	On	Off	Off
Shutdown	Off	Off	Off	Off	Off
No Flash*Freeze	On	On	On	On	On/off/floating

Note: Off: Power supply level = 0 V

Table 2-9 • Quiescent Supply Current (IDD), IGLOOe Flash*Freeze Mode*

	Core Voltage	AGLE600	AGLE3000	Units
Typical (25°C)	1.2 V	34	95	μA
	1.5 V	72	310	μA

Note: *IDD includes VCC, VPUMP, VCCI, VCCPLL, and VMV currents. Values do not include I/O static contribution, which is shown in [Table 2-13 on page 2-9](#) and [Table 2-14 on page 2-10](#) (PDC6 and PDC7).

Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOOe Sleep Mode*

	Core Voltage	AGLE600	AGLE3000	Units
VCCI/VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	μA
VCCI/VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	μA
VCCI/VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	μA
VCCI/VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	μA
VCCI/VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	μA

Note: *IDD = $N_{BANKS} \times ICCI$. Values do not include I/O static contribution, which is shown in [Table 2-13 on page 2-9](#) and [Table 2-14 on page 2-10](#) (PDC6 and PDC7).

Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOOe Shutdown Mode*

	Core Voltage	AGLE600	AGLE3000	Units
Typical (25°C)	1.2 V / 1.5 V	0	0	μA

Table 2-12 • Quiescent Supply Current (IDD) Characteristics, No Flash*Freeze Mode¹

	Core Voltage	AGLE600	AGLE3000	Units
ICCA Current²				
Typical (25°C)	1.2 V	28	89	μA
	1.5 V	82	320	μA
ICCI or IJTAG Current³				
VCCI/VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	μA
VCCI/VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	μA
VCCI/VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	μA
VCCI/VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	μA
VCCI/VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	μA

Notes:

1. $IDD = N_{BANKS} \times ICCI + ICCA$. JTAG counts as one bank when powered.
2. Includes VCC and VPUMP and VCCPLL currents.
3. Values do not include I/O static contribution (PDC6 and PDC7).

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
 - Bit 0 (LSB) = 100%
 - Bit 1 = 50%
 - Bit 2 = 25%
 - ...
 - Bit 7 (MSB) = 0.78125%
 - Average toggle rate = $(100\% + 50\% + 25\% + 12.5\% + \dots + 0.78125\%) / 8$

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-19 • Toggle Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-20 • Enable Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels
Applicable to Commercial and Industrial Conditions

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength ²	Slew Rate	VIL		VIH		VOL	VOH	IOL ¹	IOH ¹
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTTL / 3.3 V LVC MOS	12 mA	12 mA	High	−0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVC MOS Wide Range ³	100 µA	12 mA	High	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	0.1	0.1
2.5 V LVC MOS	12 mA	12 mA	High	−0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVC MOS	12 mA	12 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	12	12
1.5 V LVC MOS	12 mA	12 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12
1.2 V LVC MOS	2 mA	2 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVC MOS Wide Range ⁴	100 µA	2 mA	High	−0.3	0.3 * VCCI	0.7 * VCCI	3.6	0.1	VCCI − 0.1	0.1	0.1
3.3 V PCI	Per PCI Specification										
3.3 V PCI-X	Per PCI-X Specification										
3.3 V GTL	20 mA ⁵	20 mA ⁵	High	−0.3	VREF − 0.05	VREF + 0.05	3.6	0.4	–	20	20
2.5 V GTL	20 mA ⁵	20 mA ⁵	High	−0.3	VREF − 0.05	VREF + 0.05	3.6	0.4	–	20	20
3.3 V GTL+	35 mA	35 mA	High	−0.3	VREF − 0.1	VREF + 0.1	3.6	0.6	–	35	35
2.5 V GTL+	33 mA	33 mA	High	−0.3	VREF − 0.1	VREF + 0.1	3.6	0.6	–	33	33
HSTL (I)	8 mA	8 mA	High	−0.3	VREF − 0.1	VREF + 0.1	3.6	0.4	VCCI − 0.4	8	8

Notes:

1. Currents are measured at 85°C junction temperature.
2. The minimum drive strength for any LVC MOS 1.2 V or LVC MOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
3. All LVC MOS 3.3 V software macros support LVC MOS 3.3 V wide range as specified in the JESD8-12 specification.
4. All LVC MOS 1.2 V software macros support LVC MOS 1.2 V wide range as specified in the JESD8-12 specification.
5. Output drive strength is below JEDEC specification.
6. Output Slew Rates can be extracted from IBIS Models, <http://www.microsemi.com/soc/download/ibis/default.aspx>.

Single-Ended I/O Characteristics

3.3 V LVTTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer. The 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTTL support.

Table 2-34 • Minimum and Maximum DC Input and Output Levels

3.3 V LVTTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	−0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	−0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	10	10
24 mA	−0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

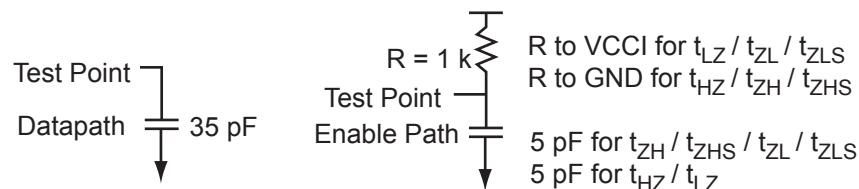


Figure 2-7 • AC Loading

Table 2-35 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	3.3	1.4	–	5

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

1.2 V DC Core Voltage

Table 2-50 • 2.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.55	6.25	0.26	1.55	1.77	1.10	6.36	5.34	2.81	2.63	12.14	11.13	ns
8 mA	Std.	1.55	5.18	0.26	1.55	1.77	1.10	5.26	4.61	3.13	3.32	11.05	10.39	ns
12 mA	Std.	1.55	4.42	0.26	1.55	1.77	1.10	4.49	4.08	3.36	3.76	10.28	9.86	ns
16 mA	Std.	1.55	4.19	0.26	1.55	1.77	1.10	4.25	3.96	3.40	3.89	10.04	9.75	ns
24 mA	Std.	1.55	4.09	0.26	1.55	1.76	1.10	4.15	3.97	3.47	4.32	9.94	9.76	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-51 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.55	3.38	0.26	1.55	1.77	1.10	3.42	3.11	2.81	2.72	9.21	8.89	ns
8 mA	Std.	1.55	2.83	0.26	1.55	1.77	1.10	2.87	2.51	3.13	3.42	8.66	8.30	ns
12 mA	Std.	1.55	2.51	0.26	1.55	1.77	1.10	2.54	2.22	3.36	3.85	8.33	8.00	ns
16 mA	Std.	1.55	2.45	0.26	1.55	1.77	1.10	2.48	2.16	3.40	3.97	8.27	7.95	ns
24 mA	Std.	1.55	2.46	0.26	1.55	1.77	1.10	2.49	2.09	3.47	4.44	8.28	7.88	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

1.2 V DC Core Voltage

Table 2-56 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	8.21	0.26	1.53	1.96	1.10	8.35	6.88	2.87	1.70	14.14	12.67	ns
4 mA	Std.	1.55	6.83	0.26	1.53	1.96	1.10	6.94	5.88	3.27	3.18	12.73	11.67	ns
6 mA	Std.	1.55	5.85	0.26	1.53	1.96	1.10	5.94	5.19	3.53	3.37	11.73	10.98	ns
8 mA	Std.	1.55	5.52	0.26	1.53	1.96	1.10	5.61	5.06	3.59	3.88	11.39	10.84	ns
12 mA	Std.	1.55	5.42	0.26	1.53	1.96	1.10	5.51	5.06	3.68	4.44	11.30	10.85	ns
16 mA	Std.	1.55	5.42	0.26	1.53	1.96	1.10	5.51	5.06	3.68	4.44	11.30	10.85	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-57 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.82	0.26	1.53	1.96	1.10	3.98	3.87	2.86	1.72	9.76	9.66	ns
4 mA	Std.	1.55	3.25	0.26	1.53	1.96	1.10	3.30	3.01	3.26	3.26	9.08	8.79	ns
6 mA	Std.	1.55	2.84	0.26	1.53	1.96	1.10	2.88	2.58	3.53	3.81	8.66	8.37	ns
8 mA	Std.	1.55	2.76	0.26	1.53	1.96	1.10	2.80	2.50	3.58	3.97	8.58	8.29	ns
12 mA	Std.	1.55	2.75	0.26	1.53	1.96	1.10	2.78	2.40	3.68	4.56	8.57	8.19	ns
16 mA	Std.	1.55	2.75	0.26	1.53	1.96	1.10	2.78	2.40	3.68	4.56	8.57	8.19	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

1.2 V DC Core Voltage

Table 2-62 • 1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	8.53	0.26	1.72	2.16	1.10	8.67	7.05	3.39	3.09	14.46	12.83	ns
4 mA	Std.	1.55	7.34	0.26	1.72	2.16	1.10	7.46	6.22	3.70	3.73	13.25	12.01	ns
6 mA	Std.	1.55	6.91	0.26	1.72	2.16	1.10	7.03	6.07	3.77	3.90	12.82	11.85	ns
8 mA	Std.	1.55	6.83	0.26	1.72	2.16	1.10	6.94	6.07	2.91	4.54	12.73	11.86	ns
12 mA	Std.	1.55	6.83	0.26	1.72	2.16	1.10	6.94	6.07	2.91	4.54	12.73	11.86	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-63 • 1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.72	0.26	1.72	2.16	1.10	3.78	3.45	3.38	3.19	9.56	9.24	ns
4 mA	Std.	1.55	3.23	0.26	1.72	2.16	1.10	3.27	2.92	3.69	3.83	9.06	8.71	ns
6 mA	Std.	1.55	3.13	0.26	1.72	2.16	1.10	3.18	2.82	3.76	4.01	8.96	8.61	ns
8 mA	Std.	1.55	3.10	0.26	1.72	2.16	1.10	3.15	2.70	3.86	4.68	8.93	8.49	ns
12 mA	Std.	1.55	3.10	0.26	1.72	2.16	1.10	3.15	2.70	3.86	4.68	8.93	8.49	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Timing Characteristics

1.2 V DC Core Voltage

Table 2-66 • 1.2 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 1.14\text{ V}$

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	9.92	0.26	2.09	2.95	1.10	9.53	7.48	4.02	3.67	15.31	13.26	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-67 • 1.2 LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 1.14\text{ V}$

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	4.06	0.26	2.09	2.95	1.10	3.92	3.46	4.01	3.79	9.71	9.24	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

1.2 V LVCMOS Wide Range

Table 2-68 • Minimum and Maximum DC Input and Output Levels

1.2 V LVCMOS Wide Range ¹		VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ²	IIH ³
Drive Strength	Equivalent Software Default Drive Strength Option ⁴	Min. (V)	Max. (V)	Min. (V)	Max (V)	Max. (V)	Min. (V)	μA	μA	Max. (mA) ⁵	Max. (mA) ⁵	μA ⁶	μA ⁶
100 μA	2 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	$0.25 * V_{CCI}$	$0.75 * V_{CCI}$	100	100	20	26	10	10

Notes:

1. Applicable to V2 devices ONLY.
2. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
3. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
4. The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
5. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
6. Currents are measured at 85°C junction temperature.
7. Software default selection highlighted in gray.

Timing Characteristics

Refer to LVCMOS 1.2 V (normal range) "Timing Characteristics" on [page 2-48](#) for worst-case timing.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-75 • 3.3 V GTL – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CCI} = 3.0\text{ V}$ $V_{REF} = 0.8\text{ V}$

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	1.83	0.19	2.41	0.67	1.84	1.83			5.47	5.46	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

1.2 V DC Core Voltage

Table 2-76 • 3.3 V GTL – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$,
Worst-Case $V_{CCI} = 3.0\text{ V}$ $V_{REF} = 0.8\text{ V}$

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.09	0.26	2.75	1.10	2.10	2.09			7.91	7.89	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

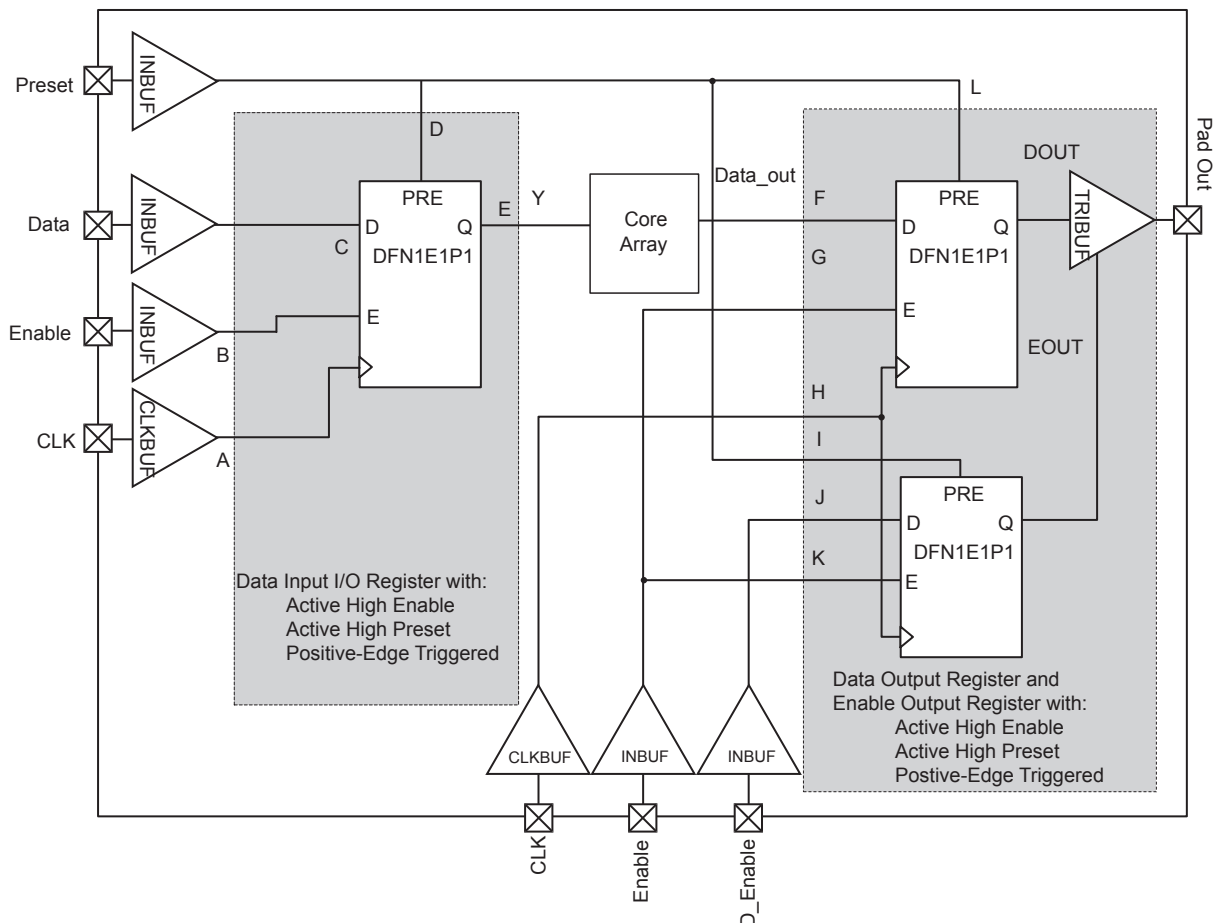


Figure 2-26 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Output Enable Register

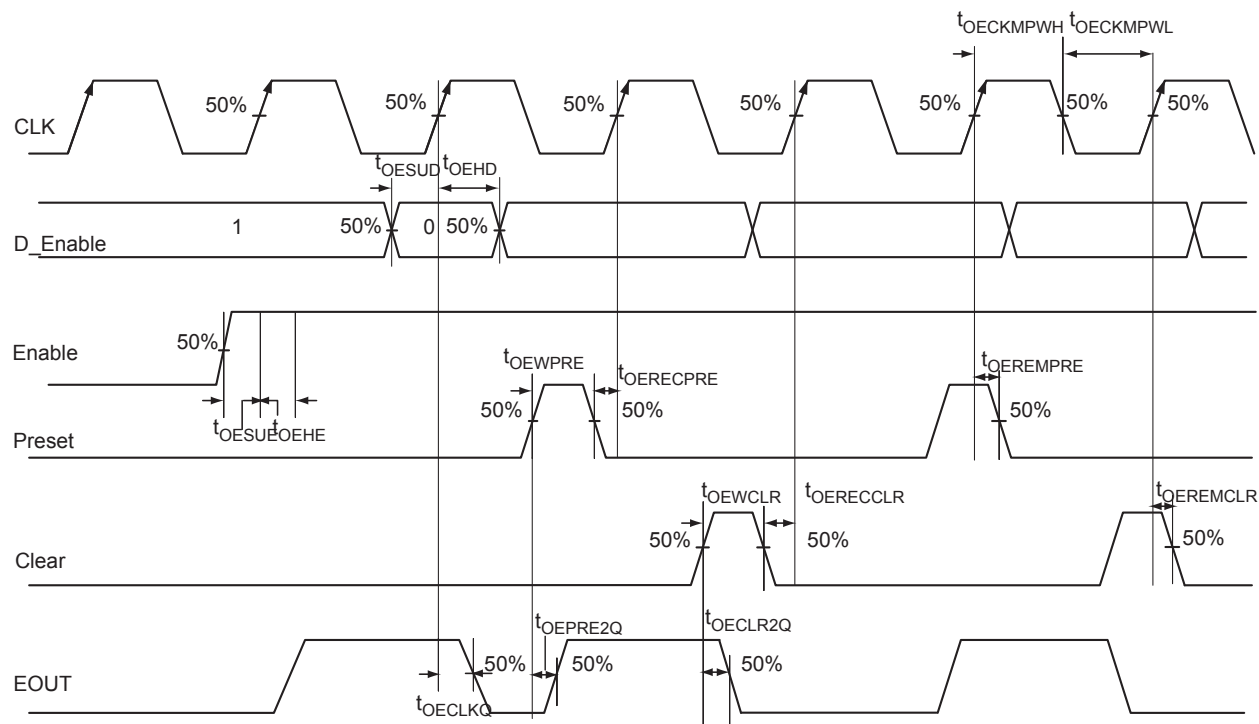


Figure 2-30 • Output Enable Register Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-127 • Output Enable Register Propagation Delays
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.75	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.51	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.73	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.13	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.13	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
t_{OEWPPE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) on [page 2-6](#) for derating values.

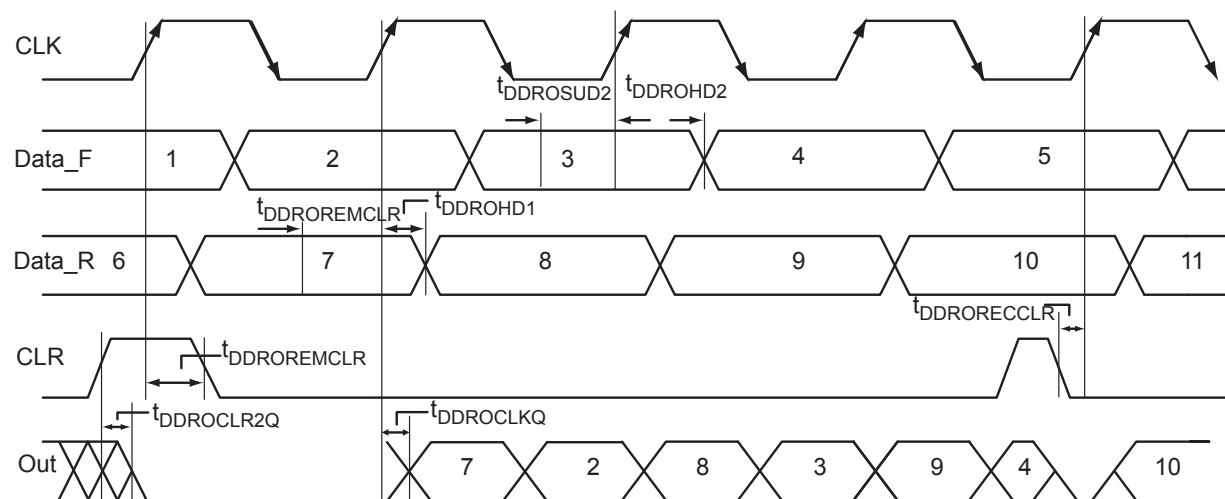


Figure 2-34 • Output DDR Timing Diagram

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The IGLOOe library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the [IGLOO](#), [Fusion](#), and [ProASIC3 Macro Library Guide](#).

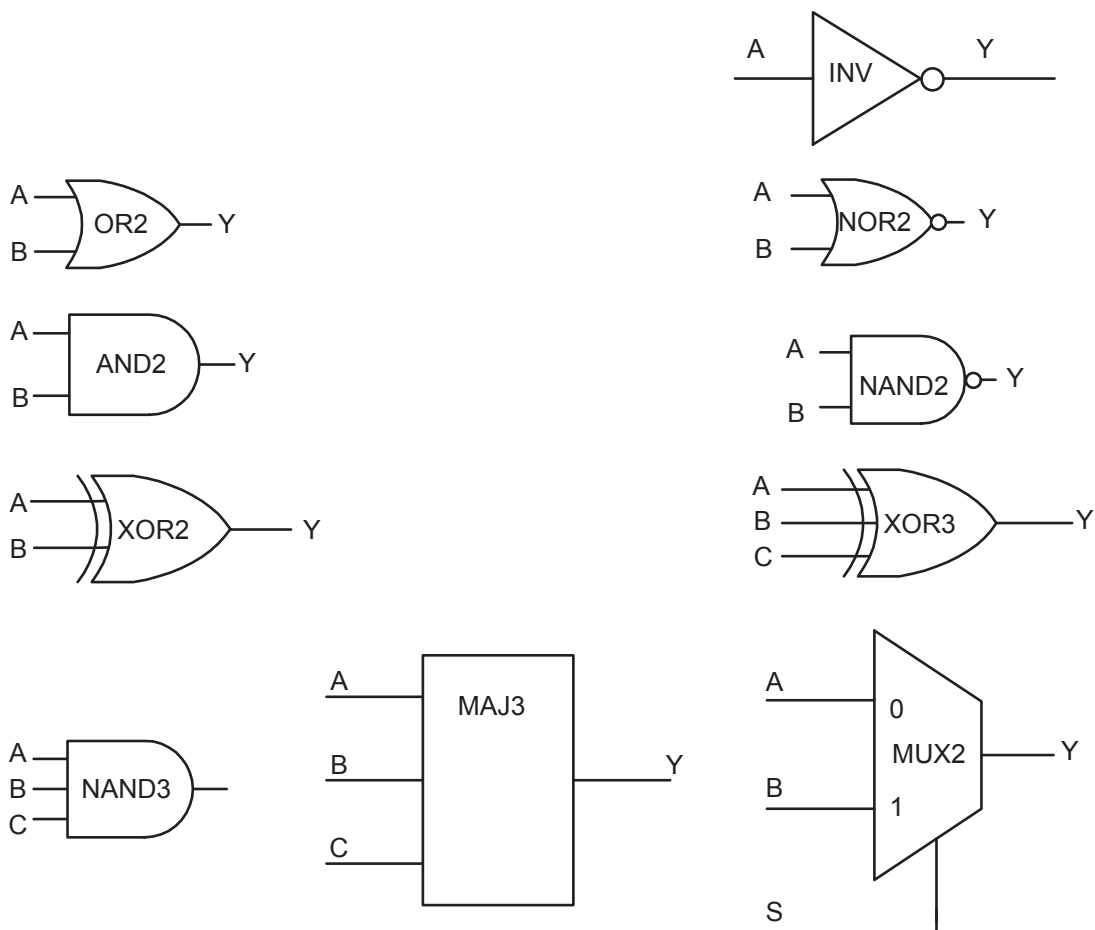


Figure 2-35 • Sample of Combinatorial Cells

FG256	
Pin Number	AGLE600 Function
P9	IO82PDB5V0
P10	IO76NDB4V1
P11	IO76PDB4V1
P12	VMV4
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO67NDB3V1
R1	GEA1/IO102PDB6V0
R2	GEA0/IO102NDB6V0
R3	GNDQ
R4	GEC2/IO99PDB5V2
R5	IO95NPB5V1
R6	IO91NDB5V1
R7	IO91PDB5V1
R8	IO83NDB5V0
R9	IO83PDB5V0
R10	IO77NDB4V1
R11	IO77PDB4V1
R12	IO69NDB4V0
R13	GDB2/IO69PDB4V0
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO100NDB5V2
T3	FF/GEB2/IO100PDB5 V2
T4	IO99NDB5V2
T5	IO88NDB5V0
T6	IO88PDB5V0
T7	IO89NSB5V0
T8	IO80NSB4V1
T9	IO81NDB4V1
T10	IO81PDB4V1
T11	IO70NDB4V0

FG256	
Pin Number	AGLE600 Function
T12	GDC2/IO70PDB4V0
T13	IO68NDB4V0
T14	GDA2/IO68PDB4V0
T15	TMS
T16	GND

FG484	
Pin Number	AGLE3000 Function
C18	GND
C19	IO76PPB1V4
C20	IO88NDB2V0
C21	IO94PPB2V1
C22	VCCIB2
D1	IO293PDB7V2
D2	IO303NDB7V3
D3	IO305NDB7V3
D4	GND
D5	GAA0/IO00NDB0V0
D6	GAA1/IO00PDB0V0
D7	GAB0/IO01NDB0V0
D8	IO20PDB0V2
D9	IO22PDB0V2
D10	IO30PDB0V3
D11	IO38NDB0V4
D12	IO52NDB1V1
D13	IO52PDB1V1
D14	IO66NDB1V3
D15	IO66PDB1V3
D16	GBB1/IO80PDB1V4
D17	GBA0/IO81NDB1V4
D18	GBA1/IO81PDB1V4
D19	GND
D20	IO88PDB2V0
D21	IO90PDB2V1
D22	IO94NPB2V1
E1	IO293NDB7V2
E2	IO299PPB7V3
E3	GND
E4	GAB2/IO308PDB7V4
E5	GAA2/IO309PDB7V4
E6	GNDQ
E7	GAB1/IO01PDB0V0
E8	IO20NDB0V2

FG484	
Pin Number	AGLE3000 Function
E9	IO22NDB0V2
E10	IO30NDB0V3
E11	IO38PDB0V4
E12	IO44NDB1V0
E13	IO58NDB1V2
E14	IO58PDB1V2
E15	GBC1/IO79PDB1V4
E16	GBB0/IO80NDB1V4
E17	GNDQ
E18	GBA2/IO82PDB2V0
E19	IO86NDB2V0
E20	GND
E21	IO90NDB2V1
E22	IO98PDB2V2
F1	IO299NPB7V3
F2	IO301NDB7V3
F3	IO301PDB7V3
F4	IO308NDB7V4
F5	IO309NDB7V4
F6	VMV7
F7	VCCPLA
F8	GAC0/IO02NDB0V0
F9	GAC1/IO02PDB0V0
F10	IO32NDB0V3
F11	IO32PDB0V3
F12	IO44PDB1V0
F13	IO50NDB1V1
F14	IO60PDB1V2
F15	GBC0/IO79NDB1V4
F16	VCCPLB
F17	VMV2
F18	IO82NDB2V0
F19	IO86PDB2V0
F20	IO96PDB2V1
F21	IO96NDB2V1

FG484	
Pin Number	AGLE3000 Function
F22	IO98NDB2V2
G1	IO289NDB7V1
G2	IO289PDB7V1
G3	IO291PPB7V2
G4	IO295PDB7V2
G5	IO297PDB7V2
G6	GAC2/IO307PDB7V4
G7	VCOMPLA
G8	GNDQ
G9	IO26NDB0V3
G10	IO26PDB0V3
G11	IO36PDB0V4
G12	IO42PDB1V0
G13	IO50PDB1V1
G14	IO60NDB1V2
G15	GNDQ
G16	VCOMPLB
G17	GBB2/IO83PDB2V0
G18	IO92PDB2V1
G19	IO92NDB2V1
G20	IO102PDB2V2
G21	IO102NDB2V2
G22	IO105NDB2V2
H1	IO286PSB7V1
H2	IO291NPB7V2
H3	VCC
H4	IO295NDB7V2
H5	IO297NDB7V2
H6	IO307NDB7V4
H7	IO287PDB7V1
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO36NDB0V4
H12	IO42NDB1V0

FG484	
Pin Number	AGLE3000 Function
N8	VCCIB6
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB3
N16	IO116NPB3V0
N17	IO132NPB3V2
N18	IO117NPB3V0
N19	IO132PPB3V2
N20	GNDQ
N21	IO126NDB3V1
N22	IO128PDB3V1
P1	IO247PDB6V1
P2	IO253PDB6V2
P3	IO270NPB6V4
P4	IO261NPB6V3
P5	IO249PPB6V1
P6	IO259PDB6V3
P7	IO259NDB6V3
P8	VCCIB6
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB3
P16	GDB0/IO152NPB3V4
P17	IO136NDB3V2
P18	IO136PDB3V2
P19	IO138PDB3V3
P20	VMV3

FG484	
Pin Number	AGLE3000 Function
P21	IO130PDB3V2
P22	IO128NDB3V1
R1	IO247NDB6V1
R2	IO245PDB6V1
R3	VCC
R4	IO249NPB6V1
R5	IO251NDB6V2
R6	IO251PDB6V2
R7	GEC0/IO236NPB6V0
R8	VMV5
R9	VCCIB5
R10	VCCIB5
R11	IO196NDB5V0
R12	IO196PDB5V0
R13	VCCIB4
R14	VCCIB4
R15	VMV3
R16	VCCPLD
R17	GDB1/IO152PPB3V4
R18	GDC1/IO151PDB3V4
R19	IO138NDB3V3
R20	VCC
R21	IO130NDB3V2
R22	IO134PDB3V2
T1	IO243PPB6V1
T2	IO245NDB6V1
T3	IO243NPB6V1
T4	IO241PDB6V0
T5	IO241NDB6V0
T6	GEC1/IO236PPB6V0
T7	VCOMPLE
T8	GNDQ
T9	GEA2/IO233PPB5V4
T10	IO206NDB5V1
T11	IO202NDB5V1

FG484	
Pin Number	AGLE3000 Function
T12	IO194NDB5V0
T13	IO186NDB4V4
T14	IO186PDB4V4
T15	GNDQ
T16	VCOMPLD
T17	VJTAG
T18	GDC0/IO151NDB3V4
T19	GDA1/IO153PDB3V4
T20	IO144PDB3V3
T21	IO140PDB3V3
T22	IO134NDB3V2
U1	IO240PPB6V0
U2	IO238PDB6V0
U3	IO238NDB6V0
U4	GEB1/IO235PDB6V0
U5	GEB0/IO235NDB6V0
U6	VMV6
U7	VCCPLE
U8	IO233NPB5V4
U9	IO222PPB5V3
U10	IO206PDB5V1
U11	IO202PDB5V1
U12	IO194PDB5V0
U13	IO176NDB4V2
U14	IO176PDB4V2
U15	VMV4
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO153NDB3V4
U20	IO144NDB3V3
U21	IO140NDB3V3
U22	IO142PDB3V3
V1	IO239PDB6V0
V2	IO240NPB6V0

FG484	
Pin Number	AGLE3000 Function
V3	GND
V4	GEA1/IO234PDB6V0
V5	GEA0/IO234NDB6V0
V6	GNDQ
V7	GEC2/IO231PDB5V4
V8	IO222NPB5V3
V9	IO204NDB5V1
V10	IO204PDB5V1
V11	IO195NDB5V0
V12	IO195PDB5V0
V13	IO178NDB4V3
V14	IO178PDB4V3
V15	IO155NDB4V0
V16	GDB2/IO155PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	IO146PDB3V4
V22	IO142NDB3V3
W1	IO239NDB6V0
W2	IO237PDB6V0
W3	IO230PSB5V4
W4	GND
W5	IO232NDB5V4
W6	FF/GEB2/IO232PDB5V4
W7	IO231NDB5V4
W8	IO214NDB5V2
W9	IO214PDB5V2
W10	IO200NDB5V0
W11	IO192NDB4V4
W12	IO184NDB4V3
W13	IO184PDB4V3
W14	IO156NDB4V0

FG484	
Pin Number	AGLE3000 Function
W15	GDC2/IO156PDB4V0
W16	IO154NDB4V0
W17	GDA2/IO154PDB4V0
W18	TMS
W19	GND
W20	IO150NDB3V4
W21	IO146NDB3V4
W22	IO148PPB3V4
Y1	VCCIB6
Y2	IO237NDB6V0
Y3	IO228NDB5V4
Y4	IO224NDB5V3
Y5	GND
Y6	IO220NDB5V3
Y7	IO220PDB5V3
Y8	VCC
Y9	VCC
Y10	IO200PDB5V0
Y11	IO192PDB4V4
Y12	IO188NPB4V4
Y13	IO187PSB4V4
Y14	VCC
Y15	VCC
Y16	IO164NDB4V1
Y17	IO164PDB4V1
Y18	GND
Y19	IO158PPB4V0
Y20	IO150PDB3V4
Y21	IO148NPB3V4
Y22	VCCIB3

Revision	Changes	Page
Revision 8 (Nov 2009)	The version changed to v2.0 for IGLOOe datasheet chapters, indicating the datasheet contains information based on final characterization.	N/A
Product Brief v2.0 DC and Switching Characteristics v2.0	The "Pro (Professional) I/O" section was revised to add "Hot-swappable and cold-sparing I/Os."	I
	The "Reprogrammable Flash Technology" section was revised to add "250 MHz (1.5 V systems) and 160 MHz (1.2 V systems) System Performance."	I
	Definitions of hot-swap and cold-sparing were added to the "Pro I/Os with Advanced I/O Standards" section.	1-7
	3.3 V LVCMOS and 1.2 V LVCMOS Wide Range support was added to the datasheet. This affects all tables that contained 3.3 V LVCMOS and 1.2 V LVCMOS data.	N/A
	IIL and IIH input leakage current information was added to all "Minimum and Maximum DC Input and Output Levels" tables.	N/A
	Values for 1.2 V wide range DC core supply voltage were added to Table 2-2 • Recommended Operating Conditions 1. Table notes regarding 3.3 V wide range and the core voltage required for programming were added to the table.	2-2
	The data in Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (1.5 V DC core supply voltage) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (1.2 V DC core supply voltage) was revised.	2-6
	3.3 V LVCMOS wide range data was included in Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings and Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings1. Table notes were added in connection with this data.	2-9, 2-10
	The temperature was revised from 110°C to 100°C in Table 2-31 • Duration of Short Circuit Event before Failure and Table 2-33 • I/O Input Rise Time, Fall Time, and Related I/O Reliability*.	2-31, 2-31
	The tables in the "Overview of I/O Performance" section and "Detailed I/O DC Characteristics" section were revised to include 3.3 V LVCMOS and 1.2 V LVCMOS wide range.	2-20, 2-28
	Most tables were updated in the following sections, revising existing values and adding information for 3.3 V and 1.2 V wide range: "Single-Ended I/O Characteristics" "Voltage-Referenced I/O Characteristics" "Differential I/O Characteristics"	2-32, 2-51, 2-62
	The value for "Delay range in block: fixed delay" was revised in Table 2-143 • IGLOOe CCC/PLL Specification and Table 2-144 • IGLOOe CCC/PLL Specification.	2-91, 2-92
	The timing characteristics tables for RAM4K9 and RAM512X18 were updated, including renaming of the address collision parameters.	2-98 – 2-101
Revision 7 (Apr 2009) Product Brief v1.4 DC and Switching Characteristics Advance v0.4	The –F speed grade is no longer offered for IGLOOe devices and was removed from the documentation. The speed grade column and note regarding –F speed grade were removed from "IGLOOe Ordering Information". The "Speed Grade and Temperature Grade Matrix" section was removed.	III, IV

Revision	Changes	Page														
Revision 3 (cont'd)	Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings ¹ was updated to change PDC3 to PDC7. The table notes were updated to reflect that power was measured on VCCI. Table note 4 is new.	2-10														
	Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO Devices and Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO Devices were updated to add PDC6 and PDC7, and to change the definition for PDC5 to bank quiescent power.	2-11, 2-12														
	A table subtitle was added for Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO Devices.	2-12														
	The "Total Static Power Consumption—PSTAT" section was updated to revise the calculation of P _{STAT} , including PDC6 and PDC7.	2-13														
	Footnote 1 was updated to include information about P _{AC13} . The PLL Contribution equation was changed from: P _{PLL} = P _{AC13} + P _{AC14} * F _{CLKOUT} to P _{PLL} = P _{DC4} + P _{AC13} * F _{CLKOUT} .	2-14														
	The "Timing Model" was updated to be consistent with the revised timing numbers.	2-16														
	In Table 2-22 • Summary of Maximum and Minimum DC Input Levels, T _J was changed to T _A in notes 1 and 2.	2-22														
	Table 2-22 • Summary of Maximum and Minimum DC Input Levels was updated to included a hysteresis value for 1.2 V LVCMOS (Schmitt trigger mode).	2-22														
	All AC Loading figures for single-ended I/O standards were changed from Datapaths at 35 pF to 5 pF.	N/A														
	The "1.2 V LVCMOS (JESD8-12A)" section is new.	2-47														
Revision 2 (Jun 2008) Product Brief v1.0	The product brief section of the datasheet was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.	N/A														
Revision 2 (cont'd) Packaging v1.1	The naming conventions changed for the following pins in the "FG484" for the A3GLE600: <table><tr><td>Pin Number</td><td>New Function Name</td></tr><tr><td>J19</td><td>IO45PPB2V1</td></tr><tr><td>K20</td><td>IO45NPB2V1</td></tr><tr><td>M2</td><td>IO114NPB6V1</td></tr><tr><td>N1</td><td>IO114PPB6V1</td></tr><tr><td>N4</td><td>GFC2/IO115PPB6V1</td></tr><tr><td>P3</td><td>IO115NPB6V1</td></tr></table>	Pin Number	New Function Name	J19	IO45PPB2V1	K20	IO45NPB2V1	M2	IO114NPB6V1	N1	IO114PPB6V1	N4	GFC2/IO115PPB6V1	P3	IO115NPB6V1	4-6
Pin Number	New Function Name															
J19	IO45PPB2V1															
K20	IO45NPB2V1															
M2	IO114NPB6V1															
N1	IO114PPB6V1															
N4	GFC2/IO115PPB6V1															
P3	IO115NPB6V1															
Revision 1 (Mar 2008) Product Brief rev. 1	The "Low Power" section was updated to change "1.2 V and 1.5 V Core Voltage" to "1.2 V and 1.5 V Core and I/O Voltage." The text "(from 25 μW)" was removed from "Low Power Active FPGA Operation." 1.2_V was added to the list of core and I/O voltages in the "Pro (Professional) I/O" and "Pro I/Os with Advanced I/O Standards" section sections.	I I, 1-7														
Revision 0 (Jan 2008)	This document was previously in datasheet Advance v0.4. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is 51700096-001-0.	N/A														