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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	75264
Total RAM Bits	516096
Number of I/O	341
Number of Gates	3000000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agle3000v2-fgg484

Temperature Grade Offerings

Package	AGLE600	AGLE3000
		M1AGLPE3000
FG256	C, I	–
FG484	C, I	C, I
FG896	–	C, I

Note: C = Commercial temperature range: 0°C to 70°C ambient temperature.
I = Industrial temperature range: –40°C to 85°C ambient temperature.

References made to IGLOOe devices also apply to ARM-enabled IGLOOe devices. The ARM-enabled part numbers start with M1 (Cortex-M1).

Contact your local Microsemi SoC Products Group representative for device availability:

http://www.microsemi.com/soc/contact/default.aspx.

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Flash Advantages

Low Power

Flash-based IGLOOe devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOOe devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOOe devices also have low dynamic power consumption to further maximize power savings; power is even further reduced by the use of a 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, gives the IGLOOe device the lowest total system power offered by any FPGA.

Security

The nonvolatile, flash-based IGLOOe devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOOe devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOOe devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of protection in the FPGA industry for programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOOe devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOOe devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOOe devices with AES-based security provide a high level of protection for remote field updates over public networks such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of the IGLOOe family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The IGLOOe family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. An IGLOOe device provides the best available security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOOe FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Instant On

Flash-based IGLOOe devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based IGLOOe devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOOe device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOOe devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature[1]

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

Table 2-4 • Overshoot and Undershoot Limits [1, 3]

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at junction temperature at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
3. *This table does not provide PCI overshoot/undershoot limits.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOOe device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5.

There are five regions to consider during power-up.

IGLOOe I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.

Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels (continued) Applicable to Commercial and Industrial Conditions

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength[2]	Slew Rate	VIL		VIH		VOL	VOH	IOL[1]	IOH[1]
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
HSTL (II)	15 mA[5]	15 mA[5]	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15
SSTL2 (I)	15 mA	15 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15
SSTL2 (II)	18 mA	18 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18
SSTL3 (I)	14 mA	14 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14
SSTL3 (II)	21 mA	21 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-12 specification.*
4. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*
5. *Output drive strength is below JEDEC specification.*
6. *Output Slew Rates can be extracted from IBIS Models, http://www.microsemi.com/soc/download/ibis/default.aspx.*

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer. The 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTL support.

Table 2-34 • Minimum and Maximum DC Input and Output Levels

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	10	10
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

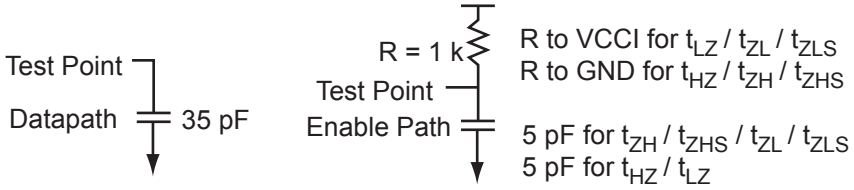


Figure 2-7 • AC Loading

Table 2-35 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	5

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

1.2 V DC Core Voltage

Table 2-56 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	8.21	0.26	1.53	1.96	1.10	8.35	6.88	2.87	1.70	14.14	12.67	ns
4 mA	Std.	1.55	6.83	0.26	1.53	1.96	1.10	6.94	5.88	3.27	3.18	12.73	11.67	ns
6 mA	Std.	1.55	5.85	0.26	1.53	1.96	1.10	5.94	5.19	3.53	3.37	11.73	10.98	ns
8 mA	Std.	1.55	5.52	0.26	1.53	1.96	1.10	5.61	5.06	3.59	3.88	11.39	10.84	ns
12 mA	Std.	1.55	5.42	0.26	1.53	1.96	1.10	5.51	5.06	3.68	4.44	11.30	10.85	ns
16 mA	Std.	1.55	5.42	0.26	1.53	1.96	1.10	5.51	5.06	3.68	4.44	11.30	10.85	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-57 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.82	0.26	1.53	1.96	1.10	3.98	3.87	2.86	1.72	9.76	9.66	ns
4 mA	Std.	1.55	3.25	0.26	1.53	1.96	1.10	3.30	3.01	3.26	3.26	9.08	8.79	ns
6 mA	Std.	1.55	2.84	0.26	1.53	1.96	1.10	2.88	2.58	3.53	3.81	8.66	8.37	ns
8 mA	Std.	1.55	2.76	0.26	1.53	1.96	1.10	2.80	2.50	3.58	3.97	8.58	8.29	ns
12 mA	Std.	1.55	2.75	0.26	1.53	1.96	1.10	2.78	2.40	3.68	4.56	8.57	8.19	ns
16 mA	Std.	1.55	2.75	0.26	1.53	1.96	1.10	2.78	2.40	3.68	4.56	8.57	8.19	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-60 • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	7.61	0.18	1.47	1.77	0.66	7.76	6.33	2.81	2.34	11.36	9.92	ns
4 mA	Std.	0.97	6.54	0.18	1.47	1.77	0.66	6.67	5.56	3.09	2.88	10.26	9.16	ns
6 mA	Std.	0.97	6.15	0.18	1.47	1.77	0.66	6.27	5.42	3.15	3.02	9.87	9.02	ns
8 mA	Std.	0.97	6.07	0.18	1.47	1.77	0.66	6.20	5.42	2.64	3.56	9.79	9.02	ns
12 mA	Std.	0.97	6.07	0.18	1.47	1.77	0.66	6.20	5.42	2.64	3.56	9.79	9.02	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-61 • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	3.25	0.18	1.47	1.77	0.66	3.32	3.00	2.80	2.43	6.92	6.59	ns
4 mA	Std.	0.97	2.81	0.18	1.47	1.77	0.66	2.87	2.51	3.08	2.97	6.46	6.10	ns
6 mA	Std.	0.97	2.72	0.18	1.47	1.77	0.66	2.78	2.41	3.14	3.12	6.37	6.01	ns
8 mA	Std.	0.97	2.69	0.18	1.47	1.77	0.66	2.75	2.30	3.24	3.67	6.35	5.89	ns
12 mA	Std.	0.97	2.69	0.18	1.47	1.77	0.66	2.75	2.30	3.24	3.67	6.35	5.89	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Voltage-Referenced I/O Characteristics

3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-73 • Minimum and Maximum DC Input and Output Levels

3.3 V GTL	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
20 mA[5]	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20	268	181	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Output drive strength is below JEDEC specification.*

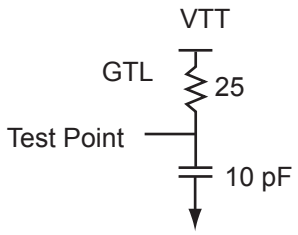


Figure 2-13 • AC Loading

Table 2-74 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.05	VREF + 0.05	0.8	0.8	1.2	10

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). IGLOOe devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-89 • Minimum and Maximum DC Input and Output Levels

HSTL Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
8 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	8	8	32	39	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

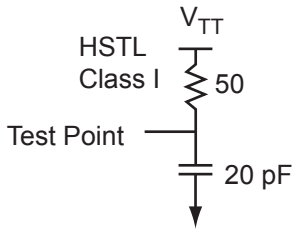


Figure 2-17 • AC Loading

Table 2-90 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-91 • HSTL Class I – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 1.4 V VREF = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	2.74	0.19	1.77	0.67	2.79	2.73			6.42	6.36	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-92 • HSTL Class I – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 1.4 V VREF = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	3.10	0.26	1.94	1.10	3.12	3.10			8.93	8.91	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). IGLOOe devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-101 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
18 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18	169	124	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

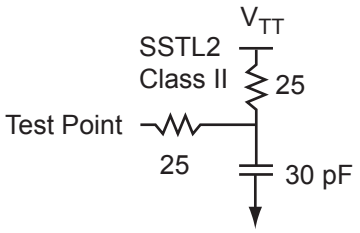


Figure 2-20 • AC Loading

Table 2-102 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input HIGH (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-103 • SSTL 2 Class II – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 2.3 V VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	1.94	0.19	1.15	0.67	1.97	1.66			5.60	5.29	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-104 • SSTL 2 Class II – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 2.3 V VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.20	0.26	1.39	1.10	2.24	1.97			8.05	7.78	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

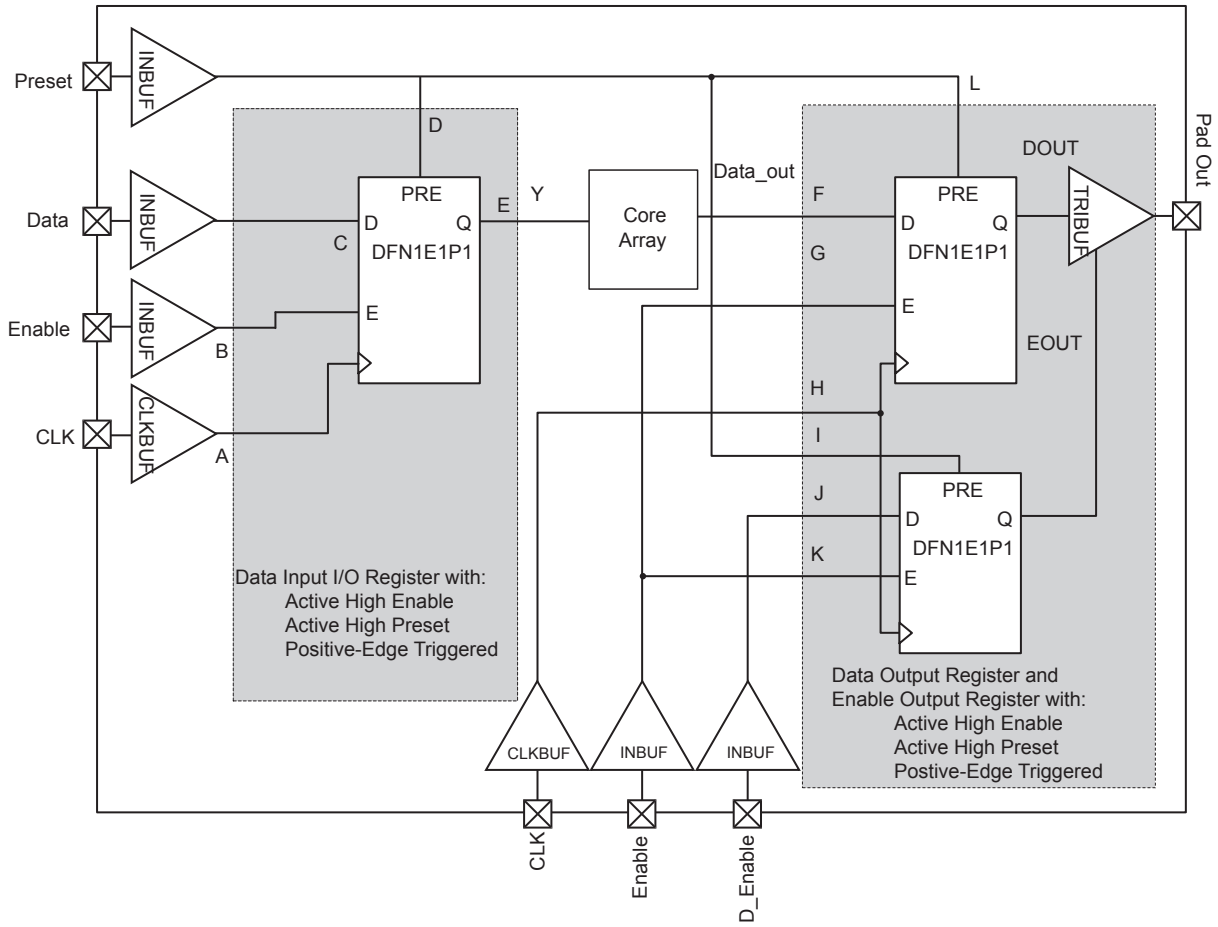


Figure 2-26 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

***Table 2-121* • Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: See Figure 2-26 on page 2-66 for more information.

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-149 • FIFO
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.99	ns
t_{ENH}	REN, WEN Hold Time	0.16	ns
t_{BKS}	BLK Setup Time	0.30	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.76	ns
t_{DH}	Input Data (WD) Hold Time	0.25	ns
t_{CKQ1}	Clock HIGH to New Data Valid on RD (pass-through)	3.33	ns
t_{CKQ2}	Clock HIGH to New Data Valid on RD (pipelined)	1.80	ns
t_{RCKEF}	RCLK HIGH to Empty Flag Valid	3.53	ns
t_{WCKFF}	WCLK HIGH to Full Flag Valid	3.35	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	12.85	ns
t_{RSTFG}	RESET LOW to Empty/Full Flag Valid	3.48	ns
t_{RSTAF}	RESET LOW to Almost Empty/Full Flag Valid	12.72	ns
t_{RSTBQ}	RESET LOW to Data Out LOW on RD (pass-through)	2.02	ns
	RESET LOW to Data Out LOW on RD (pipelined)	2.02	ns
$t_{REMRSTB}$	RESET Removal	0.61	ns
$t_{RECRSTB}$	RESET Recovery	3.21	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.68	ns
t_{CYC}	Clock Cycle Time	6.24	ns
F_{MAX}	Maximum Frequency	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

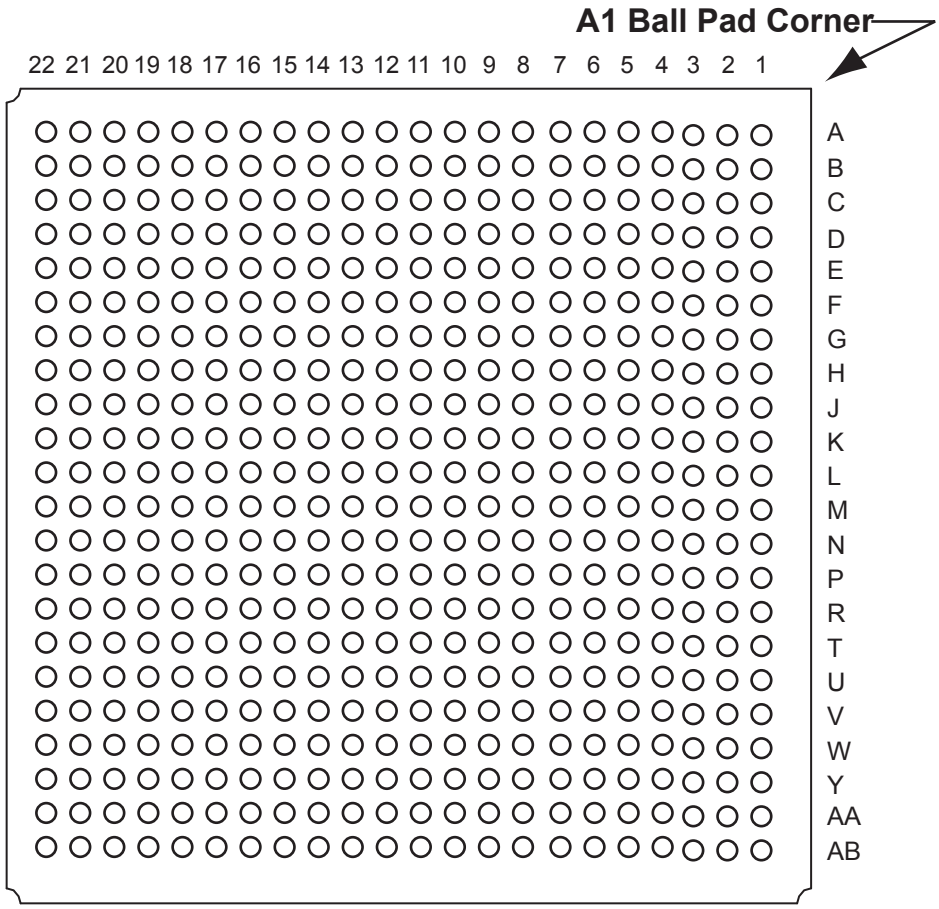
Applies to 1.2 V DC Core Voltage

Table 2-150 • FIFO
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	4.13	ns
t_{ENH}	REN, WEN Hold Time	0.31	ns
t_{BKS}	BLK Setup Time	0.47	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (WD) Setup Time	1.56	ns
t_{DH}	Input Data (WD) Hold Time	0.49	ns
t_{CKQ1}	Clock HIGH to New Data Valid on RD (pass-through)	6.80	ns
t_{CKQ2}	Clock HIGH to New Data Valid on RD (pipelined)	3.62	ns
t_{RCKEF}	RCLK HIGH to Empty Flag Valid	7.23	ns
t_{WCKFF}	WCLK HIGH to Full Flag Valid	6.85	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	26.61	ns
t_{RSTFG}	RESET LOW to Empty/Full Flag Valid	7.12	ns
t_{RSTAF}	RESET LOW to Almost Empty/Full Flag Valid	26.33	ns
t_{RSTBQ}	RESET LOW to Data Out LOW on RD (pass-through)	4.09	ns
	RESET LOW to Data Out LOW on RD (pipelined)	4.09	ns
$t_{REMRSTB}$	RESET Removal	1.23	ns
$t_{RECRSTB}$	RESET Recovery	6.58	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	1.18	ns
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

FG484



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

FG484	
Pin Number	**AGLE600 Function**
V3	GND
V4	GEA1/IO102PDB6V0
V5	GEA0/IO102NDB6V0
V6	GNDQ
V7	GEC2/IO99PDB5V2
V8	IO95NPB5V1
V9	IO91NDB5V1
V10	IO91PDB5V1
V11	IO83NDB5V0
V12	IO83PDB5V0
V13	IO77NDB4V1
V14	IO77PDB4V1
V15	IO69NDB4V0
V16	GDB2/IO69PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO63NDB3V1
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO100NDB5V2
W6	FF/GEB2/IO100PDB5V2
W7	IO99NDB5V2
W8	IO88NDB5V0
W9	IO88PDB5V0
W10	IO89NDB5V0
W11	IO80NDB4V1
W12	IO81NDB4V1
W13	IO81PDB4V1
W14	IO70NDB4V0
W15	GDC2/IO70PDB4V0

FG484	
Pin Number	**AGLE600 Function**
W16	IO68NDB4V0
W17	GDA2/IO68PDB4V0
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB6
Y2	NC
Y3	NC
Y4	IO98NDB5V2
Y5	GND
Y6	IO94NDB5V1
Y7	IO94PDB5V1
Y8	VCC
Y9	VCC
Y10	IO89PDB5V0
Y11	IO80PDB4V1
Y12	IO78NPB4V1
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB3

FG484	
Pin Number	AGLE3000 Function
C18	GND
C19	IO76PPB1V4
C20	IO88NDB2V0
C21	IO94PPB2V1
C22	VCCIB2
D1	IO293PDB7V2
D2	IO303NDB7V3
D3	IO305NDB7V3
D4	GND
D5	GAA0/IO00NDB0V0
D6	GAA1/IO00PDB0V0
D7	GAB0/IO01NDB0V0
D8	IO20PDB0V2
D9	IO22PDB0V2
D10	IO30PDB0V3
D11	IO38NDB0V4
D12	IO52NDB1V1
D13	IO52PDB1V1
D14	IO66NDB1V3
D15	IO66PDB1V3
D16	GBB1/IO80PDB1V4
D17	GBA0/IO81NDB1V4
D18	GBA1/IO81PDB1V4
D19	GND
D20	IO88PDB2V0
D21	IO90PDB2V1
D22	IO94NPB2V1
E1	IO293NDB7V2
E2	IO299PPB7V3
E3	GND
E4	GAB2/IO308PDB7V4
E5	GAA2/IO309PDB7V4
E6	GNDQ
E7	GAB1/IO01PDB0V0
E8	IO20NDB0V2

FG484	
Pin Number	AGLE3000 Function
E9	IO22NDB0V2
E10	IO30NDB0V3
E11	IO38PDB0V4
E12	IO44NDB1V0
E13	IO58NDB1V2
E14	IO58PDB1V2
E15	GBC1/IO79PDB1V4
E16	GBB0/IO80NDB1V4
E17	GNDQ
E18	GBA2/IO82PDB2V0
E19	IO86NDB2V0
E20	GND
E21	IO90NDB2V1
E22	IO98PDB2V2
F1	IO299NPB7V3
F2	IO301NDB7V3
F3	IO301PDB7V3
F4	IO308NDB7V4
F5	IO309NDB7V4
F6	VMV7
F7	VCCPLA
F8	GAC0/IO02NDB0V0
F9	GAC1/IO02PDB0V0
F10	IO32NDB0V3
F11	IO32PDB0V3
F12	IO44PDB1V0
F13	IO50NDB1V1
F14	IO60PDB1V2
F15	GBC0/IO79NDB1V4
F16	VCCPLB
F17	VMV2
F18	IO82NDB2V0
F19	IO86PDB2V0
F20	IO96PDB2V1
F21	IO96NDB2V1

FG484	
Pin Number	AGLE3000 Function
F22	IO98NDB2V2
G1	IO289NDB7V1
G2	IO289PDB7V1
G3	IO291PPB7V2
G4	IO295PDB7V2
G5	IO297PDB7V2
G6	GAC2/IO307PDB7V4
G7	VCOMPLA
G8	GNDQ
G9	IO26NDB0V3
G10	IO26PDB0V3
G11	IO36PDB0V4
G12	IO42PDB1V0
G13	IO50PDB1V1
G14	IO60NDB1V2
G15	GNDQ
G16	VCOMPLB
G17	GBB2/IO83PDB2V0
G18	IO92PDB2V1
G19	IO92NDB2V1
G20	IO102PDB2V2
G21	IO102NDB2V2
G22	IO105NDB2V2
H1	IO286PSB7V1
H2	IO291NPB7V2
H3	VCC
H4	IO295NDB7V2
H5	IO297NDB7V2
H6	IO307NDB7V4
H7	IO287PDB7V1
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO36NDB0V4
H12	IO42NDB1V0

FG484	
Pin Number	AGLE3000 Function
H13	VCCIB1
H14	VCCIB1
H15	VMV1
H16	GBC2/IO84PDB2V0
H17	IO83NDB2V0
H18	IO100NDB2V2
H19	IO100PDB2V2
H20	VCC
H21	VMV2
H22	IO105PDB2V2
J1	IO285NDB7V1
J2	IO285PDB7V1
J3	VMV7
J4	IO279PDB7V0
J5	IO283PDB7V1
J6	IO281PDB7V0
J7	IO287NDB7V1
J8	VCCIB7
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB2
J16	IO84NDB2V0
J17	IO104NDB2V2
J18	IO104PDB2V2
J19	IO106PPB2V3
J20	GNDQ
J21	IO109PDB2V3
J22	IO107PDB2V3
K1	IO277NDB7V0
K2	IO277PDB7V0
K3	GNDQ

FG484	
Pin Number	AGLE3000 Function
K4	IO279NDB7V0
K5	IO283NDB7V1
K6	IO281NDB7V0
K7	GFC1/IO275PPB7V0
K8	VCCIB7
K9	VCC
K10	GND
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB2
K16	GCC1/IO112PPB2V3
K17	IO108NDB2V3
K18	IO108PDB2V3
K19	IO110NPB2V3
K20	IO106NPB2V3
K21	IO109NDB2V3
K22	IO107NDB2V3
L1	IO257PSB6V2
L2	IO276PDB7V0
L3	IO276NDB7V0
L4	GFB0/IO274NPB7V0
L5	GFA0/IO273NDB6V4
L6	GFB1/IO274PPB7V0
L7	VCOMPLF
L8	GFC0/IO275NPB7V0
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO112NPB2V3
L16	GCB1/IO113PPB2V3

FG484	
Pin Number	AGLE3000 Function
L17	GCA0/IO114NPB3V0
L18	VCOMPLC
L19	GCB0/IO113NPB2V3
L20	IO110PPB2V3
L21	IO111NDB2V3
L22	IO111PDB2V3
M1	GNDQ
M2	IO255NPB6V2
M3	IO272NDB6V4
M4	GFA2/IO272PDB6V4
M5	GFA1/IO273PDB6V4
M6	VCCPLF
M7	IO271NDB6V4
M8	GFB2/IO271PDB6V4
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO116PPB3V0
M16	GCA1/IO114PPB3V0
M17	GCC2/IO117PPB3V0
M18	VCCPLC
M19	GCA2/IO115PDB3V0
M20	IO115NDB3V0
M21	IO126PDB3V1
M22	IO124PSB3V1
N1	IO255PPB6V2
N2	IO253NDB6V2
N3	VMV6
N4	GFC2/IO270PPB6V4
N5	IO261PPB6V3
N6	IO263PDB6V3
N7	IO263NDB6V3

Revision	Changes	Page
Revision 10 (April 2012)	In Table 2-2 • Recommended Operating Conditions 1, VPUMP programming voltage for operation was changed from "0 to 3.45 V" to "0 to 3.6 V" (SAR 32256). Values for VCCPLL at 1.2–1.5 V DC core supply voltage were changed from "1.14 to 1.26 V" to "1.14 to 1.575 V" (SAR 34701).	2-2
	The tables in the "Quiescent Supply Current" section were updated with revised notes on IDD. Table 2-8 • Power Supply State per Mode is new (SARs 34745, 36949).	2-7
	t_{DOUT} was corrected to t_{DIN} in Figure 2-4 • Input Buffer Timing Model and Delays (example) (SAR 37105).	2-17
	"TBD" for 3.3 V LVCMOS Wide Range in Table 2-28 • I/O Output Buffer Maximum Resistances1 and Table 2-30 • I/O Short Currents IOSH/IOSL was replaced by "Same as regular 3.3 V LVCMOS" (SAR 33855). Values were also added for 1.2 V LVCMOS and 1.2 V LVCMOS Wide Range.	2-28, 2-30
	The formulas in the table notes for Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 34753).	2-29
	IOSH and IOSL values were added to 3.3 V LVCMOS Wide Range Table 2-40 • Minimum and Maximum DC Input and Output Levels, 1.2 V LVCMOS Table 2-64 • Minimum and Maximum DC Input and Output Levels, and 1.2 V LVCMOS Wide Range Table 2-68 • Minimum and Maximum DC Input and Output Levels (SAR 33855).	2-35, 2-47, 2-48
	Figure 2-48 • FIFO Read and Figure 2-49 • FIFO Write have been added (SAR 34844).	2-103
	Values for $F_{DDRIMAX}$ and F_{DDOMAX} were added to the tables in the Input DDR "Timing Characteristics" section and Output DDR "Timing Characteristics" section (SAR 34802).	2-77,2-81
	Minimum pulse width High and Low values were added to the tables in the "Global Tree Timing Characteristics" section. The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 36952).	2-89
Revision 9 (March 2012)	The "In-System Programming (ISP) and Security" section and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34665).	I, 1-2
	The Y security option and Licensed DPA Logo were added to the "IGLOOe Ordering Information" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 34725).	III
	The following sentence was removed from the "Advanced Architecture" section: "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOOe devices via an IEEE 1532 JTAG interface" (SAR 34685).	1-3
	The "Specifying I/O States During Programming" section is new (SAR 34696).	1-7
	Values for VCCPLL at 1.5 V DC core supply voltage were changed from "1.4 to 1.6 V" to "1.425 to 1.575 V" in Table 2-2 • Recommended Operating Conditions 1 (SAR 32292).	2-2
	The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Contribution—PCLOCK" section, was corrected to the "Spine Architecture" section of the Global Resources chapter in the *IGLOOe FPGA Fabric User's Guide* (SAR 34731).	2-13