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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	75264
Total RAM Bits	516096
Number of I/O	341
Number of Gates	3000000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agle3000v2-fgg484i

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, Flash-based IGLOOe devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The IGLOOe family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the IGLOOe family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOOe flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOOe FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The IGLOOe family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOOe family FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

Advanced Architecture

The proprietary IGLOOe architecture provides granularity comparable to standard-cell ASICs. The IGLOOe device consists of five distinct and programmable architectural features (Figure 1-1 on page 4):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- Pro I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOOe core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Microsemi ProASIC® family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

Pro I/Os with Advanced I/O Standards

The IGLOOe family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V). IGLOOe FPGAs support 19 different I/O standards, including single-ended, differential, and voltage-referenced. The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported. Each I/O bank is subdivided into VREF minibanks, which are used by voltage-referenced I/Os. VREF minibanks contain 8 to 18 I/Os. All the I/Os in a given minibank share a common VREF line. Therefore, if any I/O in a given VREF minibank is configured as a VREF pin, the remaining I/Os in that minibank will be able to use that reference voltage.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications (e.g., PCI 66 MHz, bidirectional SSTL 2 and 3, Class I and II)
- Double-Data-Rate applications (e.g., DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications, and DDR 200 MHz SRAM using bidirectional HSTL Class II).

IGLOOe banks support M-LVDS with 20 multi-drop points.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Wide Range I/O Support

IGLOOe devices support JEDEC-defined wide range I/O operation. IGLOOe devices support both the JESD8-B specification, covering 3.0 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click **PDB Configuration**. A FlashPoint – Programming File Generator window appears.
3. Click the **Specify I/O States During Programming** button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-4 on page 1-8).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

   Z -Tri-State: I/O is tristated

User I/O Characteristics

Timing Model

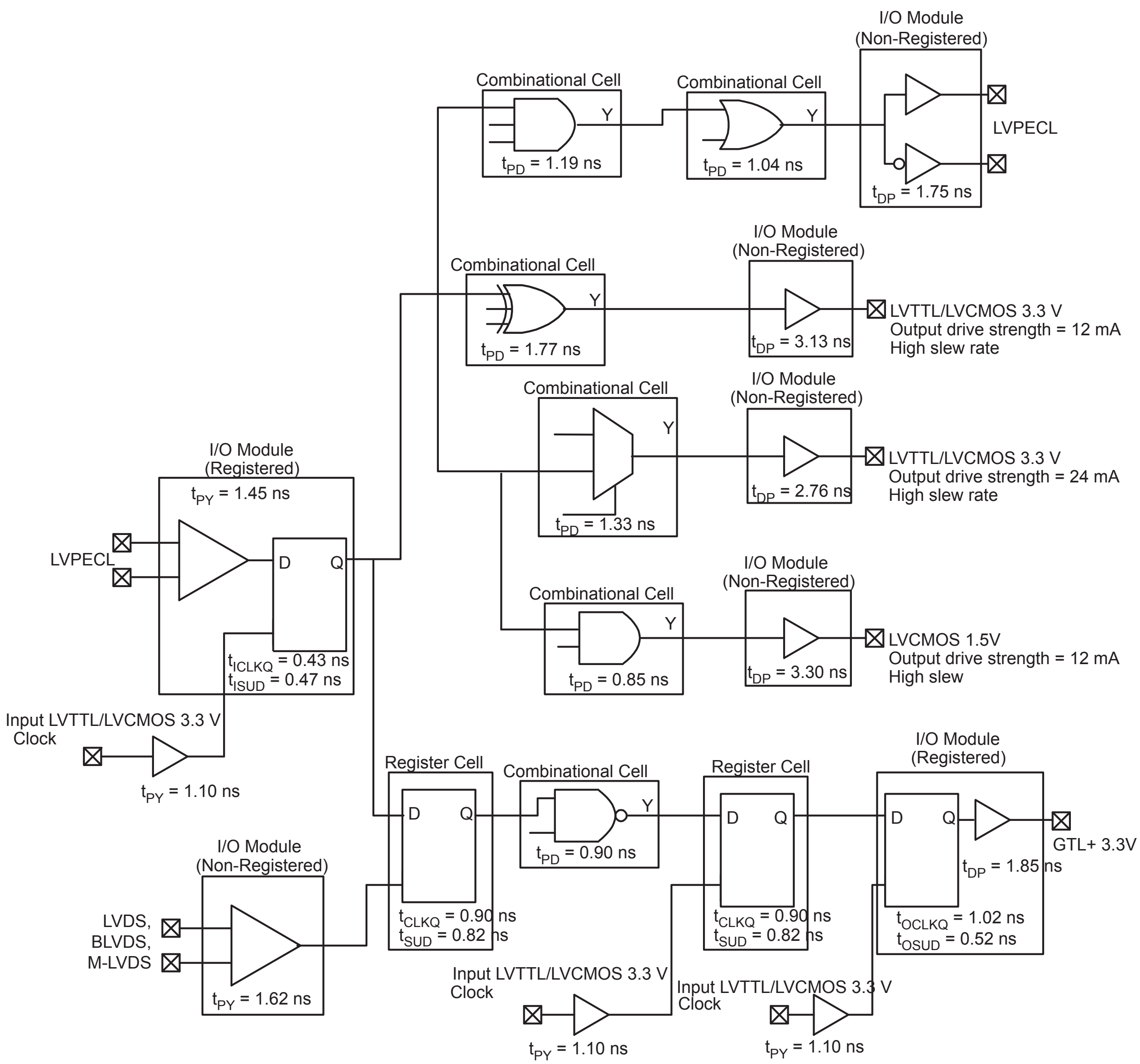

Figure 2-3 • **Timing Model**
Operating Conditions: Std. Speed, Commercial Temperature Range (T_J = 70°C), Worst-Case VCC = 1.425 V, Applicable to 1.5 V DC Core Voltage, V2 and V5 devices

***Table 2-30* • I/O Short Currents IOSH/IOSL**

	Drive Strength	IOSH (mA)*	IOSL (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	25	27
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
1.2 V LVCMOS	2 mA	20	26
1.2 V LVCMOS Wide Range	100 µA	20	26
3.3 V PCI/PCIX	Per PCI/PCI-X Specification	Per PCI Curves	
3.3 V GTL	25 mA	268	181
2.5 V GTL	25 mA	169	124
3.3 V GTL+	35 mA	268	181
2.5 V GTL+	33 mA	169	124
HSTL (I)	8 mA	32	39
HSTL (II)	15 mA	66	55
SSTL2 (I)	15 mA	83	87
SSTL2 (II)	18 mA	169	124
SSTL3 (I)	14 mA	51	54
SSTL3 (II)	21 mA	103	109

Note: $T_J = 100°C$

1.2 V DC Core Voltage

Table 2-38 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.55	5.54	0.26	1.31	1.58	1.10	5.63	4.53	2.79	2.87	11.42	10.32	ns
8 mA	Std.	1.55	4.60	0.26	1.31	1.58	1.10	4.67	3.94	3.09	3.45	10.45	9.73	ns
12 mA	Std.	1.55	3.93	0.26	1.31	1.58	1.10	3.99	3.51	3.28	3.82	9.77	9.29	ns
16 mA	Std.	1.55	3.74	0.26	1.31	1.58	1.10	3.79	3.41	3.32	3.92	9.58	9.20	ns
24 mA	Std.	1.55	3.64	0.26	1.31	1.58	1.10	3.69	3.42	3.38	4.30	9.48	9.21	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-39 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.55	3.26	0.26	1.31	1.58	1.10	3.33	2.67	2.79	3.01	9.12	8.46	ns
8 mA	Std.	1.55	2.77	0.26	1.31	1.58	1.10	2.80	2.24	3.09	3.59	8.59	8.03	ns
12 mA	Std.	1.55	2.47	0.26	1.31	1.58	1.10	2.51	2.04	3.28	3.97	8.29	7.82	ns
16 mA	Std.	1.55	2.42	0.26	1.31	1.58	1.10	2.46	2.00	3.33	4.08	8.24	7.79	ns
24 mA	Std.	1.55	2.45	0.26	1.31	1.58	1.10	2.48	1.95	3.38	4.46	8.26	7.73	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-42 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	4 mA	Std.	0.97	7.26	0.18	1.42	1.84	0.66	7.28	5.78	3.18	2.93	10.88	9.38	ns
100 µA	8 mA	Std.	0.97	5.94	0.18	1.42	1.84	0.66	5.96	4.96	3.59	3.69	9.56	8.56	ns
100 µA	12 mA	Std.	0.97	5.00	0.18	1.42	1.84	0.66	5.02	4.34	3.86	4.16	8.62	7.94	ns
100 µA	16 mA	Std.	0.97	4.73	0.18	1.42	1.84	0.66	4.75	4.21	3.92	4.29	8.35	7.81	ns
100 µA	24 mA	Std.	0.97	4.59	0.18	1.42	1.84	0.66	4.61	4.23	3.99	4.78	8.21	7.82	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-43 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	4 mA	Std.	0.97	4.10	0.18	1.42	1.84	0.66	4.12	3.17	3.18	3.11	7.71	6.77	ns
100 µA	8 mA	Std.	0.97	3.37	0.18	1.42	1.84	0.66	3.39	2.57	3.59	3.87	6.99	6.16	ns
100 µA	12 mA	Std.	0.97	2.96	0.18	1.42	1.84	0.66	2.98	2.28	3.86	4.36	6.58	5.87	ns
100 µA	16 mA	Std.	0.97	2.90	0.18	1.42	1.84	0.66	2.92	2.22	3.93	4.49	6.51	5.82	ns
100 µA	24 mA	Std.	0.97	2.92	0.18	1.42	1.84	0.66	2.94	2.15	4.00	4.99	6.54	5.75	ns

Notes:

1. *The minimum drive strength for any or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
3. *Software default selection highlighted in gray.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-46 • **Minimum and Maximum DC Input and Output Levels**

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	μA[4]	μA[4]
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	65	74	10	10
16 mA	–0.3	0.7	1.7	3.6	0.7	1.7	16	16	83	87	10	10
24 mA	–0.3	0.7	1.7	3.6	0.7	1.7	24	24	169	124	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

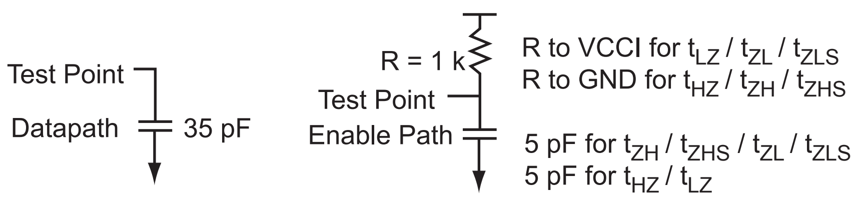

Figure 2-8 • **AC Loading**

Table 2-47 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	5

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-60 • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	7.61	0.18	1.47	1.77	0.66	7.76	6.33	2.81	2.34	11.36	9.92	ns
4 mA	Std.	0.97	6.54	0.18	1.47	1.77	0.66	6.67	5.56	3.09	2.88	10.26	9.16	ns
6 mA	Std.	0.97	6.15	0.18	1.47	1.77	0.66	6.27	5.42	3.15	3.02	9.87	9.02	ns
8 mA	Std.	0.97	6.07	0.18	1.47	1.77	0.66	6.20	5.42	2.64	3.56	9.79	9.02	ns
12 mA	Std.	0.97	6.07	0.18	1.47	1.77	0.66	6.20	5.42	2.64	3.56	9.79	9.02	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-61 • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	3.25	0.18	1.47	1.77	0.66	3.32	3.00	2.80	2.43	6.92	6.59	ns
4 mA	Std.	0.97	2.81	0.18	1.47	1.77	0.66	2.87	2.51	3.08	2.97	6.46	6.10	ns
6 mA	Std.	0.97	2.72	0.18	1.47	1.77	0.66	2.78	2.41	3.14	3.12	6.37	6.01	ns
8 mA	Std.	0.97	2.69	0.18	1.47	1.77	0.66	2.75	2.30	3.24	3.67	6.35	5.89	ns
12 mA	Std.	0.97	2.69	0.18	1.47	1.77	0.66	2.75	2.30	3.24	3.67	6.35	5.89	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-121 **• Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: *See Figure 2-26 on page 2-66 for more information.*

DDR Module Specifications

Input DDR Module

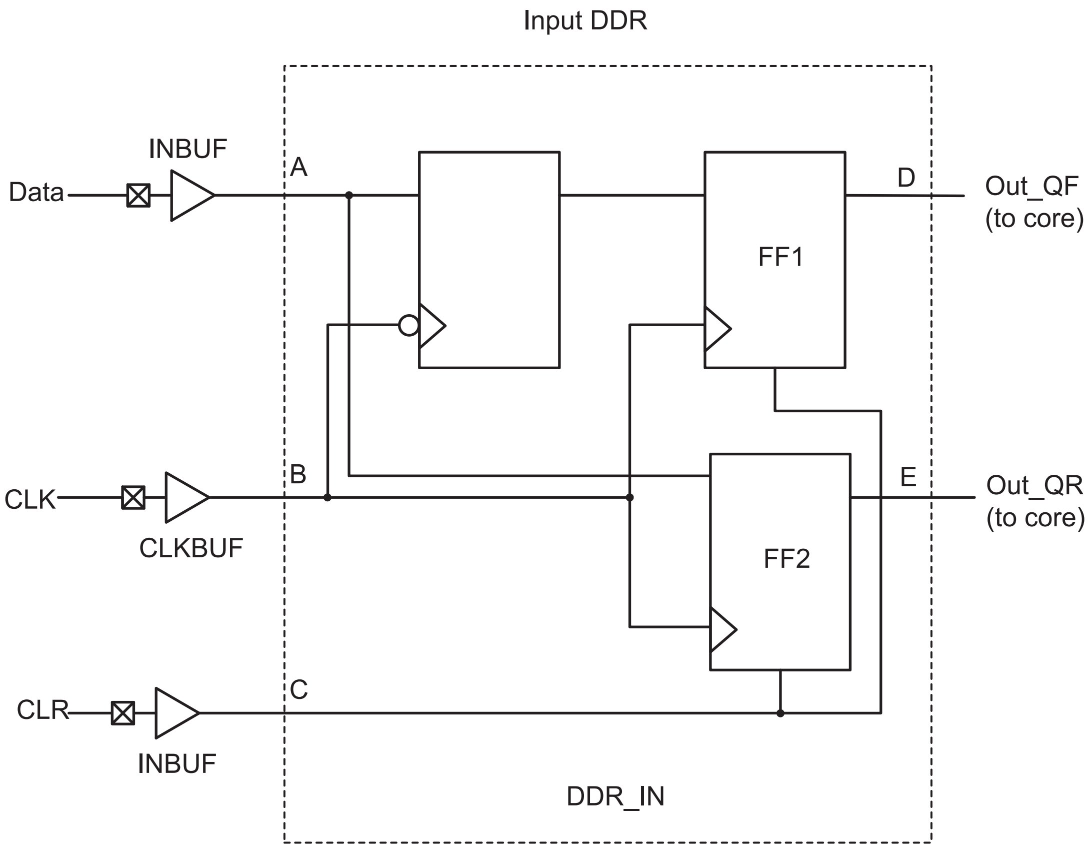

Figure 2-31 **• Input DDR Timing Model**

Table 2-129 **• Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

VersaTile Specifications as a Sequential Module

The IGLOOe library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

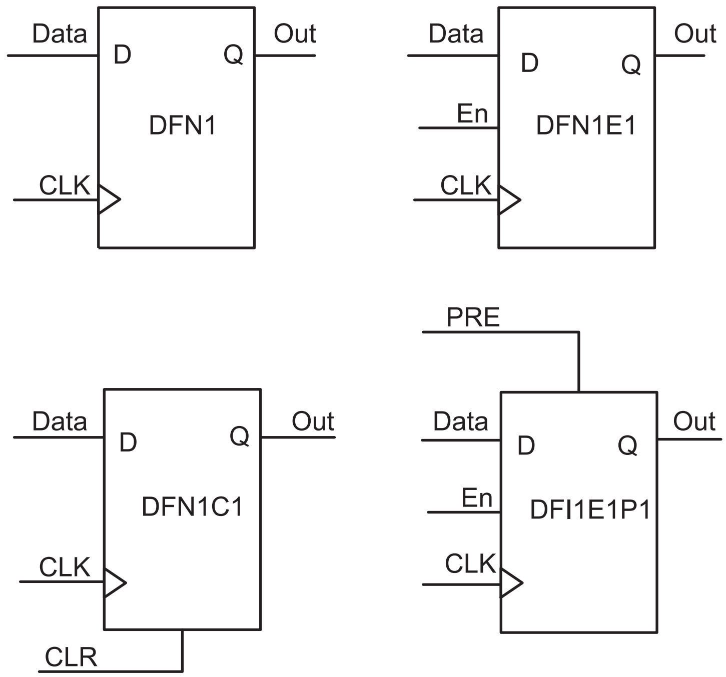

Figure 2-37 • **Sample of Sequential Cells**

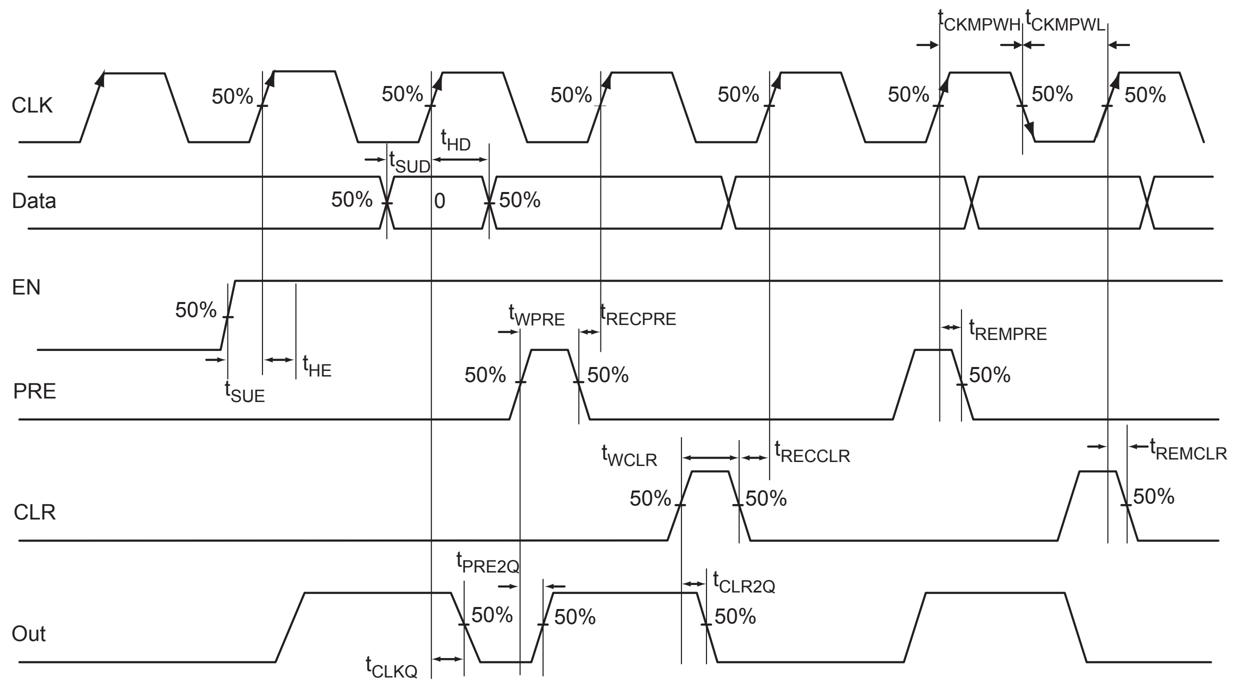

***Figure 2-38* • Timing Model and Waveforms**

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-137* • Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.89	ns
t_{SUD}	Data Setup Time for the Core Register	0.81	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.73	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.60	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.62	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.56	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.56	ns

Note: For specific junction temperature and voltage supply levels, refer to *Table 2-6 on page 2-6* *for derating values.*

1.2 V DC Core Voltage

Table 2-138 **• Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	1.61	ns
t_{SUD}	Data Setup Time for the Core Register	1.17	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	1.29	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.87	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.89	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.24	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.46	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.46	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.95	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.95	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-145 • RAM4K9
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{AS}	Address Setup Time	0.83	ns
t_{AH}	Address Hold Time	0.16	ns
t_{ENS}	REN, WEN Setup Time	0.81	ns
t_{ENH}	REN, WEN Hold Time	0.16	ns
t_{BKS}	BLK Setup Time	1.65	ns
t_{BKH}	BLK Hold Time	0.16	ns
t_{DS}	Input Data (DIN) Setup Time	0.71	ns
t_{DH}	Input Data (DIN) Hold Time	0.36	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DOUT (output retained, WMODE = 0)	3.53	ns
	Clock HIGH to New Data Valid on DOUT (flow-through, WMODE = 1)	3.06	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DOUT (pipelined)	1.81	ns
t_{C2CWWL}[1]	Address collision clk-to-clk delay for reliable write after write on same address; applicable to closing edge	0.23	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.35	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	0.41	ns
t_{RSTBQ}	RESET Low to Data Out Low on DOUT (flow-through)	2.06	ns
	RESET Low to Data Out Low on DOUT (pipelined)	2.06	ns
$t_{REMRSTB}$	RESET Removal	0.61	ns
$t_{RECRSTB}$	RESET Recovery	3.21	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.68	ns
t_{CYC}	Clock Cycle Time	6.24	ns
F_{MAX}	Maximum Frequency	160	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to* Table 2-6 on page 2-6 *for derating values.*

Timing Waveforms

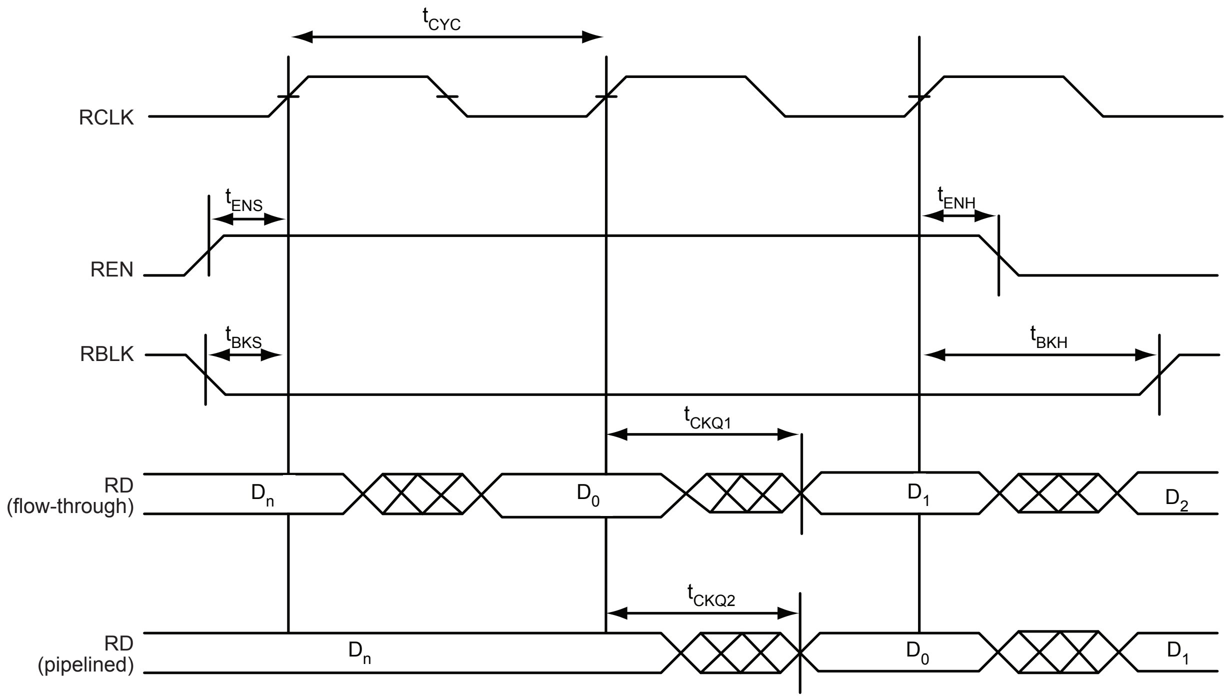

Figure 2-48 • **FIFO Read**

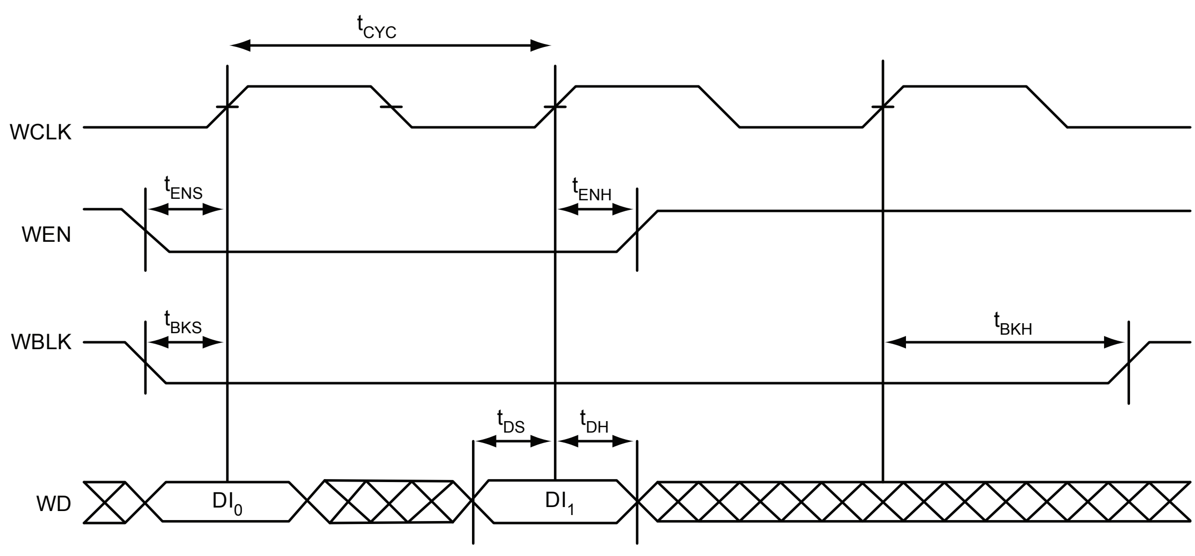

Figure 2-49 • **FIFO Write**

VCOMPLA/B/C/D/E/F PLL Ground

Ground to analog PLL power supplies. When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There are six VCOMPL pins (PLL ground) on IGLOOe devices.

VJTAG JTAG Supply Voltage

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

VPUMP Programming Supply Voltage

IGLOOe devices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

User-Defined Supply Pins

VREF I/O Voltage Reference

Reference voltage for I/O minibanks. VREF pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, can be designated the voltage reference I/O. Only certain I/O standards require a voltage reference—HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One VREF pin can support the number of I/Os available in its minibank.

FG896	
Pin Number	AGLE3000 Function
AK14	IO197PDB5V0
AK15	IO191NDB4V4
AK16	IO191PDB4V4
AK17	IO189NDB4V4
AK18	IO189PDB4V4
AK19	IO179PPB4V3
AK20	IO175NDB4V2
AK21	IO175PDB4V2
AK22	IO169NDB4V1
AK23	IO169PDB4V1
AK24	GND
AK25	IO167PPB4V1
AK26	GND
AK27	GDC2/IO156PPB4V0
AK28	GND
AK29	GND
B1	GND
B2	GND
B3	GAA2/IO309PPB7V4
B4	VCC
B5	IO14PPB0V1
B6	VCC
B7	IO07PPB0V0
B8	IO09PDB0V1
B9	IO15PPB0V1
B10	IO19NDB0V2
B11	IO19PDB0V2
B12	IO29NDB0V3
B13	IO29PDB0V3
B14	IO31PPB0V3
B15	IO37NDB0V4
B16	IO37PDB0V4
B17	IO41PDB1V0
B18	IO51NDB1V1
B19	IO59PDB1V2

FG896	
Pin Number	AGLE3000 Function
B20	IO53PDB1V1
B21	IO53NDB1V1
B22	IO61NDB1V2
B23	IO61PDB1V2
B24	IO69NPB1V3
B25	VCC
B26	GBC0/IO79NPB1V4
B27	VCC
B28	IO64NPB1V2
B29	GND
B30	GND
C1	GND
C2	IO309NPB7V4
C3	VCC
C4	GAA0/IO00NPB0V0
C5	VCCIB0
C6	IO03PDB0V0
C7	IO03NDB0V0
C8	GAB1/IO01PDB0V0
C9	IO05PDB0V0
C10	IO15NPB0V1
C11	IO25NDB0V3
C12	IO25PDB0V3
C13	IO31NPB0V3
C14	IO27NDB0V3
C15	IO39NDB0V4
C16	IO39PDB0V4
C17	IO55PPB1V1
C18	IO51PDB1V1
C19	IO59NDB1V2
C20	IO63NDB1V2
C21	IO63PDB1V2
C22	IO67NDB1V3
C23	IO67PDB1V3
C24	IO75NDB1V4

FG896	
Pin Number	AGLE3000 Function
C25	IO75PDB1V4
C26	VCCIB1
C27	IO64PPB1V2
C28	VCC
C29	GBA1/IO81PPB1V4
C30	GND
D1	IO303PPB7V3
D2	VCC
D3	IO305NPB7V3
D4	GND
D5	GAA1/IO00PPB0V0
D6	GAC1/IO02PDB0V0
D7	IO06NPB0V0
D8	GAB0/IO01NDB0V0
D9	IO05NDB0V0
D10	IO11NDB0V1
D11	IO11PDB0V1
D12	IO23NDB0V2
D13	IO23PDB0V2
D14	IO27PDB0V3
D15	IO40PDB0V4
D16	IO47NDB1V0
D17	IO47PDB1V0
D18	IO55NPB1V1
D19	IO65NDB1V3
D20	IO65PDB1V3
D21	IO71NDB1V3
D22	IO71PDB1V3
D23	IO73NDB1V4
D24	IO73PDB1V4
D25	IO74NDB1V4
D26	GBB0/IO80NPB1V4
D27	GND
D28	GBA0/IO81NPB1V4
D29	VCC

Revision	Changes	Page
Revision 6 (Feb 2009) Product Brief v1.3	The "Pro (Professional) I/O" section was revised to add two bullets regarding wide range power supply voltage support.	I
	3.0 V was added to the list of supported voltages in the "Pro I/Os with Advanced I/O Standards" section. The "Wide Range I/O Support" section is new.	1-7
Revision 5 (Oct 2008) Product Brief v1.2	The Quiescent Current values in Table 1 • IGLOOe Product Family table were updated.	I
Revision 4 (Jul 2008) Product Brief v1.1 DC and Switching Characteristics Advance v0.3	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A
Revision 3 (Jun 2008) DC and Switching Characteristics Advance v0.2	Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2 V I/O set. DDR Tables have two additional data points added to reflect both edges for Input DDR setup and hold time. The power data table has been updated to match SmartPower data rather then simulation values.	N/A
	Table 2-144 • IGLOOe CCC/PLL Specification was updated to add VMV to the VCCI parameter row and remove the word "output" from the parameter description for VCCI. Table note 3 was added.	2-92
	Table 2-2 • Recommended Operating Conditions 1 was updated to include the T_J parameter. Table note 9 is new.	2-2
	In Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature1, the maximum operating junction temperature was changed from 110° to 100°.	2-3
	VMV was removed from Table 2-4 • Overshoot and Undershoot Limits 1, 3. The title of the table was revised to remove "as measured on quiet I/Os." Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted.	2-3
	The "PLL Behavior at Brownout Condition" section is new.	2-4
	Figure 2-2 • V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels is new.	2-5
	EQ 2 was updated. The temperature was changed to 100°C, and therefore the end result changed.	2-6
	The table notes for Table 2-9 • Quiescent Supply Current (IDD), IGLOOe Flash*Freeze Mode*, Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOOe Sleep Mode*, and Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOOe Shutdown Mode* were updated to remove VMV and include PDC6 and PDC7. VCCI and VJTAG were removed from the statement about IDD in the table note for Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOOe Shutdown Mode*.	2-7
	Note 2 of Table 2-12 • Quiescent Supply Current (IDD) Characteristics, No Flash*Freeze Mode1 was updated to include VCCPLL. Note 4 was updated to include PDC6 and PDC7.	2-8
	Table note 3 was added to Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings and referenced for 1.2 V LVCMOS.	2-9

Revision	Changes	Page
Revision 3 (cont'd)	Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings1 was updated to change PDC3 to PDC7. The table notes were updated to reflect that power was measured on VCCI. Table note 4 is new.	2-10
	Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO Devices and Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO Devices were updated to add PDC6 and PDC7, and to change the definition for PDC5 to bank quiescent power.	2-11, 2-12
	A table subtitle was added for Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO Devices.	2-12
	The "Total Static Power Consumption—PSTAT" section was updated to revise the calculation of P_{STAT}, including PDC6 and PDC7.	2-13
	Footnote 1 was updated to include information about P_{AC13}. The PLL Contribution equation was changed from: $P_{PLL} = P_{AC13} + P_{AC14}$ * FCLKOUT to PPLL = $P_{DC4} + P_{AC13}$ * F_{CLKOUT}.	2-14
	The "Timing Model" was updated to be consistent with the revised timing numbers.	2-16
	In Table 2-22 • Summary of Maximum and Minimum DC Input Levels, T_J was changed to T_A in notes 1 and 2.	2-22
	Table 2-22 • Summary of Maximum and Minimum DC Input Levels was updated to included a hysteresis value for 1.2 V LVCMOS (Schmitt trigger mode).	2-22
	All AC Loading figures for single-ended I/O standards were changed from Datapaths at 35 pF to 5 pF.	N/A
	The "1.2 V LVCMOS (JESD8-12A)" section is new.	2-47
Revision 2 (Jun 2008) Product Brief v1.0	The product brief section of the datasheet was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.	N/A
Revision 2 (cont'd) Packaging v1.1	The naming conventions changed for the following pins in the "FG484" for the A3GLE600: Pin Number — New Function Name J19 — IO45PPB2V1 K20 — IO45NPB2V1 M2 — IO114NPB6V1 N1 — IO114PPB6V1 N4 — GFC2/IO115PPB6V1 P3 — IO115NPB6V1	4-6
Revision 1 (Mar 2008) Product Brief rev. 1	The "Low Power" section was updated to change "1.2 V and 1.5 V Core Voltage" to "1.2 V and 1.5 V Core and I/O Voltage." The text "(from 25 µW)" was removed from "Low Power Active FPGA Operation." 1.2_V was added to the list of core and I/O voltages in the "Pro (Professional) I/O" and "Pro I/Os with Advanced I/O Standards" section sections.	I I, 1-7
Revision 0 (Jan 2008)	This document was previously in datasheet Advance v0.4. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is 51700096-001-0.	N/A