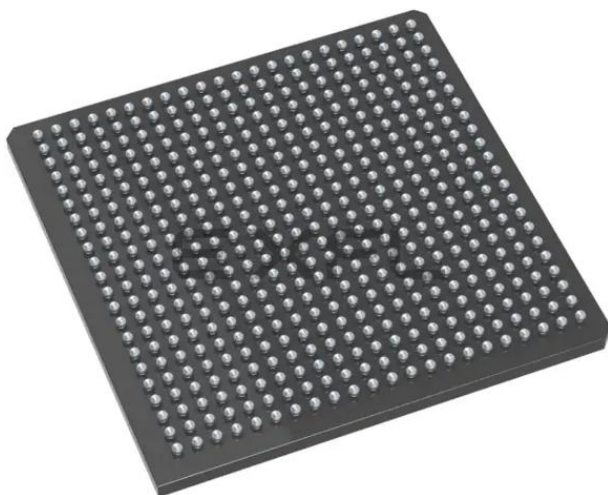




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	75264
Total RAM Bits	516096
Number of I/O	341
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agle3000v5-fg484

I/Os Per Package ¹

IGLOOe Devices	AGLE600		AGLE3000	
ARM-Enabled IGLOOe Devices			M1AGLE3000	
Package	I/O Types			
	Single-Ended I/O ¹	Differential I/O Pairs	Single-Ended I/O ¹	Differential I/O Pairs
FG256	165	79	–	–
FG484	270	135	341	168
FG896	–	–	620	310

Notes:

- When considering migrating your design to a lower- or higher-density device, refer to the [IGLOOe FPGA Fabric User's Guide](#) to ensure compliance with design and board migration requirements.
- Each used differential I/O pair reduces the number of single-ended I/Os available by two.
- For AGL3000 devices, the usage of certain I/O standards is limited as follows:
 - SSTL3(I) and (II): up to 40 I/Os per north or south bank
 - LVPECL / GTL+ 3.3 V / GTL 3.3 V: up to 48 I/Os per north or south bank
 - SSTL2(I) and (II) / GTL+ 2.5 V / GTL 2.5 V: up to 72 I/Os per north or south bank
- FG256 and FG484 are footprint-compatible packages.
- When using voltage-referenced I/O standards, one I/O pin should be assigned as a voltage-referenced pin (VREF) per minibank (group of I/Os).
- When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not as a regular I/O, the number of single-ended user I/Os available is reduced by one.
- "G" indicates RoHS-compliant packages. Refer to ["IGLOOe Ordering Information"](#) on page III for the location of the "G" in the part number.

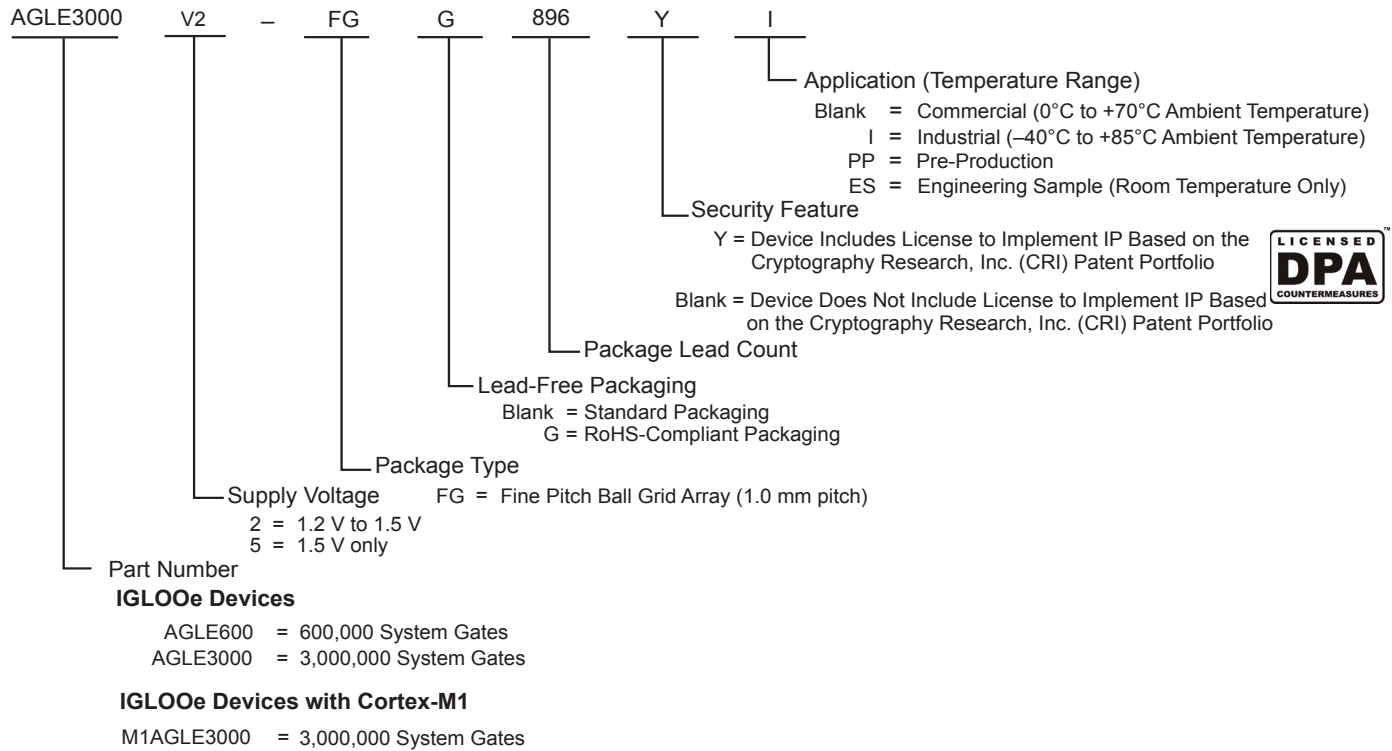
IGLOOe FPGAs Package Sizes Dimensions

Package	FG256	FG484	FG896
Length × Width (mm × mm)	17 × 17	23 × 23	31 × 31
Nominal Area (mm ²)	289	529	961
Pitch (mm)	1	1	1
Height (mm)	1.6	2.23	2.23

IGLOOe Device Status

IGLOOe Devices	Status	M1 IGLOOe Devices	Status
AGLE600	Production		
AGLE3000	Production	M1AGLE3000	Production

IGLOOe Ordering Information



Note: Marking Information: IGLOO V2 devices do not have V2 marking, but IGLOO V5 devices are marked accordingly.

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Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja} . The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 100°C. EQ 2 shows a sample calculation of the absolute maximum power dissipation allowed for an 896-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (}^{\circ}\text{C)} - \text{Max. ambient temp. (}^{\circ}\text{C)}}{\theta_{ja} (^{\circ}\text{C/W)}} = \frac{100^{\circ}\text{C} - 70^{\circ}\text{C}}{13.6^{\circ}\text{C/W}} = 2.206 \text{ W}$$

EQ 2

Table 2-5 • Package Thermal Resistivities

Package Type	Pin Count	θ_{jc}	θ_{ja}			Units
			Still Air	200 ft./min.	500 ft./min.	
Plastic Quad Flat Package (PQFP)	208	8.0	26.1	22.5	20.8	C/W
Plastic Quad Flat Package (PQFP) with embedded heat spreader	208	3.8	16.2	13.3	11.9	C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.9	22.8	21.5	C/W
	484	3.2	20.5	17.0	15.9	C/W
	676	3.2	16.4	13.0	12.0	C/W
	896	2.4	13.6	10.4	9.4	C/W

Temperature and Voltage Derating Factors

Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays
(normalized to $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.425 \text{ V}$)
For IGLOOe V2 or V5 devices, 1.5 V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature ($^{\circ}\text{C}$)					
	-40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.945	0.965	0.978	1.000	1.008	1.013
1.500	0.876	0.893	0.906	0.927	0.934	0.940
1.575	0.824	0.840	0.852	0.872	0.879	0.884

Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays
(normalized to $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.14 \text{ V}$)
For IGLOOe V2, 1.2 V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature ($^{\circ}\text{C}$)					
	-40°C	0°C	25°C	70°C	85°C	100°C
1.14	0.968	0.978	0.991	1.000	1.006	1.010
1.20	0.864	0.873	0.885	0.893	0.898	0.902
1.26	0.793	0.803	0.813	0.821	0.826	0.829

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in [Table 2-19 on page 2-15](#).
- Enable rates of output buffers—guidelines are provided for typical applications in [Table 2-20 on page 2-15](#).
- Read rate and write rate to the memory—guidelines are provided for typical applications in [Table 2-20 on page 2-15](#). The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption— P_{TOTAL}

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption— P_{STAT}

$$P_{STAT} = (PDC1 \text{ or } PDC2 \text{ or } PDC3) + N_{BANKS} * PDC5 + N_{INPUTS} * PDC6 + N_{OUTPUTS} * PDC7$$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{BANKS} is the number of I/O banks powered in the design.

Total Dynamic Power Consumption— P_{DYN}

$$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$$

Global Clock Contribution— P_{CLOCK}

$$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S-CELL} * PAC4) * F_{CLK}$$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *IGLOOe FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *IGLOOe FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

Sequential Cells Contribution— P_{S-CELL}

$$P_{S-CELL} = N_{S-CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-19 on page 2-15](#).

F_{CLK} is the global clock signal frequency.

Table 2-28 • I/O Output Buffer Maximum Resistances¹ (continued)

Standard	Drive Strength	R _{PULL-DOWN} (Ω) ²	R _{PULL-UP} (Ω) ³
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75
3.3 V GTL	20 mA ⁵	11	—
2.5 V GTL	20 mA ⁵	14	—
3.3 V GTL+	35 mA	12	—
2.5 V GTL+	33 mA	15	—
HSTL (I)	8 mA	50	50
HSTL (II)	15 mA	25	25
SSTL2 (I)	15 mA	27	31
SSTL2 (II)	18 mA	13	15
SSTL3 (I)	14 mA	44	69
SSTL3 (II)	21 mA	18	32

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website at <http://www.microsemi.com/soc/techdocs/models/ibis.html>.
2. $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / IOL_{spec}$
3. $R_{(PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / IOH_{spec}$
4. Applicable to IGLOOe V2 devices operating in the 1.2 V core range ONLY.
5. Output drive strength is below JEDEC specification.

**Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values**

VCCI	R _(WEAK PULL-UP) ¹ (Ω)		R _(WEAK PULL-DOWN) ² (Ω)	
	Minimum	Maximum	Minimum	Maximum
3.3 V	10 k	45 k	10 k	45 k
3.3 V (wide range I/Os)	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k
1.2 V	25 k	110 k	25 k	150 k
1.2 V (wide range I/Os)	19 k	110 k	19 k	150 k

Notes:

1. $R_{(WEAK PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / I_{(WEAK PULL-UP-MIN)}$
2. $R_{(WEAK PULL-DOWN-MAX)} = (VOL_{spec}) / I_{(WEAK PULL-DOWN-MIN)}$

1.2 V DC Core Voltage

Table 2-38 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.55	5.54	0.26	1.31	1.58	1.10	5.63	4.53	2.79	2.87	11.42	10.32	ns
8 mA	Std.	1.55	4.60	0.26	1.31	1.58	1.10	4.67	3.94	3.09	3.45	10.45	9.73	ns
12 mA	Std.	1.55	3.93	0.26	1.31	1.58	1.10	3.99	3.51	3.28	3.82	9.77	9.29	ns
16 mA	Std.	1.55	3.74	0.26	1.31	1.58	1.10	3.79	3.41	3.32	3.92	9.58	9.20	ns
24 mA	Std.	1.55	3.64	0.26	1.31	1.58	1.10	3.69	3.42	3.38	4.30	9.48	9.21	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-39 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.55	3.26	0.26	1.31	1.58	1.10	3.33	2.67	2.79	3.01	9.12	8.46	ns
8 mA	Std.	1.55	2.77	0.26	1.31	1.58	1.10	2.80	2.24	3.09	3.59	8.59	8.03	ns
12 mA	Std.	1.55	2.47	0.26	1.31	1.58	1.10	2.51	2.04	3.28	3.97	8.29	7.82	ns
16 mA	Std.	1.55	2.42	0.26	1.31	1.58	1.10	2.46	2.00	3.33	4.08	8.24	7.79	ns
24 mA	Std.	1.55	2.45	0.26	1.31	1.58	1.10	2.48	1.95	3.38	4.46	8.26	7.73	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

3.3 V LVCMOS Wide Range

Table 2-40 • Minimum and Maximum DC Input and Output Levels

3.3 V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Equivalent Software Default Drive Strength Option ³	Min. (V)	Max. (V)	Min. (V)	Max. (V)	Max. (V)	Min. (V)	μA	μA	Max. (mA) ⁴	Max. (mA) ⁴	μA ⁵	μA ⁵
100 μA	2 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	25	27	10	10
100 μA	4 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	25	27	10	10
100 μA	6 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	51	54	10	10
100 μA	8 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	51	54	10	10
100 μA	12 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	103	109	10	10
100 μA	16 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	132	127	10	10
100 μA	24 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	268	181	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
4. Currents are measured at 85°C junction temperature.
5. All LVCMOS 3.3 V software macros supports LVCMOS 3.3 V wide range as specified in the JDEC8a specification.
6. Software default selection highlighted in gray.

Table 2-41 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)
0	3.3	1.4	—	5

Note: *Measuring point = V_{trip} . See Table 2-23 on page 2-23 for a complete table of trip points.

1.2 V DC Core Voltage

Table 2-44 • 3.3 V LVC MOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	4 mA	Std.	1.55	8.14	0.26	1.66	2.14	1.10	8.14	6.46	3.80	3.79	13.93	12.25	ns
100 μA	8 mA	Std.	1.55	6.68	0.26	1.66	2.14	1.10	6.68	5.57	4.25	4.69	12.47	11.36	ns
100 μA	12 mA	Std.	1.55	5.65	0.26	1.66	2.14	1.10	5.65	4.91	4.55	5.25	11.44	10.69	ns
100 μA	16 mA	Std.	1.55	5.36	0.26	1.66	2.14	1.10	5.36	4.76	4.61	5.41	11.14	10.55	ns
100 μA	24 mA	Std.	1.55	5.20	0.26	1.66	2.14	1.10	5.20	4.78	4.69	6.00	10.99	10.56	ns

Notes:

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-45 • 3.3 V LVC MOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	4 mA	Std.	1.55	4.65	0.26	1.66	2.14	1.10	4.65	3.64	3.80	4.00	10.44	9.43	ns
100 μA	8 mA	Std.	1.55	3.85	0.26	1.66	2.14	1.10	3.85	2.99	4.25	4.91	9.64	8.77	ns
100 μA	12 mA	Std.	1.55	3.40	0.26	1.66	2.14	1.10	3.40	2.68	4.55	5.49	9.19	8.46	ns
100 μA	16 mA	Std.	1.55	3.33	0.26	1.66	2.14	1.10	3.33	2.62	4.62	5.65	9.11	8.41	ns
100 μA	24 mA	Std.	1.55	3.36	0.26	1.66	2.14	1.10	3.36	2.54	4.71	6.24	9.15	8.32	ns

Notes:

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.
3. Software default selection highlighted in gray.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-48 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Unit
4 mA	Std.	0.97	5.55	0.18	1.31	1.41	0.66	5.66	4.75	2.28	1.96	9.26	8.34	ns
8 mA	Std.	0.97	4.58	0.18	1.31	1.41	0.66	4.67	4.07	2.58	2.53	8.27	7.66	ns
12 mA	Std.	0.97	3.89	0.18	1.31	1.41	0.66	3.97	3.58	2.78	2.91	7.56	7.17	ns
16 mA	Std.	0.97	3.68	0.18	1.31	1.41	0.66	3.75	3.47	2.82	3.01	7.35	7.06	ns
24 mA	Std.	0.97	3.59	0.18	1.31	1.41	0.66	3.66	3.48	2.88	3.37	7.26	7.08	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-49 • 2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Unit
4 mA	Std.	0.97	2.94	0.18	1.31	1.41	0.66	3.00	2.68	2.28	2.03	6.60	6.27	ns
8 mA	Std.	0.97	2.45	0.18	1.31	1.41	0.66	2.50	2.12	2.58	2.62	6.10	5.72	ns
12 mA	Std.	0.97	2.15	0.18	1.31	1.41	0.66	2.20	1.85	2.78	2.98	5.80	5.45	ns
16 mA	Std.	0.97	2.10	0.18	1.31	1.41	0.66	2.15	1.80	2.82	3.08	5.75	5.40	ns
24 mA	Std.	0.97	2.11	0.18	1.31	1.41	0.66	2.16	1.74	2.88	3.47	5.75	5.33	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Timing Characteristics

1.2 V DC Core Voltage

Table 2-66 • 1.2 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 1.14\text{ V}$

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	9.92	0.26	2.09	2.95	1.10	9.53	7.48	4.02	3.67	15.31	13.26	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

Table 2-67 • 1.2 LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 1.14\text{ V}$

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	4.06	0.26	2.09	2.95	1.10	3.92	3.46	4.01	3.79	9.71	9.24	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.

1.2 V LVCMOS Wide Range

Table 2-68 • Minimum and Maximum DC Input and Output Levels

1.2 V LVCMOS Wide Range ¹		VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ²	IIH ³
Drive Strength	Equivalent Software Default Drive Strength Option ⁴	Min. (V)	Max. (V)	Min. (V)	Max (V)	Max. (V)	Min. (V)	μA	μA	Max. (mA) ⁵	Max. (mA) ⁵	μA ⁶	μA ⁶
100 μA	2 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	$0.25 * V_{CCI}$	$0.75 * V_{CCI}$	100	100	20	26	10	10

Notes:

1. Applicable to V2 devices ONLY.
2. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
3. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
4. The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
5. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
6. Currents are measured at 85°C junction temperature.
7. Software default selection highlighted in gray.

Timing Characteristics

Refer to LVCMOS 1.2 V (normal range) "Timing Characteristics" on [page 2-48](#) for worst-case timing.

Table 2-121 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{iCLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{iSUD}	Data Setup Time for the Input Data Register	C, A
t_{iHD}	Data Hold Time for the Input Data Register	C, A
t_{iSUE}	Enable Setup Time for the Input Data Register	B, A
t_{iHE}	Enable Hold Time for the Input Data Register	B, A
t_{iPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{iREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{iRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

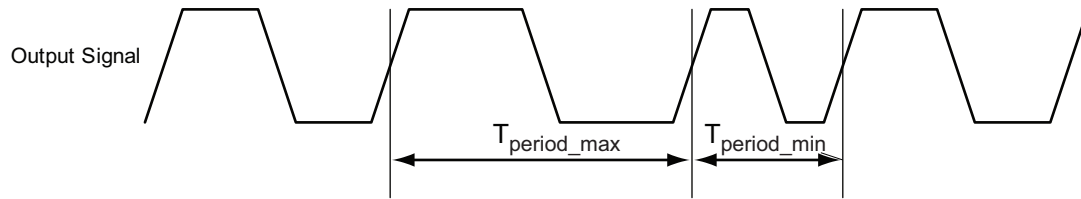
Note: See Figure 2-26 on page 2-66 for more information.

1.2 V DC Core Voltage

Table 2-128 • Output Enable Register Propagation Delays
 Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	1.10	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	1.15	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	1.22	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.65	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.65	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
t_{OEWPPE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-6](#) for derating values.



Note: Peak-to-peak jitter measurements are defined by $T_{\text{peak-to-peak}} = T_{\text{period_max}} - T_{\text{period_min}}$.

Figure 2-40 • Peak-to-Peak Jitter Definition

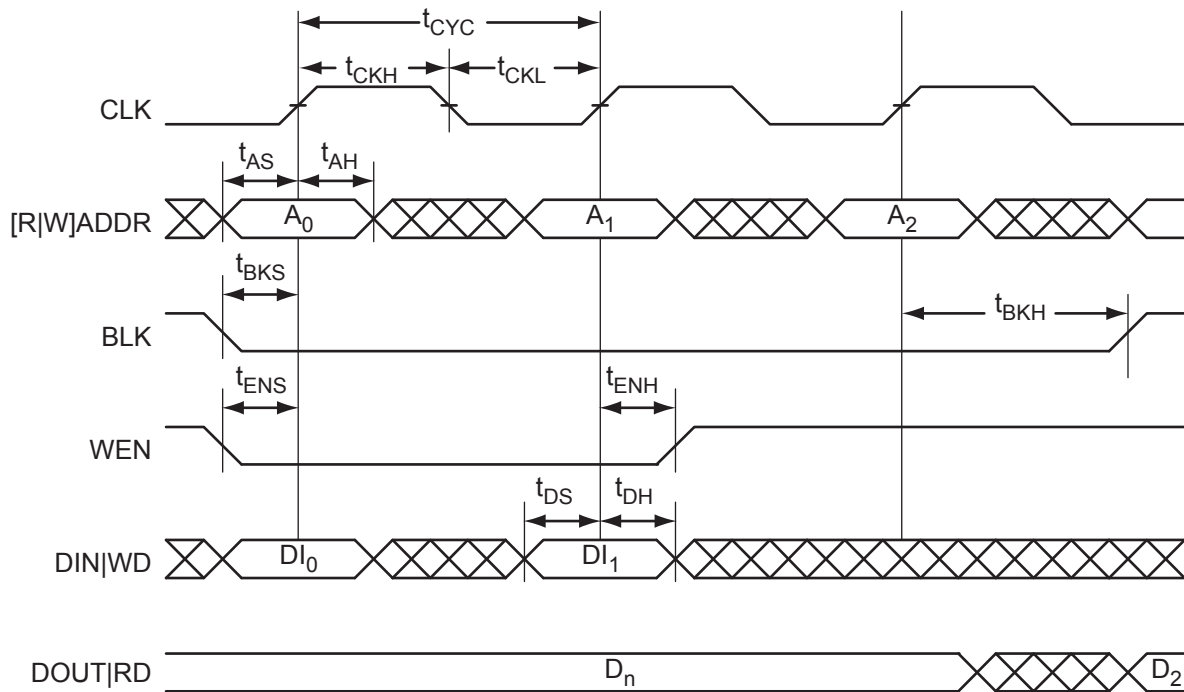


Figure 2-44 • RAM Write, Output Retained. Applicable to both RAM4K9 and RAM512X18.

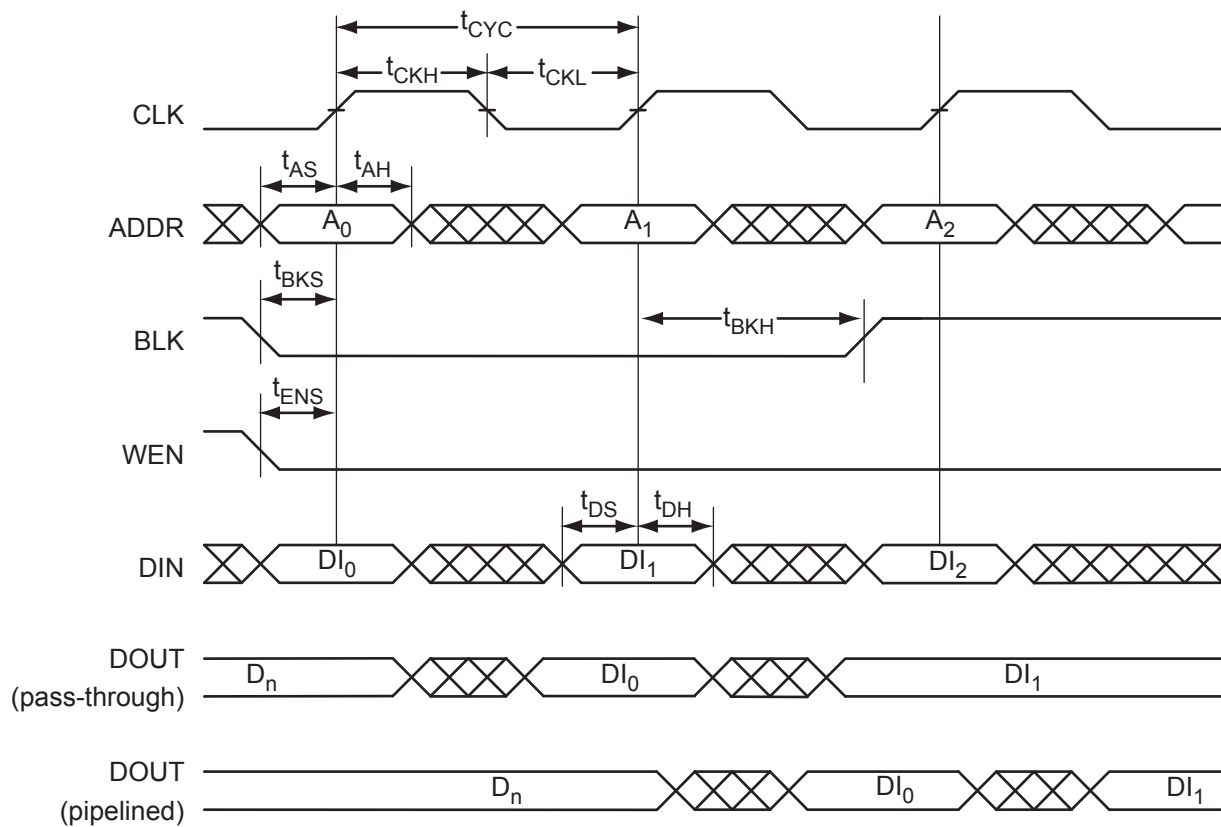


Figure 2-45 • RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 Only.

FG896	
Pin Number	AGLE3000 Function
D30	GBA2/IO82PPB2V0
E1	GND
E2	IO303NPB7V3
E3	VCCIB7
E4	IO305PPB7V3
E5	VCC
E6	GAC0/IO02NDB0V0
E7	VCCIB0
E8	IO06PPB0V0
E9	IO24NDB0V2
E10	IO24PDB0V2
E11	IO13NDB0V1
E12	IO13PDB0V1
E13	IO34NDB0V4
E14	IO34PDB0V4
E15	IO40NDB0V4
E16	IO49NDB1V1
E17	IO49PDB1V1
E18	IO50PDB1V1
E19	IO58PDB1V2
E20	IO60NDB1V2
E21	IO77PDB1V4
E22	IO68NDB1V3
E23	IO68PDB1V3
E24	VCCIB1
E25	IO74PDB1V4
E26	VCC
E27	GBB1/IO80PPB1V4
E28	VCCIB2
E29	IO82NPB2V0
E30	GND
F1	IO296PPB7V2
F2	VCC
F3	IO306PDB7V4
F4	IO297PDB7V2

FG896	
Pin Number	AGLE3000 Function
F5	VMV7
F5	VMV7
F6	GND
F7	GNDQ
F8	IO12NDB0V1
F9	IO12PDB0V1
F10	IO10PDB0V1
F11	IO16PDB0V1
F12	IO22NDB0V2
F13	IO30NDB0V3
F14	IO30PDB0V3
F15	IO36PDB0V4
F16	IO48NDB1V0
F17	IO48PDB1V0
F18	IO50NDB1V1
F19	IO58NDB1V2
F20	IO60PDB1V2
F21	IO77NDB1V4
F22	IO72NDB1V3
F23	IO72PDB1V3
F24	GNDQ
F25	GND
F26	VMV2
F26	VMV2
F27	IO86PDB2V0
F28	IO92PDB2V1
F29	VCC
F30	IO100NPB2V2
G1	GND
G2	IO296NPB7V2
G3	IO306NDB7V4
G4	IO297NDB7V2
G5	VCCIB7
G6	GNDQ
G6	GNDQ

FG896	
Pin Number	AGLE3000 Function
G7	VCC
G8	VMV0
G9	VCCIB0
G10	IO10NDB0V1
G11	IO16NDB0V1
G12	IO22PDB0V2
G13	IO26PPB0V3
G14	IO38NPB0V4
G15	IO36NDB0V4
G16	IO46NDB1V0
G17	IO46PDB1V0
G18	IO56NDB1V1
G19	IO56PDB1V1
G20	IO66NDB1V3
G21	IO66PDB1V3
G22	VCCIB1
G23	VMV1
G24	VCC
G25	GNDQ
G25	GNDQ
G26	VCCIB2
G27	IO86NDB2V0
G28	IO92NDB2V1
G29	IO100PPB2V2
G30	GND
H1	IO294PDB7V2
H2	IO294NDB7V2
H3	IO300NDB7V3
H4	IO300PDB7V3
H5	IO295PDB7V2
H6	IO299PDB7V3
H7	VCOMPLA
H8	GND
H9	IO08NDB0V0
H10	IO08PDB0V0

FG896	
Pin Number	AGLE3000 Function
L26	IO87NDB2V0
L27	IO97PDB2V1
L28	IO101PDB2V2
L29	IO103PDB2V2
L30	IO119NDB3V0
M1	IO282NDB7V1
M2	IO282PDB7V1
M3	IO292NDB7V2
M4	IO292PDB7V2
M5	IO283NDB7V1
M6	IO285PDB7V1
M7	IO287PDB7V1
M8	IO289PDB7V1
M9	IO289NDB7V1
M10	VCCIB7
M11	VCC
M12	GND
M13	GND
M14	GND
M15	GND
M16	GND
M17	GND
M18	GND
M19	GND
M20	VCC
M21	VCCIB2
M22	NC
M23	IO104PPB2V2
M24	IO102PDB2V2
M25	IO102NDB2V2
M26	IO95PDB2V1
M27	IO97NDB2V1
M28	IO101NDB2V2
M29	IO103NDB2V2
M30	IO119PDB3V0

FG896	
Pin Number	AGLE3000 Function
N1	IO276PDB7V0
N2	IO278PDB7V0
N3	IO280PDB7V0
N4	IO284PDB7V1
N5	IO279PDB7V0
N6	IO285NDB7V1
N7	IO287NDB7V1
N8	IO281NDB7V0
N9	IO281PDB7V0
N10	VCCIB7
N11	VCC
N12	GND
N13	GND
N14	GND
N15	GND
N16	GND
N17	GND
N18	GND
N19	GND
N20	VCC
N21	VCCIB2
N22	IO106NDB2V3
N23	IO106PDB2V3
N24	IO108PDB2V3
N25	IO108NDB2V3
N26	IO95NDB2V1
N27	IO99NDB2V2
N28	IO99PDB2V2
N29	IO107PDB2V3
N30	IO107NDB2V3
P1	IO276NDB7V0
P2	IO278NDB7V0
P3	IO280NDB7V0
P4	IO284NDB7V1
P5	IO279NDB7V0

FG896	
Pin Number	AGLE3000 Function
P6	GFC1/IO275PDB7V0
P7	GFC0/IO275NDB7V0
P8	IO277PDB7V0
P9	IO277NDB7V0
P10	VCCIB7
P11	VCC
P12	GND
P13	GND
P14	GND
P15	GND
P16	GND
P17	GND
P18	GND
P19	GND
P20	VCC
P21	VCCIB2
P22	GCC1/IO112PDB2V3
P23	IO110PDB2V3
P24	IO110NDB2V3
P25	IO109PPB2V3
P26	IO111NPB2V3
P27	IO105PDB2V2
P28	IO105NDB2V2
P29	GCC2/IO117PDB3V0
P30	IO117NDB3V0
R1	GFC2/IO270PDB6V4
R2	GFB1/IO274PPB7V0
R3	VCOMPLF
R4	GFA0/IO273NDB6V4
R5	GFB0/IO274NPB7V0
R6	IO271NDB6V4
R7	GFB2/IO271PDB6V4
R8	IO269PDB6V4
R9	IO269NDB6V4
R10	VCCIB7

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the IGLOOe datasheet.

Revision	Changes	Page
Revision 13 (December 2012)	The "IGLOOe Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43176). Also added the missing heading 'Supply Voltage' under V2.	III
	The note in Table 2-143 • IGLOOe CCC/PLL Specification and Table 2-144 • IGLOOe CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42568).	2-91, 2-92
	Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 12 (September 2012)	The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data.	1-2
	Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40272).	N/A
Revision 11 (August 2012)	The drive strength, IOL, and IOH value for 3.3 V GTL and 2.5 V GTL was changed from 25 mA to 20 mA in the following tables (SAR 37180): Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels , Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings Table 2-28 • I/O Output Buffer Maximum Resistances ¹ Table 2-73 • Minimum and Maximum DC Input and Output Levels Table 2-77 • Minimum and Maximum DC Input and Output Levels Also added note stating "Output drive strength is below JEDEC specification." for Tables 2-25, 2-26, and 2-28. Additionally, the IOL and IOH values for 3.3 V GTL+ and 2.5 V GTL+ were corrected from 51 to 35 (for 3.3 V GTL+) and from 40 to 33 (for 2.5 V GTL+) in table Table 2-21 (SAR 39713).	2-20 2-25 2-26 2-28 2-51 2-53
	In Table 2-117 • Minimum and Maximum DC Input and Output Levels , VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 37183).	2-65
	The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions and Packaging" section: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38318). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1

Revision	Changes	Page
Revision 9 (continued)	The example in the paragraph above Table 2-31 • Duration of Short Circuit Event before Failure was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 32287).	2-31
	The notes regarding drive strength in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section, "3.3 V LVCMOS Wide Range" section and "1.2 V LVCMOS Wide Range" section tables were revised for clarification. They now state that the minimum drive strength for the default software configuration when run in wide range is $\pm 100 \mu\text{A}$. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 34766).	2-23, 2-35, 2-48
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34886).	2-32
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34793): "It uses a 5 V–tolerant input buffer and push-pull output buffer."	2-38
	Table 2-143 • IGLOOe CCC/PLL Specification and Table 2-144 • IGLOOe CCC/PLL Specification were updated. A note was added to both tables indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34818).	2-91, 2-92
	The following figures were deleted. Reference was made to a new application note, Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs , which covers these cases in detail (SAR 34869). Figure 2-46 • Write Access after Write onto Same Address Figure 2-47 • Read Access after Write onto Same Address Figure 2-48 • Write Access after Read onto Same Address The port names in the SRAM "Timing Waveforms" , SRAM "Timing Characteristics" tables, Figure 2-50 • FIFO Reset , and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 35749).	2-95, 2-98, 2-104, 2-106
	The "Pin Descriptions and Packaging" chapter is new (SAR 34768).	3-1
	Package names used in the "Package Pin Assignments" section were revised to match standards given in Package Mechanical Drawings (SAR 34768)	4-1
July 2010	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "IGLOOe Device Status" table on page II indicates the status for each device in the device family.	N/A