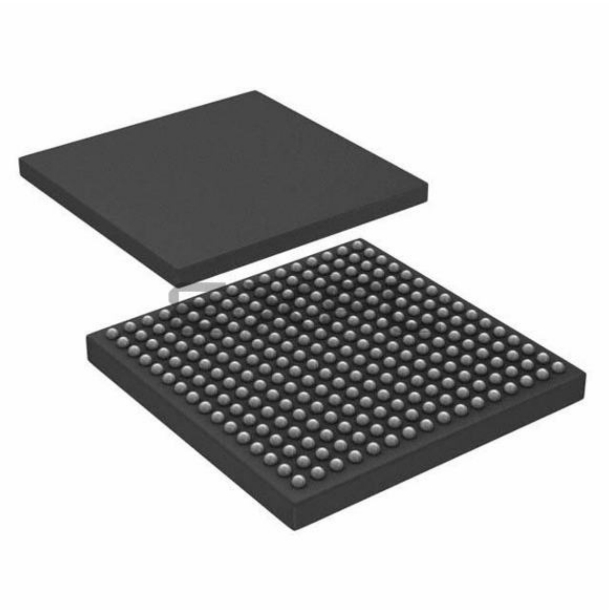

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 13824 |
| Total RAM Bits | 110592 |
| Number of I/O | 165 |
| Number of Gates | 600000 |
| Voltage - Supply | 1.14V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/agle600v2-fg256 |

## Flash Advantages

### Low Power

Flash-based IGLOOe devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOOe devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOOe devices also have low dynamic power consumption to further maximize power savings; power is even further reduced by the use of a 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, gives the IGLOOe device the lowest total system power offered by any FPGA.

### Security

The nonvolatile, flash-based IGLOOe devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOOe devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOOe devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of protection in the FPGA industry for programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOOe devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOOe devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOOe devices with AES-based security provide a high level of protection for remote field updates over public networks such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of the IGLOOe family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The IGLOOe family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. An IGLOOe device provides the best available security for programmable logic designs.

### Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOOe FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

### Instant On

Flash-based IGLOOe devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based IGLOOe devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOOe device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOOe devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

### *Pro I/Os with Advanced I/O Standards*

The IGLOOe family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V). IGLOOe FPGAs support 19 different I/O standards, including single-ended, differential, and voltage-referenced. The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported. Each I/O bank is subdivided into VREF minibanks, which are used by voltage-referenced I/Os. VREF minibanks contain 8 to 18 I/Os. All the I/Os in a given minibank share a common VREF line. Therefore, if any I/O in a given VREF minibank is configured as a VREF pin, the remaining I/Os in that minibank will be able to use that reference voltage.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications (e.g., PCI 66 MHz, bidirectional SSTL 2 and 3, Class I and II)
- Double-Data-Rate applications (e.g., DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications, and DDR 200 MHz SRAM using bidirectional HSTL Class II).

IGLOOe banks support M-LVDS with 20 multi-drop points.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

## Wide Range I/O Support

IGLOOe devices support JEDEC-defined wide range I/O operation. IGLOOe devices support both the JESD8-B specification, covering 3.0 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

## Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

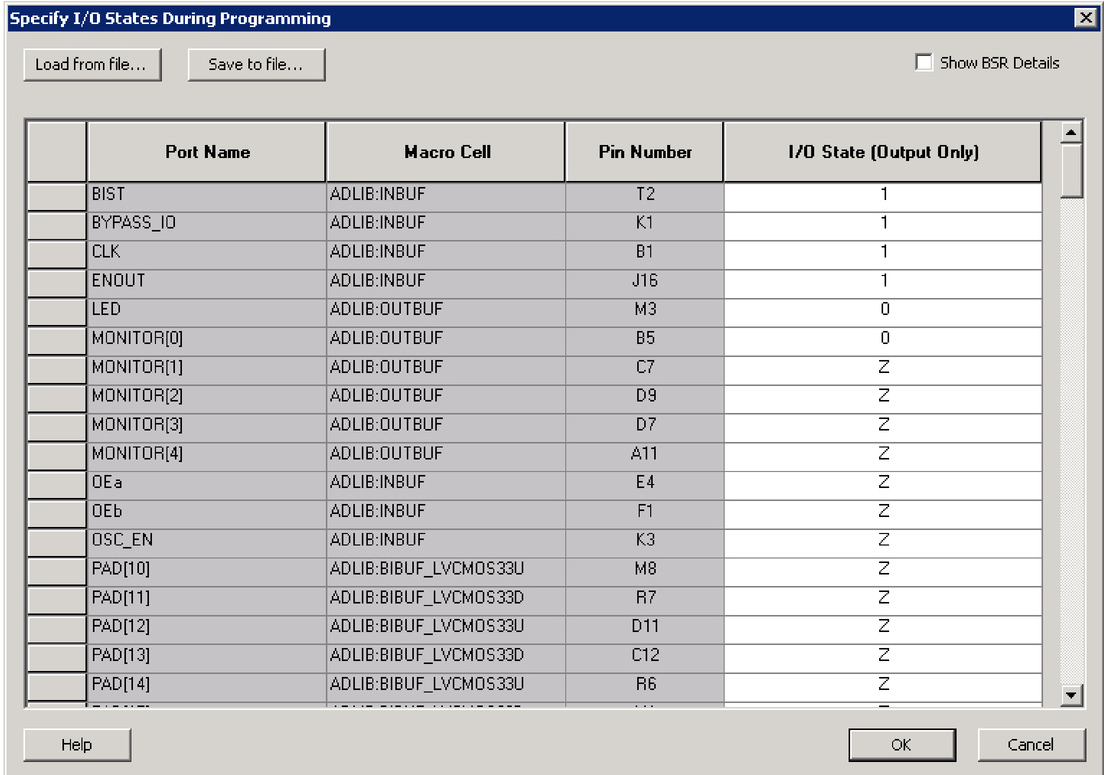
1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click **PDB Configuration**. A FlashPoint – Programming File Generator window appears.
3. Click the **Specify I/O States During Programming** button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-4 on page 1-8).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

   Z -Tri-State: I/O is tristated




| | Port Name | Macro Cell | Pin Number | I/O State (Output Only) |
|---|---|---|---|---|
| | BIST | ADLIB:INBUF | T2 | 1 |
| | BYPASS_IO | ADLIB:INBUF | K1 | 1 |
| | CLK | ADLIB:INBUF | B1 | 1 |
| | ENOUT | ADLIB:INBUF | J16 | 1 |
| | LED | ADLIB:OUTBUF | M3 | 0 |
| | MONITOR[0] | ADLIB:OUTBUF | B5 | 0 |
| | MONITOR[1] | ADLIB:OUTBUF | C7 | Z |
| | MONITOR[2] | ADLIB:OUTBUF | D9 | Z |
| | MONITOR[3] | ADLIB:OUTBUF | D7 | Z |
| | MONITOR[4] | ADLIB:OUTBUF | A11 | Z |
| | OEa | ADLIB:INBUF | E4 | Z |
| | OEb | ADLIB:INBUF | F1 | Z |
| | OSC_EN | ADLIB:INBUF | K3 | Z |
| | PAD[10] | ADLIB:BIBUF_LVCMOS33U | M8 | Z |
| | PAD[11] | ADLIB:BIBUF_LVCMOS33D | R7 | Z |
| | PAD[12] | ADLIB:BIBUF_LVCMOS33U | D11 | Z |
| | PAD[13] | ADLIB:BIBUF_LVCMOS33D | C12 | Z |
| | PAD[14] | ADLIB:BIBUF_LVCMOS33U | R6 | Z |

***Figure 1-4 •*** **I/O States During Programming Window**

6. Click OK to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

## Overview of I/O Performance

### Summary of I/O DC Input and Output Levels – Default I/O Software Settings

**Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions**

| I/O Standard | Drive Strength | Equivalent Software Default Drive Strength[2] | Slew Rate | VIL Min. V | VIL Max. V | VIH Min. V | VIH Max. V | VOL Max. V | VOH Min. V | IOL[1] mA | IOH[1] mA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 12 mA | 12 mA | High | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 |
| 3.3 V LVCMOS Wide Range[3] | 100 µA | 12 mA | High | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VCCI – 0.2 | 0.1 | 0.1 |
| 2.5 V LVCMOS | 12 mA | 12 mA | High | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 12 | 12 |
| 1.8 V LVCMOS | 12 mA | 12 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI – 0.45 | 12 | 12 |
| 1.5 V LVCMOS | 12 mA | 12 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 |
| 1.2 V LVCMOS | 2 mA | 2 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 |
| 1.2 V LVCMOS Wide Range[4] | 100 µA | 2 mA | High | –0.3 | 0.3 * VCCI | 0.7 * VCCI | 3.6 | 0.1 | VCCI – 0.1 | 0.1 | 0.1 |
| 3.3 V PCI | Per PCI Specification | | | | | | | | | | |
| 3.3 V PCI-X | Per PCI-X Specification | | | | | | | | | | |
| 3.3 V GTL | 20 mA[5] | 20 mA[5] | High | –0.3 | VREF – 0.05 | VREF + 0.05 | 3.6 | 0.4 | – | 20 | 20 |
| 2.5 V GTL | 20 mA[5] | 20 mA[5] | High | –0.3 | VREF – 0.05 | VREF + 0.05 | 3.6 | 0.4 | – | 20 | 20 |
| 3.3 V GTL+ | 35 mA | 35 mA | High | –0.3 | VREF – 0.1 | VREF + 0.1 | 3.6 | 0.6 | – | 35 | 35 |
| 2.5 V GTL+ | 33 mA | 33 mA | High | –0.3 | VREF – 0.1 | VREF + 0.1 | 3.6 | 0.6 | – | 33 | 33 |
| HSTL (I) | 8 mA | 8 mA | High | –0.3 | VREF – 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI – 0.4 | 8 | 8 |

*Notes:*

1. *Currents are measured at 85°C junction temperature.*
2. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-12 specification.*
4. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*
5. *Output drive strength is below JEDEC specification.*
6. *Output Slew Rates can be extracted from IBIS Models, http://www.microsemi.com/soc/download/ibis/default.aspx.*

### Summary of I/O Timing Characteristics – Default I/O Software Settings

**Table 2-23 • Summary of AC Measuring Points**

| Standard | Input Reference Voltage (VREF_TYP) | Board Termination Voltage (VTT_REF) | Measuring Trip Point (Vtrip) |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | – | – | 1.4 V |
| 3.3 V LVCMOS Wide Range | – | – | 1.4 V |
| 2.5 V LVCMOS | – | – | 1.2 V |
| 1.8 V LVCMOS | – | – | 0.90 V |
| 1.5 V LVCMOS | – | – | 0.75 V |
| 1.2 V LVCMOS* | – | – | 0.6 V |
| 1.2 V LVCMOS – Wide Range* | – | – | 0.6 V |
| 3.3 V PCI | – | – | 0.285 * VCCI (RR) |
| | – | – | 0.615 * VCCI (FF)) |
| 3.3 V PCI-X | – | – | 0.285 * VCCI (RR) |
| | – | – | 0.615 * VCCI (FF) |
| 3.3 V GTL | 0.8 V | 1.2 V | VREF |
| 2.5 V GTL | 0.8 V | 1.2 V | VREF |
| 3.3 V GTL+ | 1.0 V | 1.5 V | VREF |
| 2.5 V GTL+ | 1.0 V | 1.5 V | VREF |
| HSTL (I) | 0.75 V | 0.75 V | VREF |
| HSTL (II) | 0.75 V | 0.75 V | VREF |
| SSTL2 (I) | 1.25 V | 1.25 V | VREF |
| SSTL2 (II) | 1.25 V | 1.25 V | VREF |
| SSTL3 (I) | 1.5 V | 1.485 V | VREF |
| SSTL3 (II) | 1.5 V | 1.485 V | VREF |
| LVDS | – | – | Cross point |
| LVPECL | – | – | Cross point |

*Note: *Applicable to V2 devices ONLY operating in the 1.2 V core range.*

**Table 2-24 • I/O AC Parameter Definitions**

| Parameter | Definition |
|---|---|
| $t_{DP}$ | Data to Pad delay through the Output Buffer |
| $t_{PY}$ | Pad to Data delay through the Input Buffer with Schmitt trigger disabled |
| $t_{DOUT}$ | Data to Output Buffer delay through the I/O interface |
| $t_{EOUT}$ | Enable to Output Buffer Tristate Control delay through the I/O interface |
| $t_{DIN}$ | Input Buffer to Data delay through the I/O interface |
| $t_{PYS}$ | Pad to Data delay through the Input Buffer with Schmitt trigger enabled |
| $t_{HZ}$ | Enable to Pad delay through the Output Buffer—HIGH to Z |
| $t_{ZH}$ | Enable to Pad delay through the Output Buffer—Z to HIGH |
| $t_{LZ}$ | Enable to Pad delay through the Output Buffer—LOW to Z |
| $t_{ZL}$ | Enable to Pad delay through the Output Buffer—Z to LOW |
| $t_{ZHS}$ | Enable to Pad delay through the Output Buffer with delayed enable—Z to HIGH |
| $t_{ZLS}$ | Enable to Pad delay through the Output Buffer with delayed enable—Z to LOW |

**Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings**
**Std. Speed Grade, Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI (per standard)**

| I/O Standard | Drive Strength (mA) | Equivalent Software Default Drive Strength Option[1] (mA) | Slew Rate | Capacitive Load (pF) | External Resistor (Ω) | $t_{DOUT}$ (ns) | $t_{DP}$ (ns) | $t_{DIN}$ (ns) | $t_{PY}$ (ns) | $t_{PYS}$ (ns) | $t_{EOUT}$ (ns) | $t_{ZL}$ (ns) | $t_{ZH}$ (ns) | $t_{LZ}$ (ns) | $t_{HZ}$ (ns) | $t_{ZLS}$ (ns) | $t_{ZHS}$ (ns) | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 12 | 12 | High | 5 | – | 1.55 | 2.47 | 0.26 | 1.31 | 1.58 | 1.10 | 2.51 | 2.04 | 3.28 | 3.97 | 8.29 | 7.82 | ns |
| 3.3 V LVCMOS Wide Range[1,2] | 100 µA | 12 | High | 35 | – | 1.55 | 3.40 | 0.26 | 1.66 | 2.14 | 1.10 | 3.40 | 2.68 | 4.55 | 5.49 | 9.19 | 8.46 | ns |
| 2.5 V LVCMOS | 12 | 12 | High | 5 | – | 1.55 | 2.51 | 0.26 | 1.55 | 1.77 | 1.10 | 2.54 | 2.22 | 3.36 | 3.85 | 8.33 | 8.00 | ns |
| 1.8 V LVCMOS | 12 | 12 | High | 5 | – | 1.55 | 2.75 | 0.26 | 1.53 | 1.96 | 1.10 | 2.78 | 2.40 | 3.68 | 4.56 | 8.57 | 8.19 | ns |
| 1.5 V LVCMOS | 12 | 12 | High | 5 | – | 1.55 | 3.10 | 0.26 | 1.72 | 2.16 | 1.10 | 3.15 | 2.70 | 3.86 | 4.68 | 8.93 | 8.49 | ns |
| 1.2 V LVCMOS | 2 | 2 | High | 5 | – | 1.55 | 4.06 | 0.26 | 2.09 | 2.95 | 1.10 | 3.92 | 3.46 | 4.01 | 3.79 | 9.71 | 9.24 | ns |
| 1.2 V LVCMOS Wide Range[1,3] | 100 µA | 2 | High | 5 | – | 1.55 | 4.06 | 0.26 | 2.09 | 2.95 | 1.10 | 3.92 | 3.46 | 4.01 | 3.79 | 9.71 | 9.24 | ns |
| 3.3 V PCI | Per PCI spec | – | High | 10 | 25[4] | 1.55 | 2.76 | 0.26 | 1.19 | 1.63 | 1.10 | 2.79 | 2.16 | 3.29 | 3.97 | 8.58 | 7.94 | ns |
| 3.3 V PCI-X | Per PCI-X spec | – | High | 10 | 25[4] | 1.55 | 2.76 | 0.25 | 1.22 | 1.58 | 1.10 | 2.79 | 2.16 | 3.29 | 3.97 | 8.58 | 7.94 | ns |
| 3.3 V GTL | 20[5] | – | High | 10 | 25 | 1.55 | 2.08 | 0.25 | 2.76 | – | 1.10 | 2.09 | 2.08 | – | – | 7.88 | 7.87 | ns |
| 2.5 V GTL | 20[5] | – | High | 10 | 25 | 1.55 | 2.17 | 0.25 | 2.35 | – | 1.10 | 2.20 | 2.13 | – | – | 7.99 | 7.91 | ns |
| 3.3 V GTL+ | 35 | – | High | 10 | 25 | 1.55 | 2.12 | 0.25 | 1.62 | – | 1.10 | 2.14 | 2.07 | – | – | 7.93 | 7.85 | ns |
| 2.5 V GTL+ | 33 | – | High | 10 | 25 | 1.55 | 2.25 | 0.25 | 1.55 | – | 1.10 | 2.27 | 2.10 | – | – | 8.06 | 7.89 | ns |
| HSTL (I) | 8 | – | High | 20 | 50 | 1.55 | 3.09 | 0.25 | 1.95 | – | 1.10 | 3.11 | 3.09 | – | – | 8.90 | 8.88 | ns |
| HSTL (II) | 15 | – | High | 20 | 25 | 1.55 | 2.94 | 0.25 | 1.95 | – | 1.10 | 2.98 | 2.74 | – | – | 8.77 | 8.53 | ns |
| SSTL2 (I) | 15 | – | High | 30 | 50 | 1.55 | 2.18 | 0.25 | 1.40 | – | 1.10 | 2.21 | 2.03 | – | – | 7.99 | 7.82 | ns |
| SSTL2 (II) | 18 | – | High | 30 | 25 | 1.55 | 2.21 | 0.25 | 1.40 | – | 1.10 | 2.24 | 1.97 | – | – | 8.03 | 7.76 | ns |
| SSTL3 (I) | 14 | – | High | 30 | 50 | 1.55 | 2.33 | 0.25 | 1.33 | – | 1.10 | 2.36 | 2.02 | – | – | 8.15 | 7.81 | ns |
| SSTL3 (II) | 21 | – | High | 30 | 25 | 1.55 | 2.13 | 0.25 | 1.33 | – | 1.10 | 2.16 | 1.89 | – | – | 7.94 | 7.67 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
3. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*
4. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-49 for connectivity. This resistor is not required during normal operation.*
5. *Output drive strength is below JEDEC specification.*
6. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

***Table 2-31 •*** **Duration of Short Circuit Event before Failure**

| Temperature | Time before Failure |
|---|---|
| –40°C | > 20 years |
| 0°C | > 20 years |
| 25°C | > 20 years |
| 70°C | 5 years |
| 85°C | 2 years |
| 100°C | 6 months |

***Table 2-32 •*** **Schmitt Trigger Input Hysteresis**
**Hysteresis Voltage Value (Typ.) for Schmitt Mode Input Buffers**

| Input Buffer Configuration | Hysteresis Value (typ.) |
|---|---|
| 3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode) | 240 mV |
| 2.5 V LVCMOS (Schmitt trigger mode) | 140 mV |
| 1.8 V LVCMOS (Schmitt trigger mode) | 80 mV |
| 1.5 V LVCMOS (Schmitt trigger mode) | 60 mV |
| 1.2 V LVCMOS (Schmitt trigger mode) | 40 mV |

***Table 2-33 •*** **I/O Input Rise Time, Fall Time, and Related I/O Reliability***

| Input Buffer | Input Rise/Fall Time (min.) | Input Rise/Fall Time (max.) | Reliability |
|---|---|---|---|
| LVTTL/LVCMOS (Schmitt trigger disabled) | No requirement | 10 ns* | 20 years (100°C) |
| LVTTL/LVCMOS (Schmitt trigger enabled) | No requirement | No requirement, but input noise voltage cannot exceed Schmitt hysteresis. | 20 years (100°C) |
| HSTL/SSTL/GTL | No requirement | 10 ns* | 10 years (100°C) |
| LVDS/B-LVDS/M-LVDS/LVPECL | No requirement | 10 ns* | 10 years (100°C) |

Note: **The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

## Timing Characteristics

### 1.5 V DC Core Voltage

**Table 2-36 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 0.97 | 4.90 | 0.18 | 1.08 | 1.34 | 0.66 | 5.00 | 3.99 | 2.27 | 2.16 | 8.60 | 7.59 | ns |
| 8 mA | Std. | 0.97 | 4.05 | 0.18 | 1.08 | 1.34 | 0.66 | 4.13 | 3.45 | 2.53 | 2.65 | 7.73 | 7.05 | ns |
| 12 mA | Std. | 0.97 | 3.44 | 0.18 | 1.08 | 1.34 | 0.66 | 3.51 | 3.05 | 2.71 | 2.95 | 7.11 | 6.64 | ns |
| 16 mA | Std. | 0.97 | 3.27 | 0.18 | 1.08 | 1.34 | 0.66 | 3.34 | 2.96 | 2.74 | 3.04 | 6.93 | 6.55 | ns |
| 24 mA | Std. | 0.97 | 3.18 | 0.18 | 1.08 | 1.34 | 0.66 | 3.24 | 2.97 | 2.79 | 3.36 | 6.84 | 6.56 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

**Table 2-37 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 0.97 | 2.85 | 0.18 | 1.08 | 1.34 | 0.66 | 2.92 | 2.27 | 2.27 | 2.27 | 6.51 | 5.87 | ns |
| 8 mA | Std. | 0.97 | 2.39 | 0.18 | 1.08 | 1.34 | 0.66 | 2.44 | 1.88 | 2.53 | 2.76 | 6.03 | 5.47 | ns |
| 12 mA | Std. | 0.97 | 2.12 | 0.18 | 1.08 | 1.34 | 0.66 | 2.17 | 1.69 | 2.71 | 3.08 | 5.76 | 5.28 | ns |
| 16 mA | Std. | 0.97 | 2.08 | 0.18 | 1.08 | 1.34 | 0.66 | 2.12 | 1.65 | 2.75 | 3.17 | 5.72 | 5.25 | ns |
| 24 mA | Std. | 0.97 | 2.10 | 0.18 | 1.08 | 1.34 | 0.66 | 2.14 | 1.60 | 2.80 | 3.49 | 5.74 | 5.20 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*1.2 V DC Core Voltage*

***Table 2-44 •*** **3.3 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7 V**

| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 4 mA | Std. | 1.55 | 8.14 | 0.26 | 1.66 | 2.14 | 1.10 | 8.14 | 6.46 | 3.80 | 3.79 | 13.93 | 12.25 | ns |
| 100 µA | 8 mA | Std. | 1.55 | 6.68 | 0.26 | 1.66 | 2.14 | 1.10 | 6.68 | 5.57 | 4.25 | 4.69 | 12.47 | 11.36 | ns |
| 100 µA | 12 mA | Std. | 1.55 | 5.65 | 0.26 | 1.66 | 2.14 | 1.10 | 5.65 | 4.91 | 4.55 | 5.25 | 11.44 | 10.69 | ns |
| 100 µA | 16 mA | Std. | 1.55 | 5.36 | 0.26 | 1.66 | 2.14 | 1.10 | 5.36 | 4.76 | 4.61 | 5.41 | 11.14 | 10.55 | ns |
| 100 µA | 24 mA | Std. | 1.55 | 5.20 | 0.26 | 1.66 | 2.14 | 1.10 | 5.20 | 4.78 | 4.69 | 6.00 | 10.99 | 10.56 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

***Table 2-45 •*** **3.3 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7 V**

| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 4 mA | Std. | 1.55 | 4.65 | 0.26 | 1.66 | 2.14 | 110 | 4.65 | 3.64 | 3.80 | 4.00 | 10.44 | 9.43 | ns |
| 100 µA | 8 mA | Std. | 1.55 | 3.85 | 0.26 | 1.66 | 2.14 | 1.10 | 3.85 | 2.99 | 4.25 | 4.91 | 9.64 | 8.77 | ns |
| 100 µA | 12 mA | Std. | 1.55 | 3.40 | 0.26 | 1.66 | 2.14 | 1.10 | 3.40 | 2.68 | 4.55 | 5.49 | 9.19 | 8.46 | ns |
| 100 µA | 16 mA | Std. | 1.55 | 3.33 | 0.26 | 1.66 | 2.14 | 1.10 | 3.33 | 2.62 | 4.62 | 5.65 | 9.11 | 8.41 | ns |
| 100 µA | 24 mA | Std. | 1.55 | 3.36 | 0.26 | 1.66 | 2.14 | 1.10 | 3.36 | 2.54 | 4.71 | 6.24 | 9.15 | 8.32 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*
3. *Software default selection highlighted in gray.*

### 3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

**Table 2-69 • Minimum and Maximum DC Input and Output Levels**

| 3.3 V PCI/PCI-X | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min., V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | μA[4] | μA[4] |
| Per PCI specification | Per PCI curves | | | | | | | | | | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.
2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microsemi loadings for enable path characterization are described in Figure 2-12.

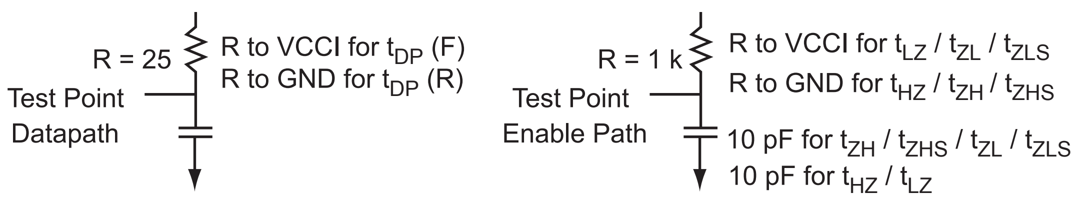



**Figure 2-12 • AC Loading**

AC loadings are defined per PCI/PCI-X specifications for the datapath; Microsemi loading for tristate is described in Table 2-70.

**Table 2-70 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|
| 0 | 3.3 | 0.285 * VCCI for $t_{DP(R)}$<br>0.615 * VCCI for $t_{DP(F)}$ | – | 10 |

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.

### SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). IGLOOe devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

**Table 2-97 • Minimum and Maximum DC Input and Output Levels**

| SSTL2 Class I | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 15 mA | –0.3 | VREF – 0.2 | VREF + 0.2 | 3.6 | 0.54 | VCCI – 0.62 | 15 | 15 | 83 | 87 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

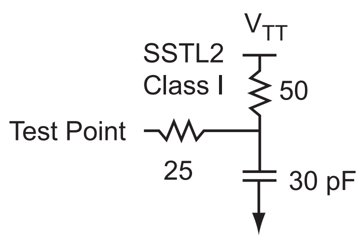



**Figure 2-19 • AC Loading**

**Table 2-98 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|---|
| VREF – 0.2 | VREF + 0.2 | 1.25 | 1.25 | 1.25 | 30 |

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

### Timing Characteristics

#### 1.5 V DC Core Voltage

**Table 2-99 • SSTL 2 Class I – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V,**
**Worst-Case VCCI = 2.3 V VREF = 1.25 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.98 | 1.91 | 0.19 | 1.15 | 0.67 | 1.94 | 1.72 | | | 5.57 | 5.35 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

#### 1.2 V DC Core Voltage

**Table 2-100 • SSTL 2 Class I – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V,**
**Worst-Case VCCI = 2.3 V VREF = 1.25 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 1.55 | 2.17 | 0.26 | 1.39 | 1.10 | 2.21 | 2.04 | | | 8.02 | 7.84 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

## SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). IGLOOe devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

***Table 2-105* • Minimum and Maximum DC Input and Output Levels**

| SSTL3 Class I | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 14 mA | –0.3 | VREF – 0.2 | VREF + 0.2 | 3.6 | 0.7 | VCCI – 1.1 | 14 | 14 | 51 | 54 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

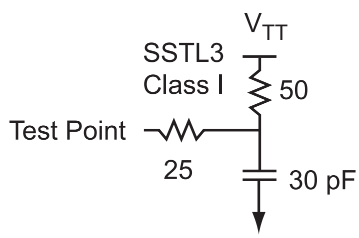



***Figure 2-21* • AC Loading**

***Table 2-106* • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|---|
| VREF – 0.2 | VREF + 0.2 | 1.5 | 1.5 | 1.485 | 30 |

*Note:* **Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

### Timing Characteristics

#### 1.5 V DC Core Voltage

***Table 2-107* • SSTL 3 Class I – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V,**
**Worst-Case VCCI = 3.0 V VREF = 1.5 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.98 | 2.05 | 0.19 | 1.09 | 0.67 | 2.09 | 1.71 | | | 5.72 | 5.34 | ns |

*Note:* *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

#### 1.2 V DC Core Voltage

***Table 2-108* • SSTL 3 Class I – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V,**
**Worst-Case VCCI = 3.0 V VREF = 1.5 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 1.55 | 2.32 | 0.26 | 1.32 | 1.10 | 2.37 | 2.02 | | | 8.17 | 7.83 | ns |

*Note:* *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

### 1.2 V DC Core Voltage

**Table 2-124 • Input Data Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | 0.68 | ns |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | 0.97 | ns |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | 0.00 | ns |
| $t_{ISUE}$ | Enable Setup Time for the Input Data Register | 1.02 | ns |
| $t_{IHE}$ | Enable Hold Time for the Input Data Register | 0.00 | ns |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | 1.19 | ns |
| $t_{IPRE2Q}$ | Asynchronous Preset-to-Q of the Input Data Register | 1.19 | ns |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{IWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{ICKMPWH}$ | Clock Minimum Pulse Width HIGH for the Input Data Register | 0.31 | ns |
| $t_{ICKMPWL}$ | Clock Minimum Pulse Width LOW for the Input Data Register | 0.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

## Output Register

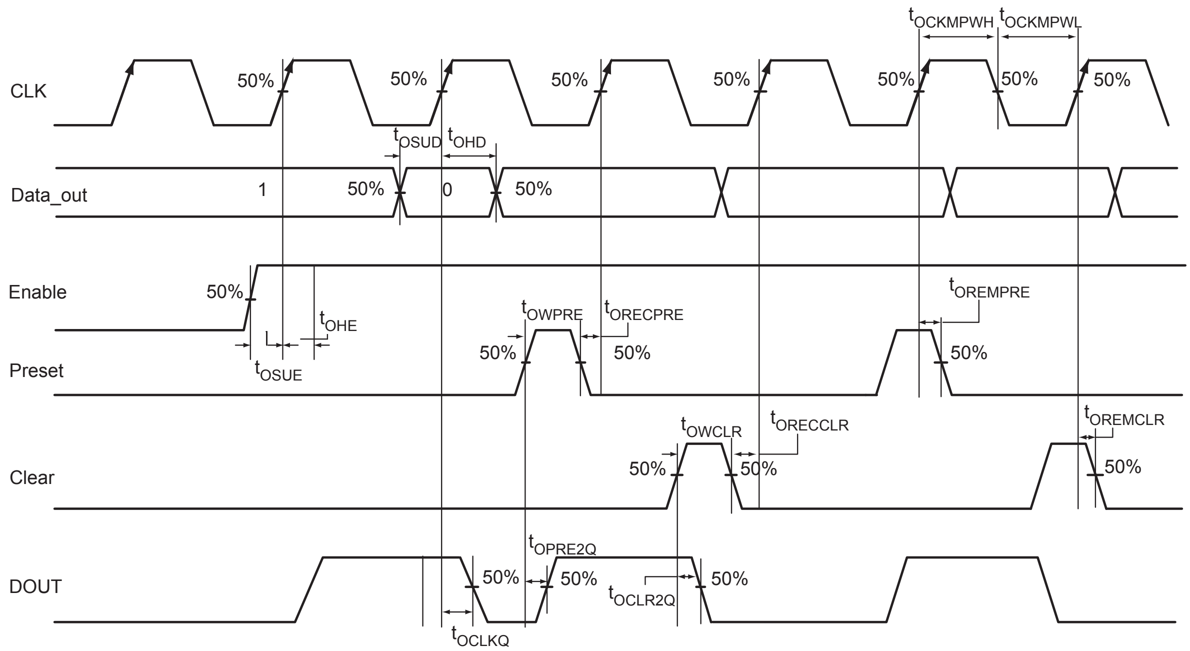



**Figure 2-29 • Output Register Timing Diagram**

### Timing Characteristics

#### 1.5 V DC Core Voltage

**Table 2-125 • Output Data Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | 1.00 | ns |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | 0.51 | ns |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | 0.00 | ns |
| $t_{OSUE}$ | Enable Setup Time for the Output Data Register | 0.70 | ns |
| $t_{OHE}$ | Enable Hold Time for the Output Data Register | 0.00 | ns |
| $t_{OCLR2Q}$ | Asynchronous Clear-to-Q of the Output Data Register | 1.34 | ns |
| $t_{OPRE2Q}$ | Asynchronous Preset-to-Q of the Output Data Register | 1.34 | ns |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | 0.24 | ns |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | 0.24 | ns |
| $t_{OWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Data Register | 0.19 | ns |
| $t_{OWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Data Register | 0.19 | ns |
| $t_{OCKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output Data Register | 0.31 | ns |
| $t_{OCKMPWL}$ | Clock Minimum Pulse Width LOW for the Output Data Register | 0.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

# VersaTile Characteristics

## VersaTile Specifications as a Combinatorial Module

The IGLOOe library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

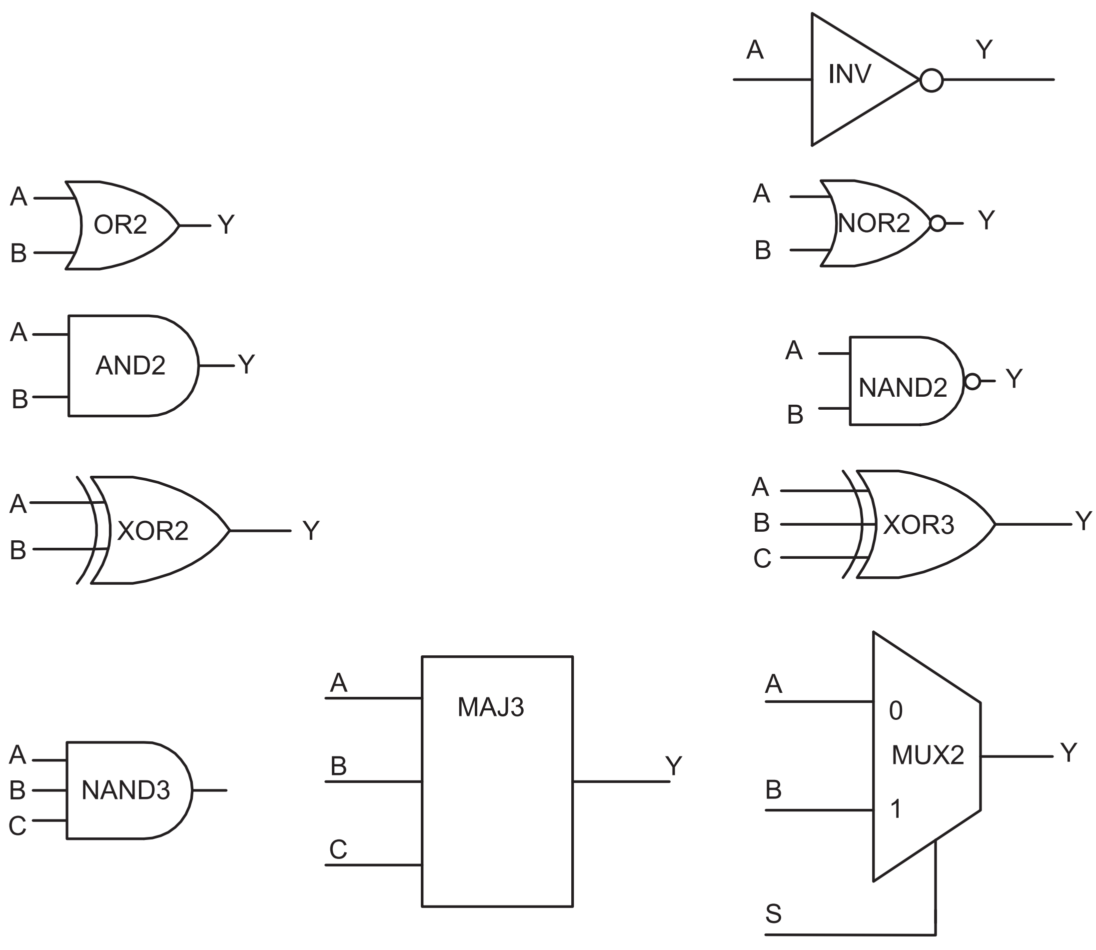



***Figure 2-35 •*** **Sample of Combinatorial Cells**

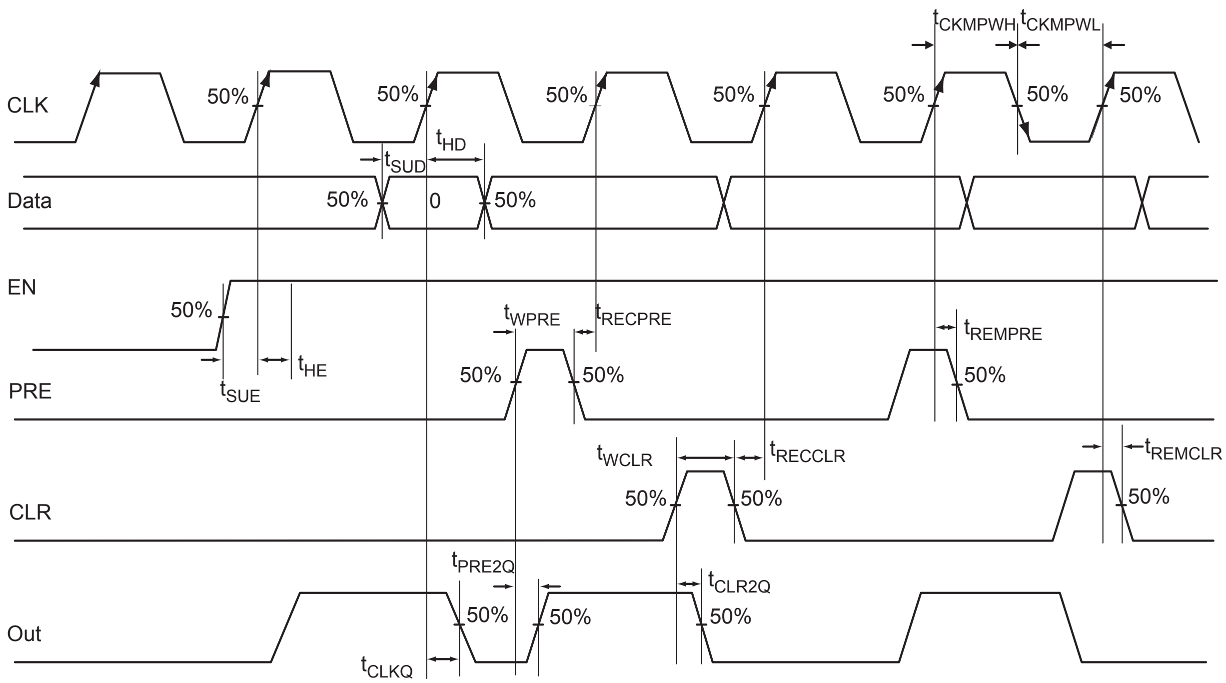



*Figure 2-38* • **Timing Model and Waveforms**

## *Timing Characteristics*

### *1.5 V DC Core Voltage*

***Table 2-137*** **• Register Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{CLKQ}$ | Clock-to-Q of the Core Register | 0.89 | ns |
| $t_{SUD}$ | Data Setup Time for the Core Register | 0.81 | ns |
| $t_{HD}$ | Data Hold Time for the Core Register | 0.00 | ns |
| $t_{SUE}$ | Enable Setup Time for the Core Register | 0.73 | ns |
| $t_{HE}$ | Enable Hold Time for the Core Register | 0.00 | ns |
| $t_{CLR2Q}$ | Asynchronous Clear-to-Q of the Core Register | 0.60 | ns |
| $t_{PRE2Q}$ | Asynchronous Preset-to-Q of the Core Register | 0.62 | ns |
| $t_{REMCLR}$ | Asynchronous Clear Removal Time for the Core Register | 0.00 | ns |
| $t_{RECCLR}$ | Asynchronous Clear Recovery Time for the Core Register | 0.24 | ns |
| $t_{REMPRE}$ | Asynchronous Preset Removal Time for the Core Register | 0.00 | ns |
| $t_{RECPRE}$ | Asynchronous Preset Recovery Time for the Core Register | 0.23 | ns |
| $t_{WCLR}$ | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.30 | ns |
| $t_{WPRE}$ | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.30 | ns |
| $t_{CKMPWH}$ | Clock Minimum Pulse Width HIGH for the Core Register | 0.56 | ns |
| $t_{CKMPWL}$ | Clock Minimum Pulse Width LOW for the Core Register | 0.56 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

| FG896 | |
|---|---|
| Pin Number | AGLE3000 Function |
| D30 | GBA2/IO82PPB2V0 |
| E1 | GND |
| E2 | IO303NPB7V3 |
| E3 | VCCIB7 |
| E4 | IO305PPB7V3 |
| E5 | VCC |
| E6 | GAC0/IO02NDB0V0 |
| E7 | VCCIB0 |
| E8 | IO06PPB0V0 |
| E9 | IO24NDB0V2 |
| E10 | IO24PDB0V2 |
| E11 | IO13NDB0V1 |
| E12 | IO13PDB0V1 |
| E13 | IO34NDB0V4 |
| E14 | IO34PDB0V4 |
| E15 | IO40NDB0V4 |
| E16 | IO49NDB1V1 |
| E17 | IO49PDB1V1 |
| E18 | IO50PDB1V1 |
| E19 | IO58PDB1V2 |
| E20 | IO60NDB1V2 |
| E21 | IO77PDB1V4 |
| E22 | IO68NDB1V3 |
| E23 | IO68PDB1V3 |
| E24 | VCCIB1 |
| E25 | IO74PDB1V4 |
| E26 | VCC |
| E27 | GBB1/IO80PPB1V4 |
| E28 | VCCIB2 |
| E29 | IO82NPB2V0 |
| E30 | GND |
| F1 | IO296PPB7V2 |
| F2 | VCC |
| F3 | IO306PDB7V4 |
| F4 | IO297PDB7V2 |

| FG896 | |
|---|---|
| Pin Number | AGLE3000 Function |
| F5 | VMV7 |
| F5 | VMV7 |
| F6 | GND |
| F7 | GNDQ |
| F8 | IO12NDB0V1 |
| F9 | IO12PDB0V1 |
| F10 | IO10PDB0V1 |
| F11 | IO16PDB0V1 |
| F12 | IO22NDB0V2 |
| F13 | IO30NDB0V3 |
| F14 | IO30PDB0V3 |
| F15 | IO36PDB0V4 |
| F16 | IO48NDB1V0 |
| F17 | IO48PDB1V0 |
| F18 | IO50NDB1V1 |
| F19 | IO58NDB1V2 |
| F20 | IO60PDB1V2 |
| F21 | IO77NDB1V4 |
| F22 | IO72NDB1V3 |
| F23 | IO72PDB1V3 |
| F24 | GNDQ |
| F25 | GND |
| F26 | VMV2 |
| F26 | VMV2 |
| F27 | IO86PDB2V0 |
| F28 | IO92PDB2V1 |
| F29 | VCC |
| F30 | IO100NPB2V2 |
| G1 | GND |
| G2 | IO296NPB7V2 |
| G3 | IO306NDB7V4 |
| G4 | IO297NDB7V2 |
| G5 | VCCIB7 |
| G6 | GNDQ |
| G6 | GNDQ |

| FG896 | |
|---|---|
| Pin Number | AGLE3000 Function |
| G7 | VCC |
| G8 | VMV0 |
| G9 | VCCIB0 |
| G10 | IO10NDB0V1 |
| G11 | IO16NDB0V1 |
| G12 | IO22PDB0V2 |
| G13 | IO26PPB0V3 |
| G14 | IO38NPB0V4 |
| G15 | IO36NDB0V4 |
| G16 | IO46NDB1V0 |
| G17 | IO46PDB1V0 |
| G18 | IO56NDB1V1 |
| G19 | IO56PDB1V1 |
| G20 | IO66NDB1V3 |
| G21 | IO66PDB1V3 |
| G22 | VCCIB1 |
| G23 | VMV1 |
| G24 | VCC |
| G25 | GNDQ |
| G25 | GNDQ |
| G26 | VCCIB2 |
| G27 | IO86NDB2V0 |
| G28 | IO92NDB2V1 |
| G29 | IO100PPB2V2 |
| G30 | GND |
| H1 | IO294PDB7V2 |
| H2 | IO294NDB7V2 |
| H3 | IO300NDB7V3 |
| H4 | IO300PDB7V3 |
| H5 | IO295PDB7V2 |
| H6 | IO299PDB7V3 |
| H7 | VCOMPLA |
| H8 | GND |
| H9 | IO08NDB0V0 |
| H10 | IO08PDB0V0 |

| FG896 | |
|---|---|
| Pin Number | AGLE3000 Function |
| L26 | IO87NDB2V0 |
| L27 | IO97PDB2V1 |
| L28 | IO101PDB2V2 |
| L29 | IO103PDB2V2 |
| L30 | IO119NDB3V0 |
| M1 | IO282NDB7V1 |
| M2 | IO282PDB7V1 |
| M3 | IO292NDB7V2 |
| M4 | IO292PDB7V2 |
| M5 | IO283NDB7V1 |
| M6 | IO285PDB7V1 |
| M7 | IO287PDB7V1 |
| M8 | IO289PDB7V1 |
| M9 | IO289NDB7V1 |
| M10 | VCCIB7 |
| M11 | VCC |
| M12 | GND |
| M13 | GND |
| M14 | GND |
| M15 | GND |
| M16 | GND |
| M17 | GND |
| M18 | GND |
| M19 | GND |
| M20 | VCC |
| M21 | VCCIB2 |
| M22 | NC |
| M23 | IO104PPB2V2 |
| M24 | IO102PDB2V2 |
| M25 | IO102NDB2V2 |
| M26 | IO95PDB2V1 |
| M27 | IO97NDB2V1 |
| M28 | IO101NDB2V2 |
| M29 | IO103NDB2V2 |
| M30 | IO119PDB3V0 |

| FG896 | |
|---|---|
| Pin Number | AGLE3000 Function |
| N1 | IO276PDB7V0 |
| N2 | IO278PDB7V0 |
| N3 | IO280PDB7V0 |
| N4 | IO284PDB7V1 |
| N5 | IO279PDB7V0 |
| N6 | IO285NDB7V1 |
| N7 | IO287NDB7V1 |
| N8 | IO281NDB7V0 |
| N9 | IO281PDB7V0 |
| N10 | VCCIB7 |
| N11 | VCC |
| N12 | GND |
| N13 | GND |
| N14 | GND |
| N15 | GND |
| N16 | GND |
| N17 | GND |
| N18 | GND |
| N19 | GND |
| N20 | VCC |
| N21 | VCCIB2 |
| N22 | IO106NDB2V3 |
| N23 | IO106PDB2V3 |
| N24 | IO108PDB2V3 |
| N25 | IO108NDB2V3 |
| N26 | IO95NDB2V1 |
| N27 | IO99NDB2V2 |
| N28 | IO99PDB2V2 |
| N29 | IO107PDB2V3 |
| N30 | IO107NDB2V3 |
| P1 | IO276NDB7V0 |
| P2 | IO278NDB7V0 |
| P3 | IO280NDB7V0 |
| P4 | IO284NDB7V1 |
| P5 | IO279NDB7V0 |

| FG896 | |
|---|---|
| Pin Number | AGLE3000 Function |
| P6 | GFC1/IO275PDB7V0 |
| P7 | GFC0/IO275NDB7V0 |
| P8 | IO277PDB7V0 |
| P9 | IO277NDB7V0 |
| P10 | VCCIB7 |
| P11 | VCC |
| P12 | GND |
| P13 | GND |
| P14 | GND |
| P15 | GND |
| P16 | GND |
| P17 | GND |
| P18 | GND |
| P19 | GND |
| P20 | VCC |
| P21 | VCCIB2 |
| P22 | GCC1/IO112PDB2V3 |
| P23 | IO110PDB2V3 |
| P24 | IO110NDB2V3 |
| P25 | IO109PPB2V3 |
| P26 | IO111NPB2V3 |
| P27 | IO105PDB2V2 |
| P28 | IO105NDB2V2 |
| P29 | GCC2/IO117PDB3V0 |
| P30 | IO117NDB3V0 |
| R1 | GFC2/IO270PDB6V4 |
| R2 | GFB1/IO274PPB7V0 |
| R3 | VCOMPLF |
| R4 | GFA0/IO273NDB6V4 |
| R5 | GFB0/IO274NPB7V0 |
| R6 | IO271NDB6V4 |
| R7 | GFB2/IO271PDB6V4 |
| R8 | IO269PDB6V4 |
| R9 | IO269NDB6V4 |
| R10 | VCCIB7 |

| Revision | Changes | Page |
|---|---|---|
| Revision 9 (continued) | The example in the paragraph above Table 2-31 • Duration of Short Circuit Event before Failure was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 32287). | 2-31 |
| | The notes regarding drive strength in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section, "3.3 V LVCMOS Wide Range" section and "1.2 V LVCMOS Wide Range" section tables were revised for clarification. They now state that the minimum drive strength for the default software configuration when run in wide range is ±100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 34766). | 2-23, 2-35, 2-48 |
| | The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34886). | 2-32 |
| | The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 34793): "It uses a 5 V–tolerant input buffer and push-pull output buffer." | 2-38 |
| | Table 2-143 • IGLOOe CCC/PLL Specification and Table 2-144 • IGLOOe CCC/PLL Specification were updated. A note was added to both tables indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34818). | 2-91, 2-92 |
| | The following figures were deleted. Reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in detail (SAR 34869).<br>Figure 2-46 • Write Access after Write onto Same Address<br>Figure 2-47 • Read Access after Write onto Same Address<br>Figure 2-48 • Write Access after Read onto Same Address<br>The port names in the SRAM "Timing Waveforms", SRAM "Timing Characteristics" tables, Figure 2-50 • FIFO Reset, and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 35749). | 2-95, 2-98, 2-104, 2-106 |
| | The "Pin Descriptions and Packaging" chapter is new (SAR 34768). | 3-1 |
| | Package names used in the "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 34768) | 4-1 |
| July 2010 | The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "IGLOOe Device Status" table on page II indicates the status for each device in the device family. | N/A |