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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	13824
Total RAM Bits	110592
Number of I/O	165
Number of Gates	600000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agle600v2-fgg256

Temperature Grade Offerings

Package	AGLE600	AGLE3000
		M1AGLPE3000
FG256	C, I	–
FG484	C, I	C, I
FG896	–	C, I

Note: C = Commercial temperature range: 0°C to 70°C ambient temperature.
I = Industrial temperature range: –40°C to 85°C ambient temperature.

References made to IGLOOe devices also apply to ARM-enabled IGLOOe devices. The ARM-enabled part numbers start with M1 (Cortex-M1).

Contact your local Microsemi SoC Products Group representative for device availability:

http://www.microsemi.com/soc/contact/default.aspx.

SRAM and FIFO

IGLOOe devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

IGLOOe devices provide designers with very flexible clock conditioning capabilities. Each member of the IGLOOe family contains six CCCs, each with an integrated PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz up to 250 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration.
- Output duty cycle = 50% ± 1.5% or better
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used
- Maximum acquisition time is 300 µs
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 250 MHz / f_{OUT_CCC}

Global Clocking

IGLOOe devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

2 – IGLOOe DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI and VMV[3]	DC I/O buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T_{STG} [2]	Storage temperature	–65 to +150	°C
T_J [2]	Junction temperature	+125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.*
2. *For flash programming and retention maximum limits, refer to Table 2-3 on page 2-3, and for recommended operating limits, refer to Table 2-2 on page 2-2.*
3. *VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information.*

Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature[1]

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

Table 2-4 • Overshoot and Undershoot Limits [1, 3]

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at junction temperature at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
3. *This table does not provide PCI overshoot/undershoot limits.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOOe device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5.

There are five regions to consider during power-up.

IGLOOe I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.

User I/O Characteristics

Timing Model

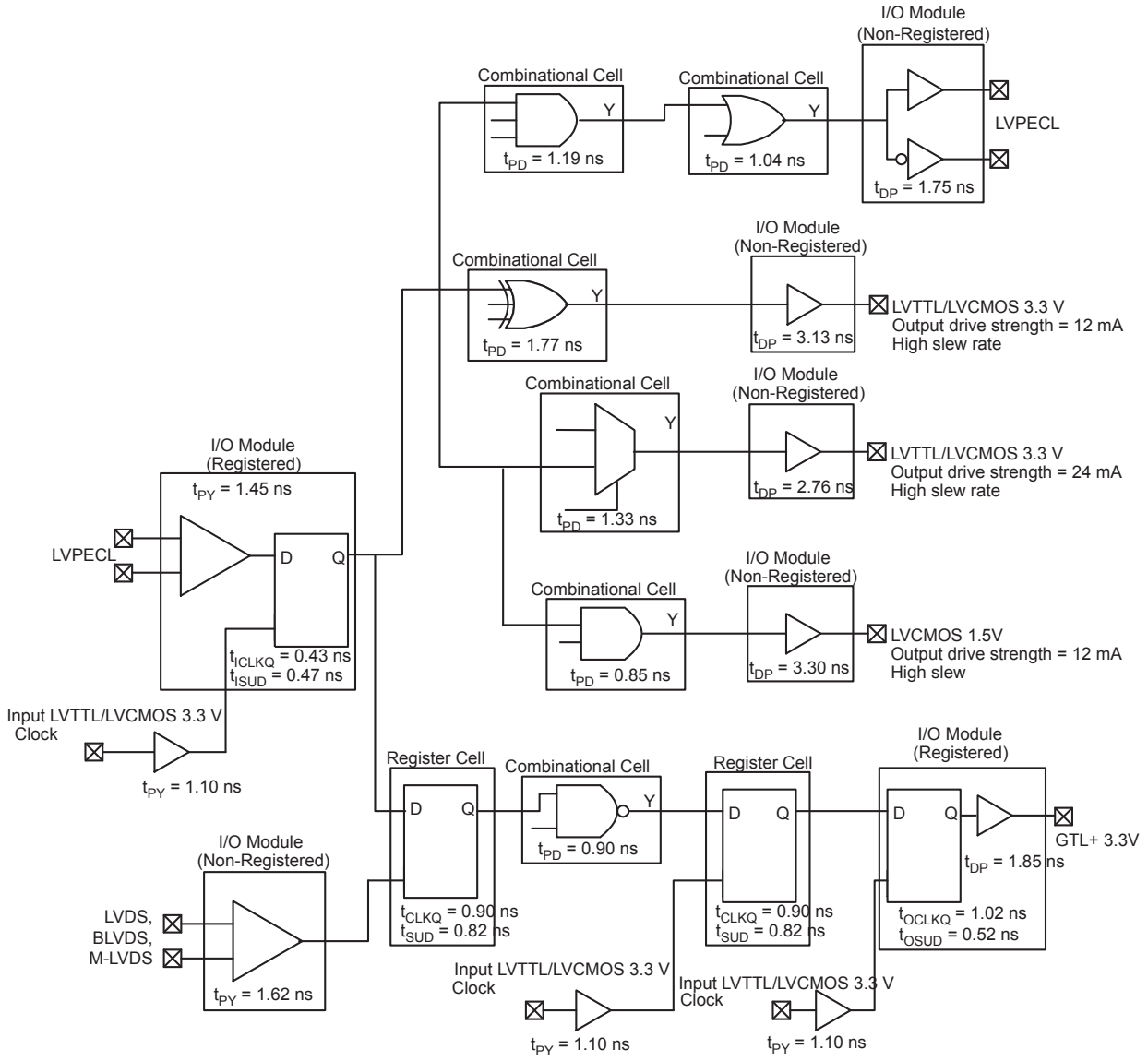

Figure 2-3 • **Timing Model**
Operating Conditions: Std. Speed, Commercial Temperature Range (T_J = 70°C), Worst-Case VCC = 1.425 V, Applicable to 1.5 V DC Core Voltage, V2 and V5 devices

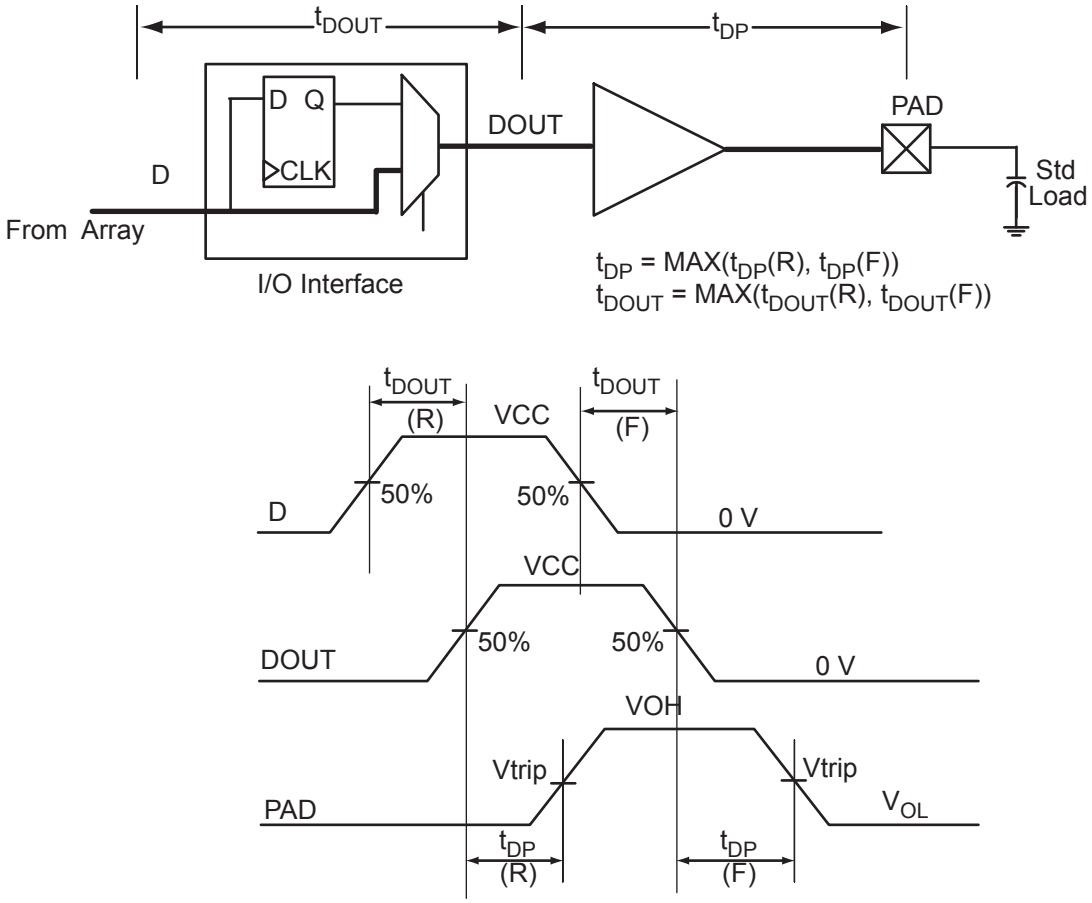

Figure 2-5 • **Output Buffer Model and Delays (example)**

Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels (continued) Applicable to Commercial and Industrial Conditions

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength[2]	Slew Rate	VIL		VIH		VOL	VOH	IOL[1]	IOH[1]
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
HSTL (II)	15 mA[5]	15 mA[5]	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15
SSTL2 (I)	15 mA	15 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15
SSTL2 (II)	18 mA	18 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18
SSTL3 (I)	14 mA	14 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14
SSTL3 (II)	21 mA	21 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-12 specification.*
4. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*
5. *Output drive strength is below JEDEC specification.*
6. *Output Slew Rates can be extracted from IBIS Models, http://www.microsemi.com/soc/download/ibis/default.aspx.*

**Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings
Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI (per standard)**

I/O Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option[1] (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12	12	High	5	–	0.97	2.12	0.18	1.08	1.34	0.66	2.17	1.69	2.71	3.08	5.76	5.28	ns
3.3 V LVCMOS Wide Range[1, 2]	100 µA	12	High	5	–	0.97	2.96	0.18	1.42	1.84	0.66	2.98	2.28	3.86	4.36	6.58	5.87	ns
2.5 V LVCMOS	12	12	High	5	–	.097	2.15	0.18	1.31	1.41	0.66	2.20	1.85	2.78	2.98	5.80	5.45	ns
1.8 V LVCMOS	12	12	High	5	–	0.97	2.37	0.18	1.27	1.59	0.66	2.42	2.03	3.07	3.57	6.02	5.62	ns
1.5 V LVCMOS	12	12	High	5	–	0.97	2.69	0.18	1.47	1.77	0.66	2.75	2.30	3.24	3.67	6.35	5.89	ns
3.3 V PCI	Per PCI spec	–	High	10	25 [3]	0.97	2.38	0.18	0.96	1.42	0.66	2.43	1.80	2.72	3.08	6.03	5.39	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 [3]	0.97	2.38	0.19	0.92	1.34	0.66	2.43	1.80	2.72	3.08	6.03	5.39	ns
3.3 V GTL	20[4]	–	High	10	25	0.97	1.78	0.19	2.35	–	0.66	1.80	1.78	–	–	5.39	5.38	ns
2.5 V GTL	20[4]	–	High	10	25	0.97	1.85	0.19	1.98	–	0.66	1.89	1.82	–	–	5.49	5.42	ns
3.3 V GTL+	35	–	High	10	25	0.97	1.80	0.19	1.32	–	0.66	1.84	1.77	–	–	5.44	5.36	ns
2.5 V GTL+	33	–	High	10	25	0.97	1.92	0.19	1.26	–	0.66	1.96	1.80	–	–	5.56	5.40	ns
HSTL (I)	8	–	High	20	50	0.97	2.67	0.18	1.72	–	0.66	2.72	2.67	–	–	6.32	6.26	ns
HSTL (II)	15	–	High	20	25	0.97	2.55	0.18	1.72	–	0.66	2.60	2.34	–	–	6.20	5.93	ns
SSTL2 (I)	15	–	High	30	50	0.97	1.86	0.19	1.12	–	0.66	1.90	1.68	–	–	5.50	5.28	ns
SSTL2 (II)	18	–	High	30	25	0.97	1.89	0.19	1.12	–	0.66	1.93	1.62	–	–	5.53	5.22	ns
SSTL3 (I)	14	–	High	30	50	0.97	2.00	0.19	1.06	–	0.66	2.04	1.67	–	–	5.64	5.27	ns
SSTL3 (II)	21	–	High	30	25	0.97	1.81	0.19	1.06	–	0.66	1.85	1.55	–	–	5.45	5.14	ns
LVDS	24	–	High	–	–	0.97	1.73	0.19	1.62	–	–	–	–	–	–	–	–	ns
LVPECL	24	–	High	–	–	0.97	1.65	0.18	1.42	–	–	–	–	–	–	–	–	ns

Notes:

1. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
3. *Resistance is used to measure I/O propagation delays as defined in PCI Specifications. See Figure 2-12 on page 2-49 for connectivity. This resistor is not required during normal operation.*
4. *Output drive strength is below JEDEC specification.*
5. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-31 • **Duration of Short Circuit Event before Failure**

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months

Table 2-32 • **Schmitt Trigger Input Hysteresis**
Hysteresis Voltage Value (Typ.) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV
1.2 V LVCMOS (Schmitt trigger mode)	40 mV

Table 2-33 • **I/O Input Rise Time, Fall Time, and Related I/O Reliability***

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns*	20 years (100°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis.	20 years (100°C)
HSTL/SSTL/GTL	No requirement	10 ns*	10 years (100°C)
LVDS/B-LVDS/M-LVDS/LVPECL	No requirement	10 ns*	10 years (100°C)

*Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-46 • Minimum and Maximum DC Input and Output Levels

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	65	74	10	10
16 mA	–0.3	0.7	1.7	3.6	0.7	1.7	16	16	83	87	10	10
24 mA	–0.3	0.7	1.7	3.6	0.7	1.7	24	24	169	124	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

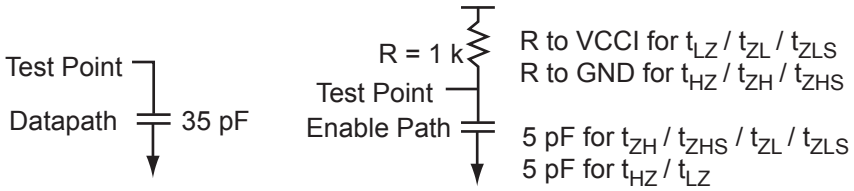

Figure 2-8 • AC Loading

Table 2-47 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	5

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-54 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	7.33	0.18	1.27	1.59	0.66	7.47	6.18	2.34	1.18	11.07	9.77	ns
4 mA	Std.	0.97	6.07	0.18	1.27	1.59	0.66	6.20	5.25	2.69	2.42	9.79	8.84	ns
6 mA	Std.	0.97	5.18	0.18	1.27	1.59	0.66	5.29	4.61	2.93	2.88	8.88	8.21	ns
8 mA	Std.	0.97	4.88	0.18	1.27	1.59	0.66	4.98	4.48	2.99	3.01	8.58	8.08	ns
12 mA	Std.	0.97	4.80	0.18	1.27	1.59	0.66	4.89	4.49	3.07	3.47	8.49	8.09	ns
16 mA	Std.	0.97	4.80	0.18	1.27	1.59	0.66	4.89	4.49	3.07	3.47	8.49	8.09	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-55 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	3.43	0.18	1.27	1.59	0.66	3.51	3.39	2.33	1.19	7.10	6.98	ns
4 mA	Std.	0.97	2.83	0.18	1.27	1.59	0.66	2.89	2.59	2.69	2.49	6.48	6.18	ns
6 mA	Std.	0.97	2.45	0.18	1.27	1.59	0.66	2.51	2.19	2.93	2.95	6.10	5.79	ns
8 mA	Std.	0.97	2.38	0.18	1.27	1.59	0.66	2.43	2.12	2.98	3.08	6.03	5.71	ns
12 mA	Std.	0.97	2.37	0.18	1.27	1.59	0.66	2.42	2.03	3.07	3.57	6.02	5.62	ns
16 mA	Std.	0.97	2.37	0.18	1.27	1.59	0.66	2.42	2.03	3.07	3.57	6.02	5.62	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

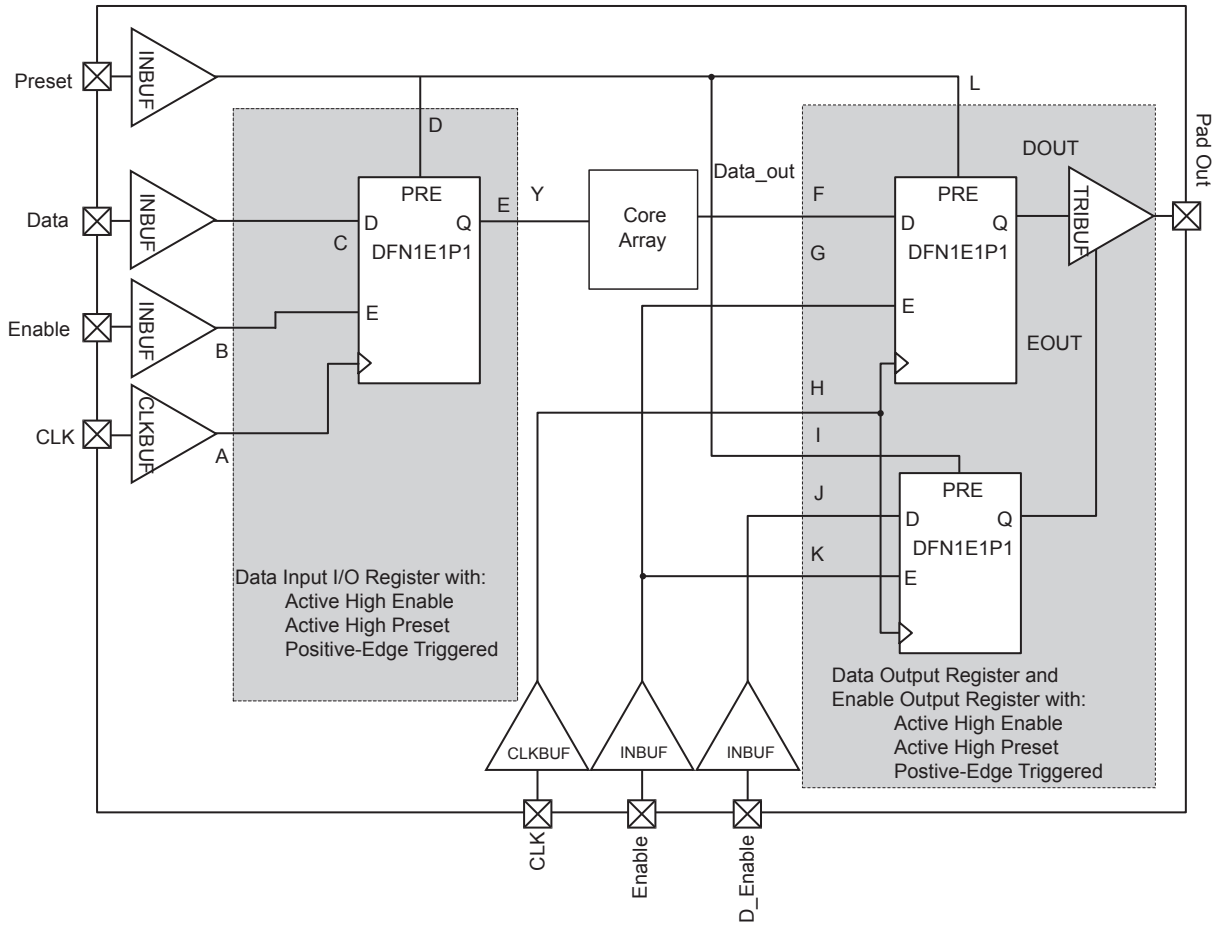

Figure 2-26 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

***Table 2-121* • Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: See Figure 2-26 on page 2-66 for more information.

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

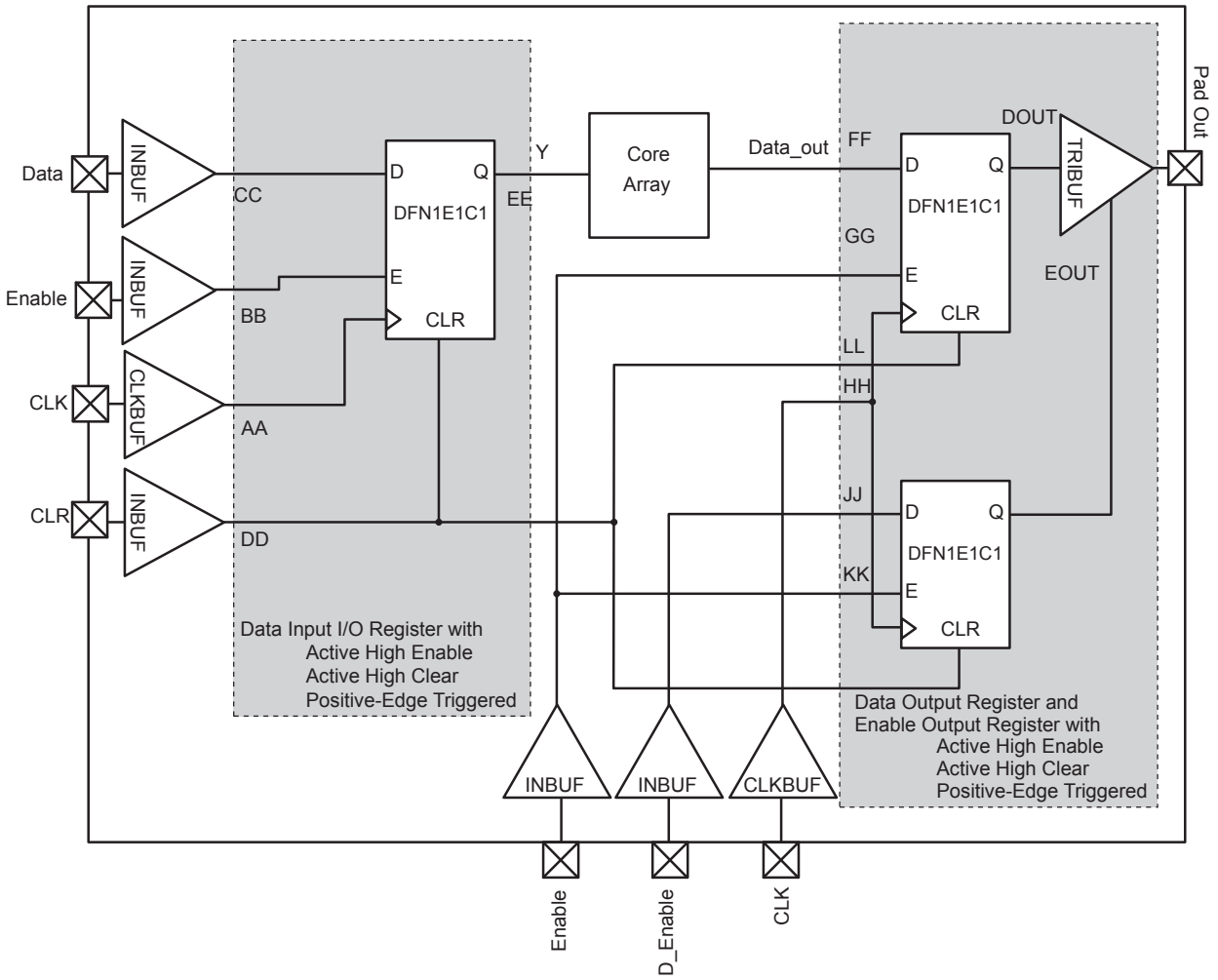

Figure 2-27 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

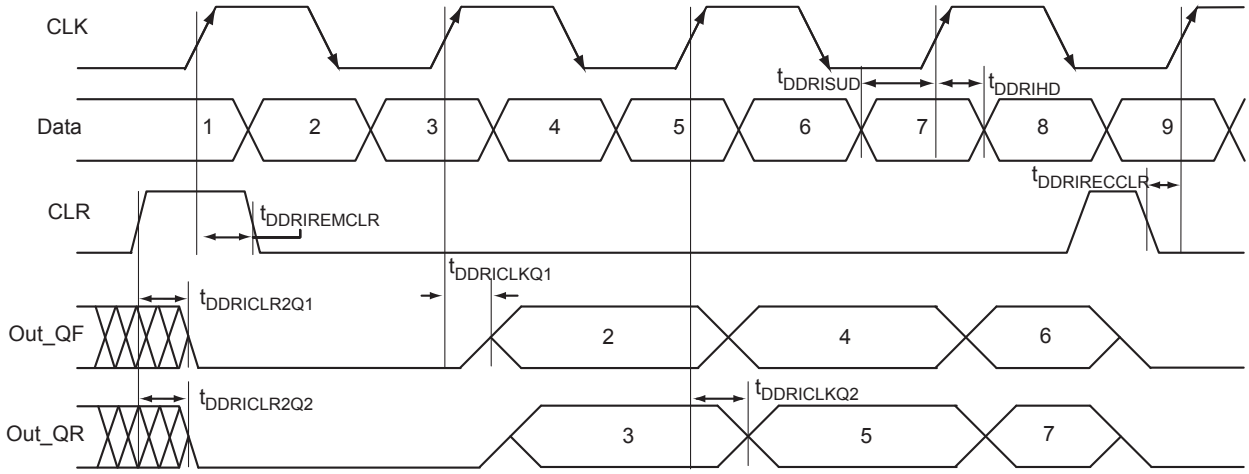

Figure 2-32 • **Input DDR Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-130 • **Input DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.48	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.65	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (negedge)	0.50	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (posedge)	0.40	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (negedge)	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (posedge)	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear to Out Out_QR for Input DDR	0.82	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.98	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.23	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

FG484	
Pin Number	AGLE600 Function
A1	GND
A2	GND
A3	VCCIB0
A4	IO06NDB0V1
A5	IO06PDB0V1
A6	IO08NDB0V1
A7	IO08PDB0V1
A8	IO11PDB0V1
A9	IO17PDB0V2
A10	IO18NDB0V2
A11	IO18PDB0V2
A12	IO22PDB1V0
A13	IO26PDB1V0
A14	IO29NDB1V1
A15	IO29PDB1V1
A16	IO31NDB1V1
A17	IO31PDB1V1
A18	IO32NDB1V1
A19	NC
A20	VCCIB1
A21	GND
A22	GND
AA1	GND
AA2	VCCIB6
AA3	NC
AA4	IO98PDB5V2
AA5	IO96NDB5V2
AA6	IO96PDB5V2
AA7	IO86NDB5V0
AA8	IO86PDB5V0
AA9	IO85PDB5V0
AA10	IO85NDB5V0
AA11	IO78PPB4V1
AA12	IO79NDB4V1
AA13	IO79PDB4V1

FG484	
Pin Number	AGLE600 Function
AA14	NC
AA15	NC
AA16	IO71NDB4V0
AA17	IO71PDB4V0
AA18	NC
AA19	NC
AA20	NC
AA21	VCCIB3
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB5
AB4	IO97NDB5V2
AB5	IO97PDB5V2
AB6	IO93NDB5V1
AB7	IO93PDB5V1
AB8	IO87NDB5V0
AB9	IO87PDB5V0
AB10	NC
AB11	NC
AB12	IO75NDB4V1
AB13	IO75PDB4V1
AB14	IO72NDB4V0
AB15	IO72PDB4V0
AB16	IO73NDB4V0
AB17	IO73PDB4V0
AB18	NC
AB19	NC
AB20	VCCIB4
AB21	GND
AB22	GND
B1	GND
B2	VCCIB7
B3	NC
B4	IO03NDB0V0

FG484	
Pin Number	AGLE600 Function
B5	IO03PDB0V0
B6	IO07NDB0V1
B7	IO07PDB0V1
B8	IO11NDB0V1
B9	IO17NDB0V2
B10	IO14PDB0V2
B11	IO19PDB0V2
B12	IO22NDB1V0
B13	IO26NDB1V0
B14	NC
B15	NC
B16	IO30NDB1V1
B17	IO30PDB1V1
B18	IO32PDB1V1
B19	NC
B20	NC
B21	VCCIB2
B22	GND
C1	VCCIB7
C2	NC
C3	NC
C4	NC
C5	GND
C6	IO04NDB0V0
C7	IO04PDB0V0
C8	VCC
C9	VCC
C10	IO14NDB0V2
C11	IO19NDB0V2
C12	NC
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC

FG896	
Pin Number	AGLE3000 Function
A2	GND
A3	GND
A4	IO14NPB0V1
A5	GND
A6	IO07NPB0V0
A7	GND
A8	IO09NDB0V1
A9	IO17NDB0V2
A10	IO17PDB0V2
A11	IO21NDB0V2
A12	IO21PDB0V2
A13	IO33NDB0V4
A14	IO33PDB0V4
A15	IO35NDB0V4
A16	IO35PDB0V4
A17	IO41NDB1V0
A18	IO43NDB1V0
A19	IO43PDB1V0
A20	IO45NDB1V0
A21	IO45PDB1V0
A22	IO57NDB1V2
A23	IO57PDB1V2
A24	GND
A25	IO69PPB1V3
A26	GND
A27	GBC1/IO79PPB1V4
A28	GND
A29	GND
AA1	IO256PDB6V2
AA2	IO248PDB6V1
AA3	IO248NDB6V1
AA4	IO246NDB6V1
AA5	GEA1/IO234PDB6V0
AA6	GEA0/IO234NDB6V0
AA7	IO243PPB6V1

FG896	
Pin Number	AGLE3000 Function
AA8	IO245NDB6V1
AA9	GEB1/IO235PPB6V0
AA10	VCC
AA11	IO226PPB5V4
AA12	VCCIB5
AA13	VCCIB5
AA14	VCCIB5
AA15	VCCIB5
AA16	VCCIB4
AA17	VCCIB4
AA18	VCCIB4
AA19	VCCIB4
AA20	IO174PDB4V2
AA21	VCC
AA22	IO142NPB3V3
AA23	IO144NDB3V3
AA24	IO144PDB3V3
AA25	IO146NDB3V4
AA26	IO146PDB3V4
AA27	IO147PDB3V4
AA28	IO139NDB3V3
AA29	IO139PDB3V3
AA30	IO133NDB3V2
AB1	IO256NDB6V2
AB2	IO244PDB6V1
AB3	IO244NDB6V1
AB4	IO241PDB6V0
AB5	IO241NDB6V0
AB6	IO243NPB6V1
AB7	VCCIB6
AB8	VCCPLE
AB9	VCC
AB10	IO222PDB5V3
AB11	IO218PPB5V3
AB12	IO206NDB5V1

FG896	
Pin Number	AGLE3000 Function
AB13	IO206PDB5V1
AB14	IO198NDB5V0
AB15	IO198PDB5V0
AB16	IO192NDB4V4
AB17	IO192PDB4V4
AB18	IO178NDB4V3
AB19	IO178PDB4V3
AB20	IO174NDB4V2
AB21	IO162NPB4V1
AB22	VCC
AB23	VCCPLD
AB24	VCCIB3
AB25	IO150PDB3V4
AB26	IO148PDB3V4
AB27	IO147NDB3V4
AB28	IO145PDB3V3
AB29	IO143PDB3V3
AB30	IO137PDB3V2
AC1	IO254PDB6V2
AC2	IO254NDB6V2
AC3	IO240PDB6V0
AC4	GEC1/IO236PDB6V0
AC5	IO237PDB6V0
AC6	IO237NDB6V0
AC7	VCOMPLE
AC8	GND
AC9	IO226NPB5V4
AC10	IO222NDB5V3
AC11	IO216NPB5V2
AC12	IO210NPB5V2
AC13	IO204NDB5V1
AC14	IO204PDB5V1
AC15	IO194NDB5V0
AC16	IO188NDB4V4
AC17	IO188PDB4V4

Revision	Changes	Page
Revision 10 (April 2012)	In Table 2-2 • Recommended Operating Conditions 1, VPUMP programming voltage for operation was changed from "0 to 3.45 V" to "0 to 3.6 V" (SAR 32256). Values for VCCPLL at 1.2–1.5 V DC core supply voltage were changed from "1.14 to 1.26 V" to "1.14 to 1.575 V" (SAR 34701).	2-2
	The tables in the "Quiescent Supply Current" section were updated with revised notes on IDD. Table 2-8 • Power Supply State per Mode is new (SARs 34745, 36949).	2-7
	t_{DOUT} was corrected to t_{DIN} in Figure 2-4 • Input Buffer Timing Model and Delays (example) (SAR 37105).	2-17
	"TBD" for 3.3 V LVCMOS Wide Range in Table 2-28 • I/O Output Buffer Maximum Resistances1 and Table 2-30 • I/O Short Currents IOSH/IOSL was replaced by "Same as regular 3.3 V LVCMOS" (SAR 33855). Values were also added for 1.2 V LVCMOS and 1.2 V LVCMOS Wide Range.	2-28, 2-30
	The formulas in the table notes for Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 34753).	2-29
	IOSH and IOSL values were added to 3.3 V LVCMOS Wide Range Table 2-40 • Minimum and Maximum DC Input and Output Levels, 1.2 V LVCMOS Table 2-64 • Minimum and Maximum DC Input and Output Levels, and 1.2 V LVCMOS Wide Range Table 2-68 • Minimum and Maximum DC Input and Output Levels (SAR 33855).	2-35, 2-47, 2-48
	Figure 2-48 • FIFO Read and Figure 2-49 • FIFO Write have been added (SAR 34844).	2-103
	Values for $F_{DDRIMAX}$ and F_{DDOMAX} were added to the tables in the Input DDR "Timing Characteristics" section and Output DDR "Timing Characteristics" section (SAR 34802).	2-77,2-81
	Minimum pulse width High and Low values were added to the tables in the "Global Tree Timing Characteristics" section. The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 36952).	2-89
Revision 9 (March 2012)	The "In-System Programming (ISP) and Security" section and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 34665).	I, 1-2
	The Y security option and Licensed DPA Logo were added to the "IGLOOe Ordering Information" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 34725).	III
	The following sentence was removed from the "Advanced Architecture" section: "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOOe devices via an IEEE 1532 JTAG interface" (SAR 34685).	1-3
	The "Specifying I/O States During Programming" section is new (SAR 34696).	1-7
	Values for VCCPLL at 1.5 V DC core supply voltage were changed from "1.4 to 1.6 V" to "1.425 to 1.575 V" in Table 2-2 • Recommended Operating Conditions 1 (SAR 32292).	2-2
	The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Contribution—PCLOCK" section, was corrected to the "Spine Architecture" section of the Global Resources chapter in the *IGLOOe FPGA Fabric User's Guide* (SAR 34731).	2-13

Revision	Changes	Page
Revision 3 (cont'd)	Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings1 was updated to change PDC3 to PDC7. The table notes were updated to reflect that power was measured on VCCI. Table note 4 is new.	2-10
	Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO Devices and Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO Devices were updated to add PDC6 and PDC7, and to change the definition for PDC5 to bank quiescent power.	2-11, 2-12
	A table subtitle was added for Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO Devices.	2-12
	The "Total Static Power Consumption—PSTAT" section was updated to revise the calculation of P_{STAT}, including PDC6 and PDC7.	2-13
	Footnote 1 was updated to include information about P_{AC13}. The PLL Contribution equation was changed from: $P_{PLL} = P_{AC13} + P_{AC14} * FCLKOUT$ to $PPLL = P_{DC4} + P_{AC13} * F_{CLKOUT}$.	2-14
	The "Timing Model" was updated to be consistent with the revised timing numbers.	2-16
	In Table 2-22 • Summary of Maximum and Minimum DC Input Levels, T_J was changed to T_A in notes 1 and 2.	2-22
	Table 2-22 • Summary of Maximum and Minimum DC Input Levels was updated to included a hysteresis value for 1.2 V LVCMOS (Schmitt trigger mode).	2-22
	All AC Loading figures for single-ended I/O standards were changed from Datapaths at 35 pF to 5 pF.	N/A
	The "1.2 V LVCMOS (JESD8-12A)" section is new.	2-47
Revision 2 (Jun 2008) Product Brief v1.0	The product brief section of the datasheet was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.	N/A
Revision 2 (cont'd) Packaging v1.1	The naming conventions changed for the following pins in the "FG484" for the A3GLE600: Pin Number — New Function Name J19 — IO45PPB2V1 K20 — IO45NPB2V1 M2 — IO114NPB6V1 N1 — IO114PPB6V1 N4 — GFC2/IO115PPB6V1 P3 — IO115NPB6V1	4-6
Revision 1 (Mar 2008) Product Brief rev. 1	The "Low Power" section was updated to change "1.2 V and 1.5 V Core Voltage" to "1.2 V and 1.5 V Core and I/O Voltage." The text "(from 25 µW)" was removed from "Low Power Active FPGA Operation." 1.2_V was added to the list of core and I/O voltages in the "Pro (Professional) I/O" and "Pro I/Os with Advanced I/O Standards" section sections.	I I, 1-7
Revision 0 (Jan 2008)	This document was previously in datasheet Advance v0.4. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is 51700096-001-0.	N/A