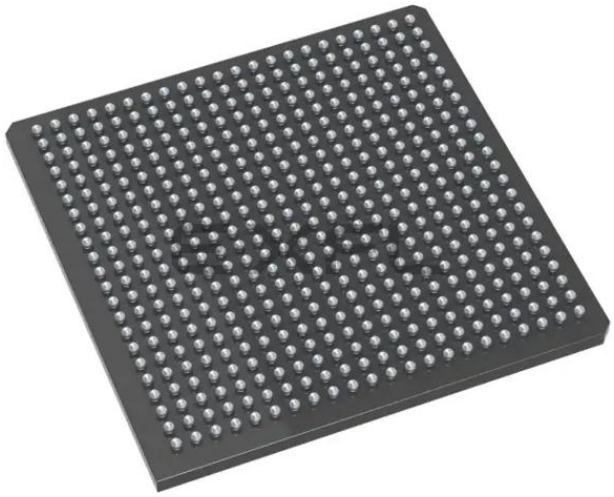
# Microchip Technology - M1AGLE3000V2-FG484I Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 75264 |
| Total RAM Bits | 516096 |
| Number of I/O | 341 |
| Number of Gates | 3000000 |
| Voltage - Supply | 1.14V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m1agle3000v2-fg484i |

### Pro I/Os with Advanced I/O Standards

The IGLOOe family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V). IGLOOe FPGAs support 19 different I/O standards, including single-ended, differential, and voltage-referenced. The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported. Each I/O bank is subdivided into VREF minibanks, which are used by voltage-referenced I/Os. VREF minibanks contain 8 to 18 I/Os. All the I/Os in a given minibank share a common VREF line. Therefore, if any I/O in a given VREF minibank is configured as a VREF pin, the remaining I/Os in that minibank will be able to use that reference voltage.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications (e.g., PCI 66 MHz, bidirectional SSTL 2 and 3, Class I and II)
- Double-Data-Rate applications (e.g., DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications, and DDR 200 MHz SRAM using bidirectional HSTL Class II).

IGLOOe banks support M-LVDS with 20 multi-drop points.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

## Wide Range I/O Support

IGLOOe devices support JEDEC-defined wide range I/O operation. IGLOOe devices support both the JESD8-B specification, covering 3.0 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

## Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click **PDB Configuration**. A FlashPoint – Programming File Generator window appears.
3. Click the **Specify I/O States During Programming** button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-4 on page 1-8).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

   Z -Tri-State: I/O is tristated

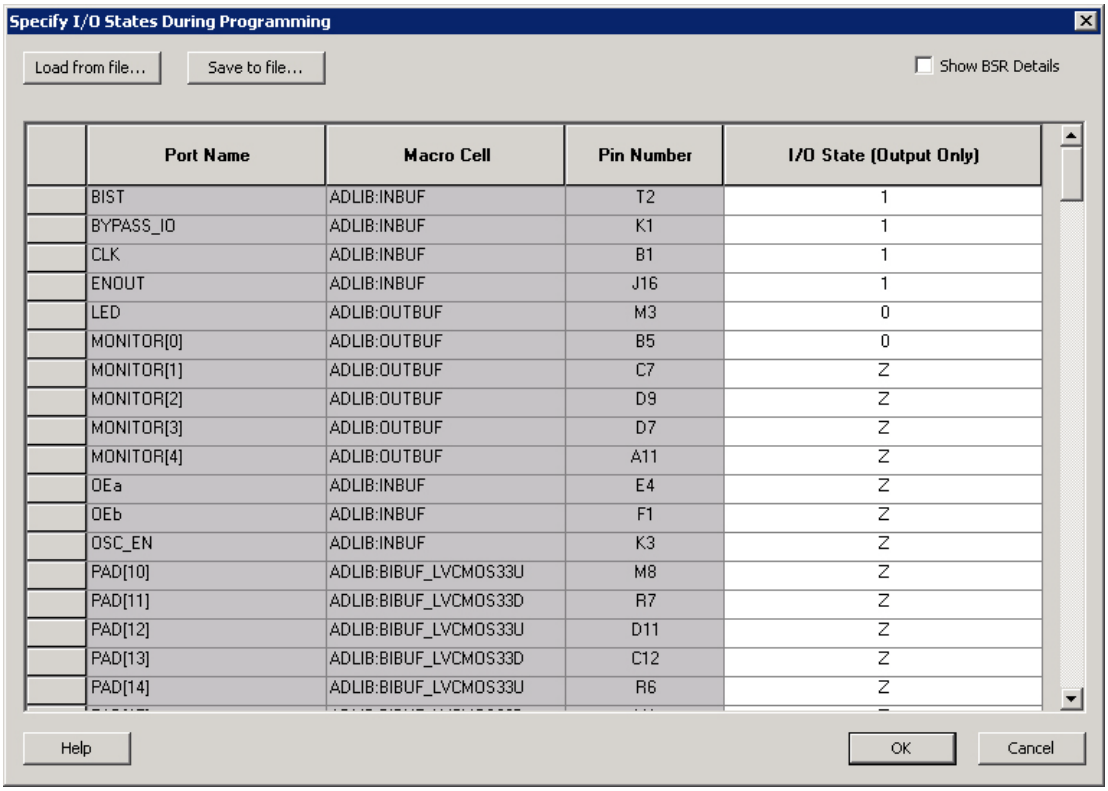



***Figure 1-4 •*** **I/O States During Programming Window**

6. Click OK to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

**Table 2-12 • Quiescent Supply Current (IDD) Characteristics, No Flash*Freeze Mode[1]**

| | Core Voltage | AGLE600 | AGLE3000 | Units |
|---|---|---|---|---|
| **ICCA Current[2]** | | | | |
| Typical (25°C) | 1.2 V | 28 | 89 | µA |
| | 1.5 V | 82 | 320 | µA |
| **ICCI or IJTAG Current[3]** | | | | |
| VCCI/VJTAG = 1.2 V (per bank) Typical (25°C) | 1.2 V | 1.7 | 1.7 | µA |
| VCCI/VJTAG = 1.5 V (per bank) Typical (25°C) | 1.2 V / 1.5 V | 1.8 | 1.8 | µA |
| VCCI/VJTAG = 1.8 V (per bank) Typical (25°C) | 1.2 V / 1.5 V | 1.9 | 1.9 | µA |
| VCCI/VJTAG = 2.5 V (per bank) Typical (25°C) | 1.2 V / 1.5 V | 2.2 | 2.2 | µA |
| VCCI/VJTAG= 3.3 V (per bank) Typical (25°C) | 1.2 V / 1.5 V | 2.5 | 2.5 | µA |

*Notes:*

1. *IDD = $N_{BANKS}$ × ICCI + ICCA. JTAG counts as one bank when powered.*
2. *Includes VCC and VPUMP and VCCPLL currents.*
3. *Values do not include I/O static contribution (PDC6 and PDC7).*

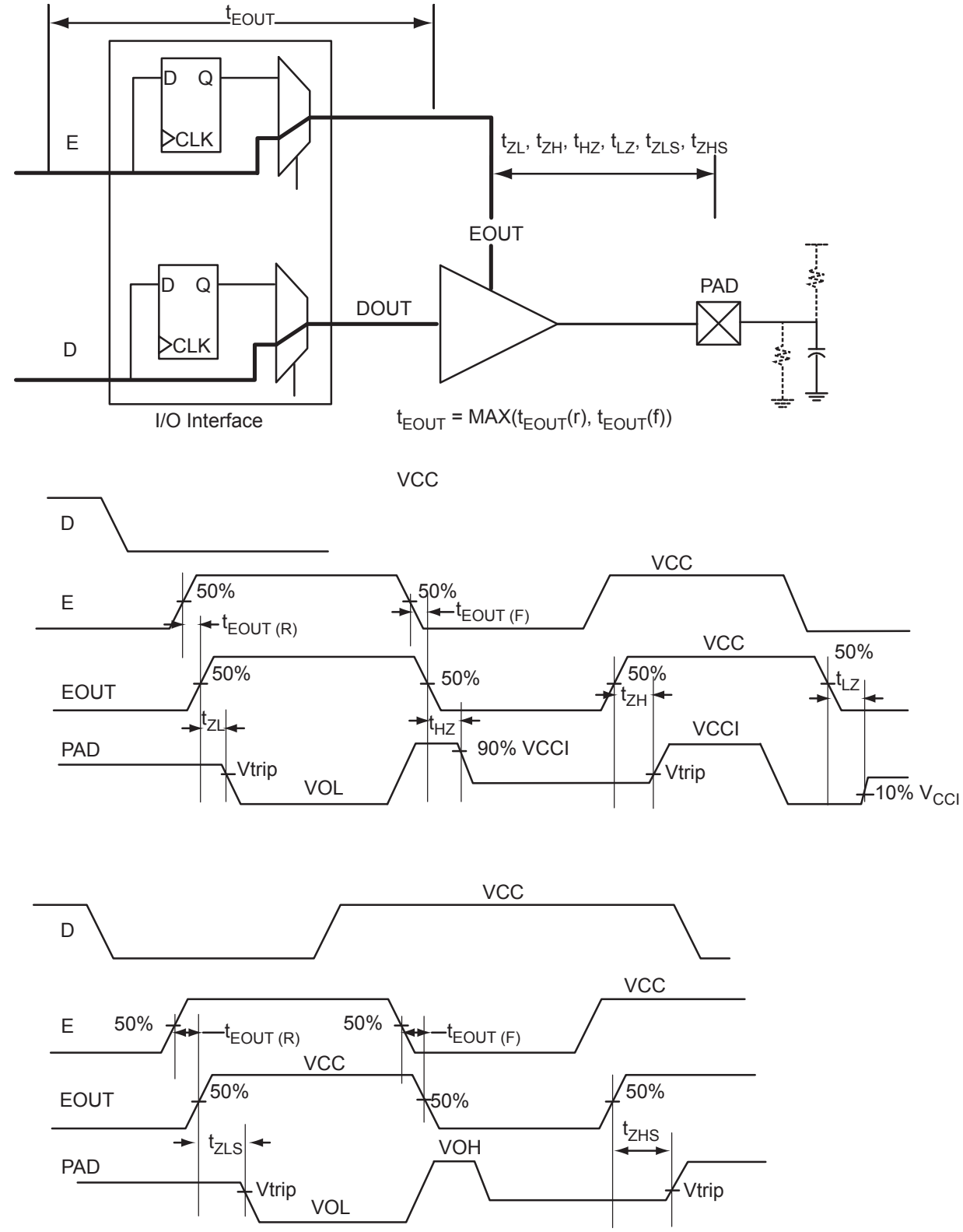



***Figure 2-6 •*** **Tristate Output Buffer Timing Model and Delays (example)**

### 1.2 V DC Core Voltage

**Table 2-50 • 2.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 1.55 | 6.25 | 0.26 | 1.55 | 1.77 | 1.10 | 6.36 | 5.34 | 2.81 | 2.63 | 12.14 | 11.13 | ns |
| 8 mA | Std. | 1.55 | 5.18 | 0.26 | 1.55 | 1.77 | 1.10 | 5.26 | 4.61 | 3.13 | 3.32 | 11.05 | 10.39 | ns |
| 12 mA | Std. | 1.55 | 4.42 | 0.26 | 1.55 | 1.77 | 1.10 | 4.49 | 4.08 | 3.36 | 3.76 | 10.28 | 9.86 | ns |
| 16 mA | Std. | 1.55 | 4.19 | 0.26 | 1.55 | 1.77 | 1.10 | 4.25 | 3.96 | 3.40 | 3.89 | 10.04 | 9.75 | ns |
| 24 mA | Std. | 1.55 | 4.09 | 0.26 | 1.55 | 1.76 | 1.10 | 4.15 | 3.97 | 3.47 | 4.32 | 9.94 | 9.76 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

**Table 2-51 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 1.55 | 3.38 | 0.26 | 1.55 | 1.77 | 1.10 | 3.42 | 3.11 | 2.81 | 2.72 | 9.21 | 8.89 | ns |
| 8 mA | Std. | 1.55 | 2.83 | 0.26 | 1.55 | 1.77 | 1.10 | 2.87 | 2.51 | 3.13 | 3.42 | 8.66 | 8.30 | ns |
| 12 mA | Std. | 1.55 | 2.51 | 0.26 | 1.55 | 1.77 | 1.10 | 2.54 | 2.22 | 3.36 | 3.85 | 8.33 | 8.00 | ns |
| 16 mA | Std. | 1.55 | 2.45 | 0.26 | 1.55 | 1.77 | 1.10 | 2.48 | 2.16 | 3.40 | 3.97 | 8.27 | 7.95 | ns |
| 24 mA | Std. | 1.55 | 2.46 | 0.26 | 1.55 | 1.77 | 1.10 | 2.49 | 2.09 | 3.47 | 4.44 | 8.28 | 7.88 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

### 1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer.

**Table 2-64 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

| 1.2 V LVCMOS[1] | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL[2] | IIH[3] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[4] | Max. mA[4] | µA[5] | µA[5] |
| 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 20 | 26 | 10 | 10 |

*Notes:*

1. *Applicable to V2 devices ONLY.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
4. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

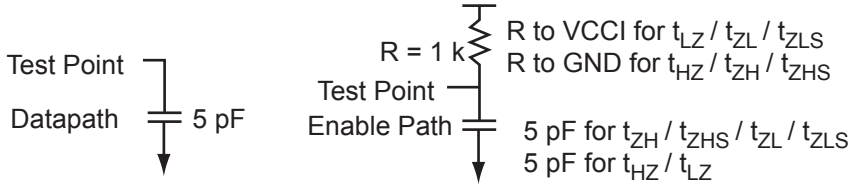



**Figure 2-11 • AC Loading**

**Table 2-65 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|
| 0 | 1.2 | 0.6 | – | 5 |

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

## HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). IGLOOe devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

**Table 2-93 • Minimum and Maximum DC Input and Output Levels**

| HSTL Class II | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 15 mA[5] | –0.3 | VREF – 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI – 0.4 | 15 | 15 | 66 | 55 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Output drive strength is below JEDEC specification.*

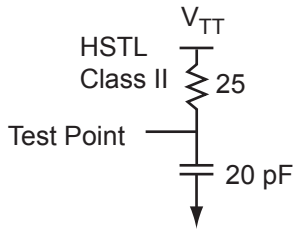



**Figure 2-18 • AC Loading**

**Table 2-94 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|---|
| VREF – 0.1 | VREF + 0.1 | 0.75 | 0.75 | 0.75 | 20 |

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

### Timing Characteristics

#### 1.5 V DC Core Voltage

**Table 2-95 • HSTL Class II – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 1.4 V VREF = 0.75 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.98 | 2.62 | 0.19 | 1.77 | 0.67 | 2.66 | 2.40 | | | 6.29 | 6.03 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

#### 1.2 V DC Core Voltage

**Table 2-96 • HSTL Class II – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 1.4 V VREF = 0.75 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 1.55 | 2.93 | 0.26 | 1.94 | 1.10 | 2.98 | 2.75 | | | 8.79 | 8.55 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

### SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). IGLOOe devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

**Table 2-101 • Minimum and Maximum DC Input and Output Levels**

| SSTL2 Class II | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 18 mA | –0.3 | VREF – 0.2 | VREF + 0.2 | 3.6 | 0.35 | VCCI – 0.43 | 18 | 18 | 169 | 124 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

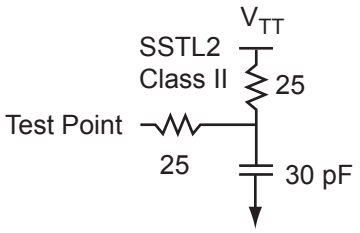



**Figure 2-20 • AC Loading**

**Table 2-102 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input HIGH (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|---|
| VREF – 0.2 | VREF + 0.2 | 1.25 | 1.25 | 1.25 | 30 |

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

## Timing Characteristics

### 1.5 V DC Core Voltage

**Table 2-103 • SSTL 2 Class II – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V,**
**Worst-Case VCCI = 2.3 V VREF = 1.25 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.98 | 1.94 | 0.19 | 1.15 | 0.67 | 1.97 | 1.66 | | | 5.60 | 5.29 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### 1.2 V DC Core Voltage

**Table 2-104 • SSTL 2 Class II – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V,**
**Worst-Case VCCI = 2.3 V VREF = 1.25 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 1.55 | 2.20 | 0.26 | 1.39 | 1.10 | 2.24 | 1.97 | | | 8.05 | 7.78 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

# Differential I/O Characteristics

## Physical Implementation

Configuration of the I/O modules as a differential pair is handled by the Microsemi Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and DDR. However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

## LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-23. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, IGLOOe also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

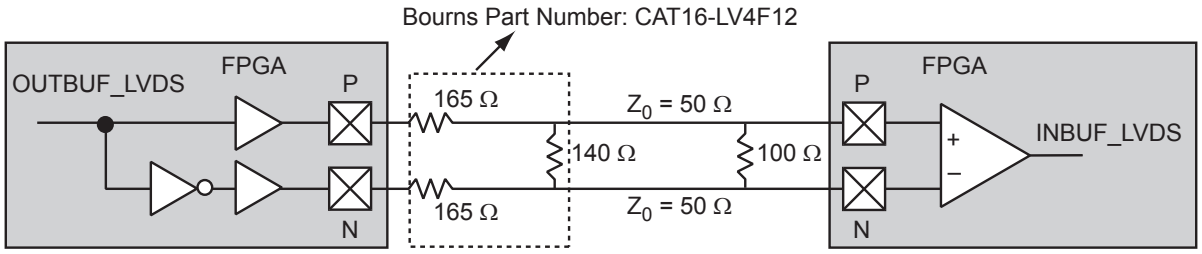



***Figure 2-23 •*** **LVDS Circuit Diagram and Board-Level Implementation**

**Table 2-113 • Minimum and Maximum DC Input and Output Levels**

| DC Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| VCCI | Supply Voltage | 2.375 | 2.5 | 2.625 | V |
| VOL | Output Low Voltage | 0.9 | 1.075 | 1.25 | V |
| VOH | Output High Voltage | 1.25 | 1.425 | 1.6 | V |
| IOL[1] | Output Lower Current | 0.65 | 0.91 | 1.16 | mA |
| IOH[1] | Output High Current | 0.65 | 0.91 | 1.16 | mA |
| VI | Input Voltage | 0 | | 2.925 | V |
| IIH[2,3] | Input High Leakage Current | | | 10 | µA |
| IIL[2,4] | Input Low Leakage Current | | | 10 | µA |
| VODIFF | Differential Output Voltage | 250 | 350 | 450 | mV |
| VOCM | Output Common Mode Voltage | 1.125 | 1.25 | 1.375 | V |
| VICM | Input Common Mode Voltage | 0.05 | 1.25 | 2.35 | V |
| VIDIFF | Input Differential Voltage | 100 | 350 | | mV |

*Notes:*

1. *IOL/IOH is defined by VODIFF/(resistor network).*
2. *Currents are measured at 85°C junction temperature.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
4. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*

**Table 2-114 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) |
|---|---|---|---|
| 1.075 | 1.325 | Cross point | – |

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

## Timing Characteristics

### 1.5 V DC Core Voltage

**Table 2-115 • LVDS – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | Units |
|---|---|---|---|---|---|
| Std. | 0.98 | 1.77 | 0.19 | 1.62 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### 1.2 V DC Core Voltage

**Table 2-116 • LVDS – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | Units |
|---|---|---|---|---|---|
| Std. | 1.55 | 2.19 | 0.26 | 1.88 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

## VersaTile Specifications as a Sequential Module

The IGLOOe library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

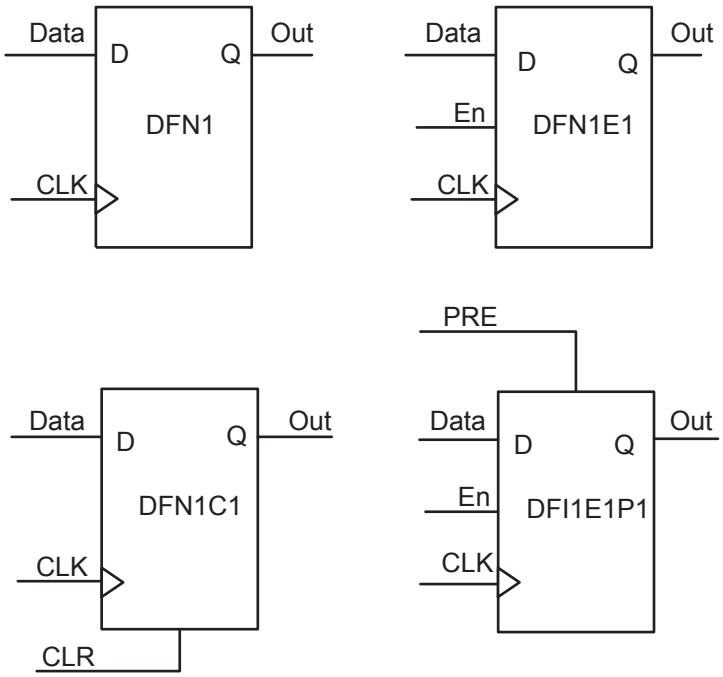



***Figure 2-37 •*** **Sample of Sequential Cells**

## Timing Characteristics

### Applies to 1.5 V DC Core Voltage

**Table 2-145 • RAM4K9**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{AS}$ | Address Setup Time | 0.83 | ns |
| $t_{AH}$ | Address Hold Time | 0.16 | ns |
| $t_{ENS}$ | REN, WEN Setup Time | 0.81 | ns |
| $t_{ENH}$ | REN, WEN Hold Time | 0.16 | ns |
| $t_{BKS}$ | BLK Setup Time | 1.65 | ns |
| $t_{BKH}$ | BLK Hold Time | 0.16 | ns |
| $t_{DS}$ | Input Data (DIN) Setup Time | 0.71 | ns |
| $t_{DH}$ | Input Data (DIN) Hold Time | 0.36 | ns |
| $t_{CKQ1}$ | Clock HIGH to New Data Valid on DOUT (output retained, WMODE = 0) | 3.53 | ns |
| | Clock HIGH to New Data Valid on DOUT (flow-through, WMODE = 1) | 3.06 | ns |
| $t_{CKQ2}$ | Clock HIGH to New Data Valid on DOUT (pipelined) | 1.81 | ns |
| $t_{C2CWWL}$ [1] | Address collision clk-to-clk delay for reliable write after write on same address; applicable to closing edge | 0.23 | ns |
| $t_{C2CRWH}$ [1] | Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge | 0.35 | ns |
| $t_{C2CWRH}$ [1] | Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge | 0.41 | ns |
| $t_{RSTBQ}$ | RESET Low to Data Out Low on DOUT (flow-through) | 2.06 | ns |
| | RESET Low to Data Out Low on DOUT (pipelined) | 2.06 | ns |
| $t_{REMRSTB}$ | RESET Removal | 0.61 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 3.21 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 0.68 | ns |
| $t_{CYC}$ | Clock Cycle Time | 6.24 | ns |
| $F_{MAX}$ | Maximum Frequency | 160 | MHz |

*Notes:*

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## Timing Waveforms

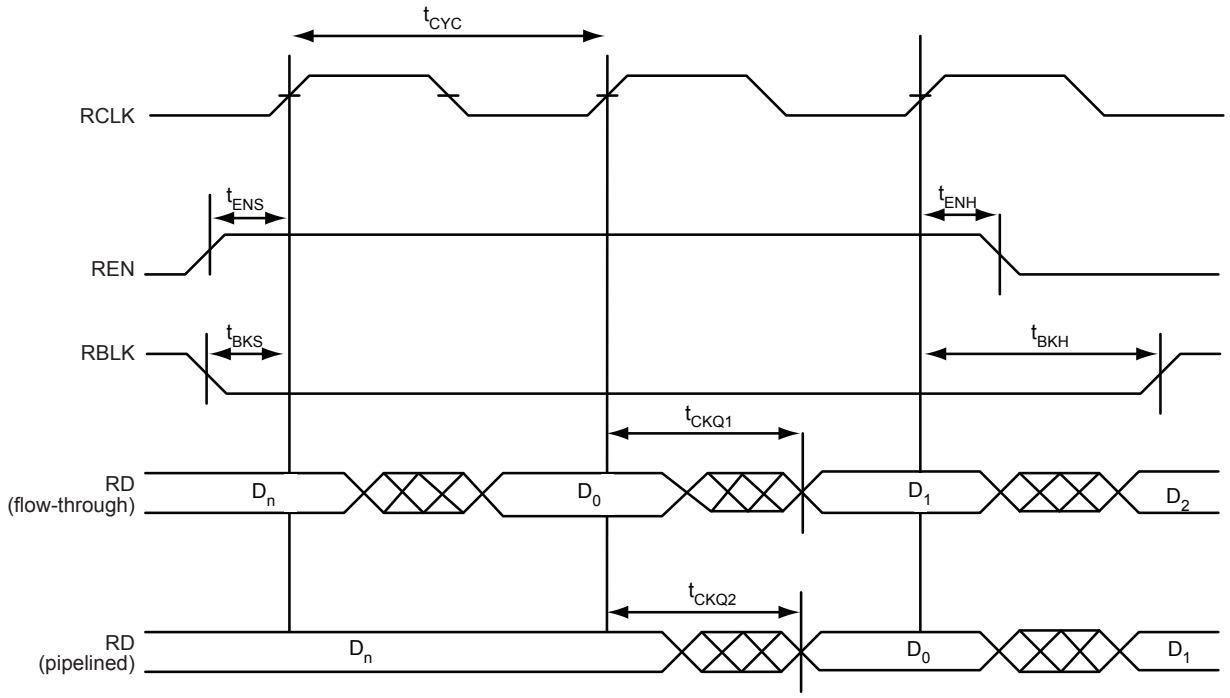



***Figure 2-48 •*** **FIFO Read**

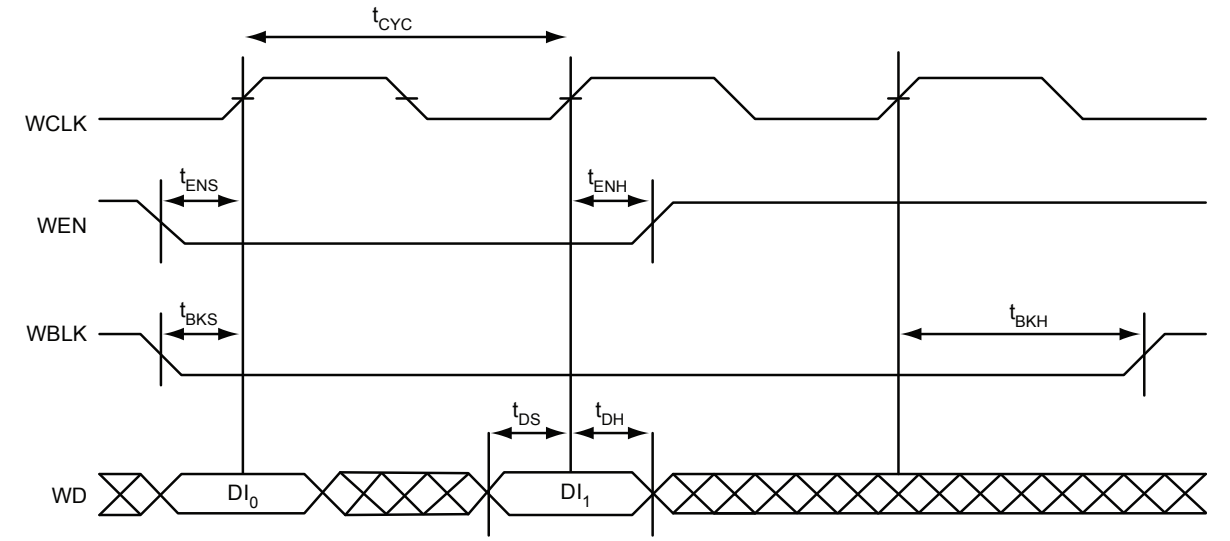



***Figure 2-49 •*** **FIFO Write**

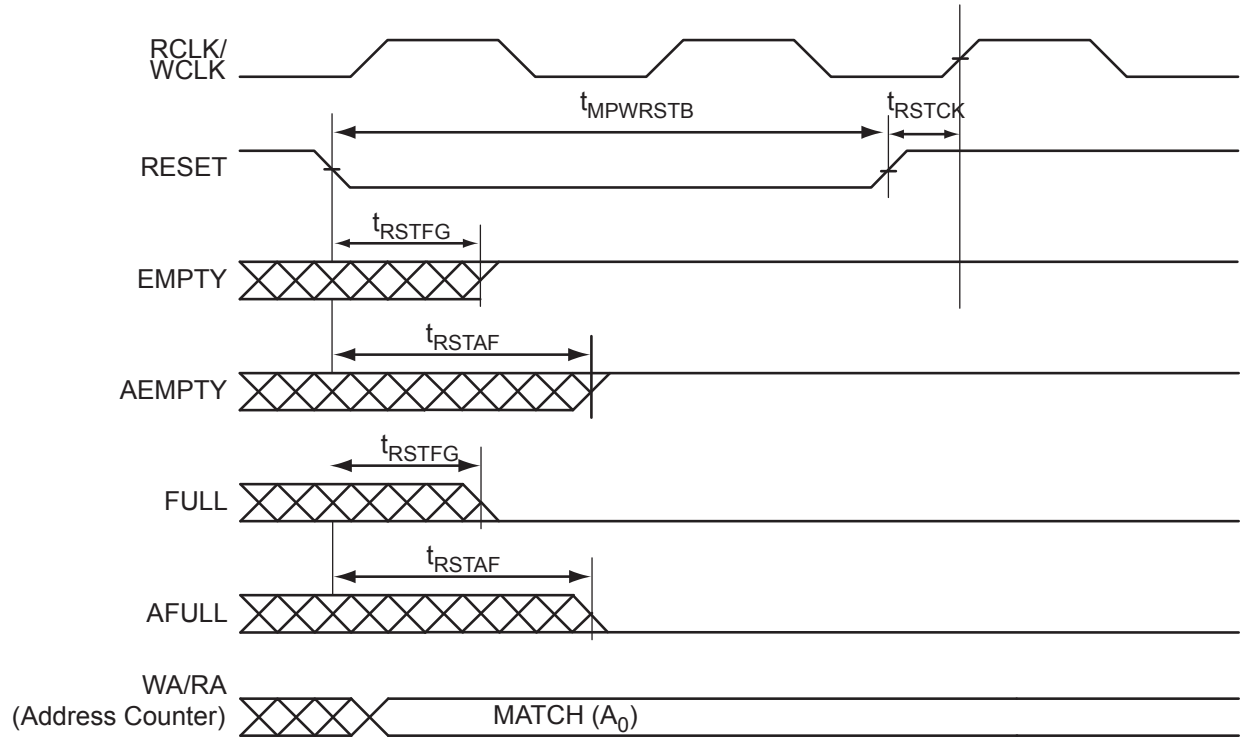



***Figure 2-50 •*** **FIFO Reset**

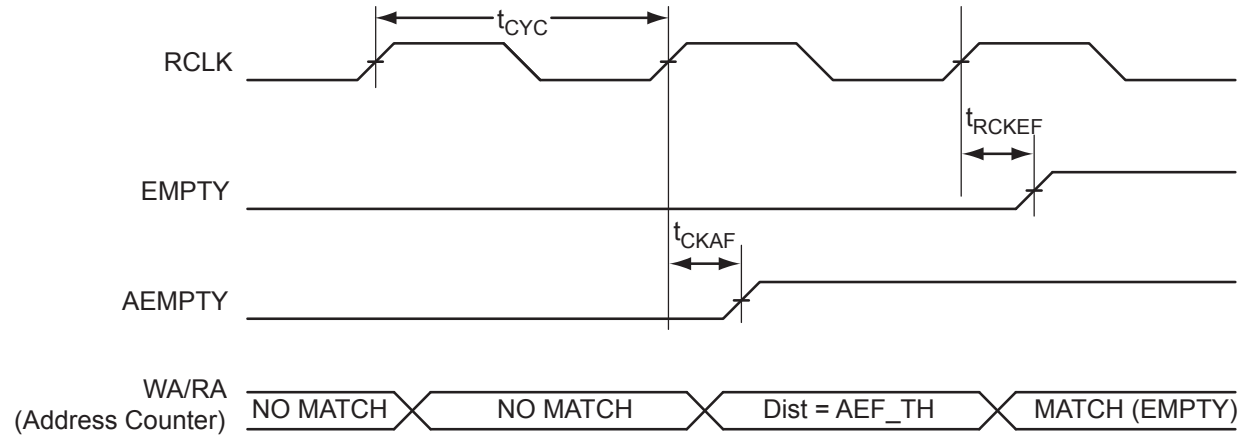



***Figure 2-51 •*** **FIFO EMPTY Flag and AEMPTY Flag Assertion**

## Timing Characteristics

### Applies to 1.5 V DC Core Voltage

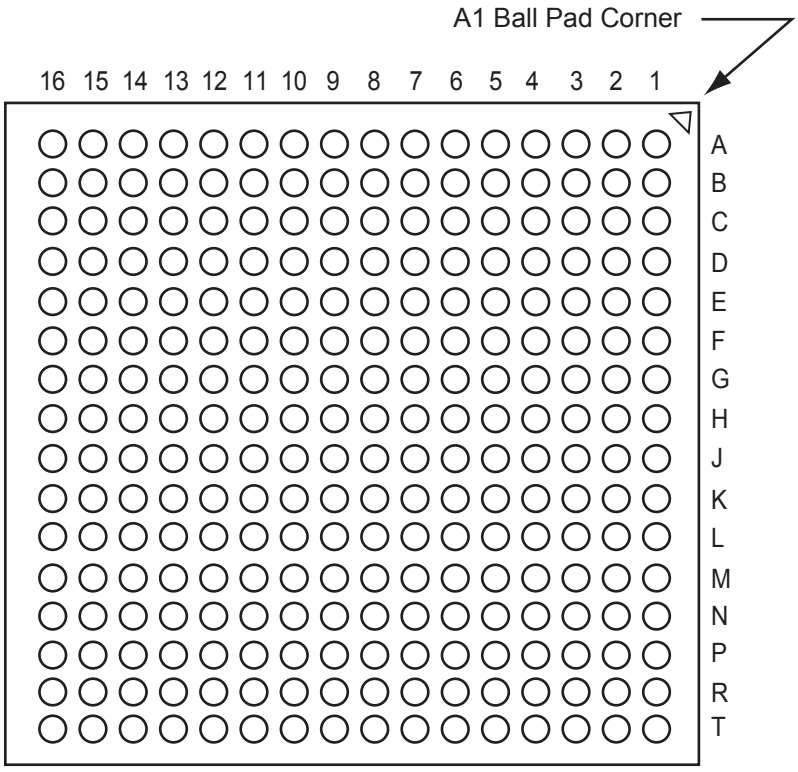
**Table 2-149 • FIFO**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{ENS}$ | REN, WEN Setup Time | 1.99 | ns |
| $t_{ENH}$ | REN, WEN Hold Time | 0.16 | ns |
| $t_{BKS}$ | BLK Setup Time | 0.30 | ns |
| $t_{BKH}$ | BLK Hold Time | 0.00 | ns |
| $t_{DS}$ | Input Data (WD) Setup Time | 0.76 | ns |
| $t_{DH}$ | Input Data (WD) Hold Time | 0.25 | ns |
| $t_{CKQ1}$ | Clock HIGH to New Data Valid on RD (pass-through) | 3.33 | ns |
| $t_{CKQ2}$ | Clock HIGH to New Data Valid on RD (pipelined) | 1.80 | ns |
| $t_{RCKEF}$ | RCLK HIGH to Empty Flag Valid | 3.53 | ns |
| $t_{WCKFF}$ | WCLK HIGH to Full Flag Valid | 3.35 | ns |
| $t_{CKAF}$ | Clock HIGH to Almost Empty/Full Flag Valid | 12.85 | ns |
| $t_{RSTFG}$ | RESET LOW to Empty/Full Flag Valid | 3.48 | ns |
| $t_{RSTAF}$ | RESET LOW to Almost Empty/Full Flag Valid | 12.72 | ns |
| $t_{RSTBQ}$ | RESET LOW to Data Out LOW on RD (pass-through) | 2.02 | ns |
| | RESET LOW to Data Out LOW on RD (pipelined) | 2.02 | ns |
| $t_{REMRSTB}$ | RESET Removal | 0.61 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 3.21 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 0.68 | ns |
| $t_{CYC}$ | Clock Cycle Time | 6.24 | ns |
| $F_{MAX}$ | Maximum Frequency | 160 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

# 4 – Package Pin Assignments

## FG256




*Note: This is the bottom view of the package.*

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

| FG256 | |
|---|---|
| **Pin Number** | **AGLE600 Function** |
| P9 | IO82PDB5V0 |
| P10 | IO76NDB4V1 |
| P11 | IO76PDB4V1 |
| P12 | VMV4 |
| P13 | TCK |
| P14 | VPUMP |
| P15 | TRST |
| P16 | GDA0/IO67NDB3V1 |
| R1 | GEA1/IO102PDB6V0 |
| R2 | GEA0/IO102NDB6V0 |
| R3 | GNDQ |
| R4 | GEC2/IO99PDB5V2 |
| R5 | IO95NPB5V1 |
| R6 | IO91NDB5V1 |
| R7 | IO91PDB5V1 |
| R8 | IO83NDB5V0 |
| R9 | IO83PDB5V0 |
| R10 | IO77NDB4V1 |
| R11 | IO77PDB4V1 |
| R12 | IO69NDB4V0 |
| R13 | GDB2/IO69PDB4V0 |
| R14 | TDI |
| R15 | GNDQ |
| R16 | TDO |
| T1 | GND |
| T2 | IO100NDB5V2 |
| T3 | FF/GEB2/IO100PDB5V2 |
| T4 | IO99NDB5V2 |
| T5 | IO88NDB5V0 |
| T6 | IO88PDB5V0 |
| T7 | IO89NSB5V0 |
| T8 | IO80NSB4V1 |
| T9 | IO81NDB4V1 |
| T10 | IO81PDB4V1 |
| T11 | IO70NDB4V0 |

| FG256 | |
|---|---|
| **Pin Number** | **AGLE600 Function** |
| T12 | GDC2/IO70PDB4V0 |
| T13 | IO68NDB4V0 |
| T14 | GDA2/IO68PDB4V0 |
| T15 | TMS |
| T16 | GND |

| FG484 | |
|---|---|
| Pin Number | AGLE600 Function |
| C18 | GND |
| C19 | NC |
| C20 | NC |
| C21 | NC |
| C22 | VCCIB2 |
| D1 | NC |
| D2 | NC |
| D3 | NC |
| D4 | GND |
| D5 | GAA0/IO00NDB0V0 |
| D6 | GAA1/IO00PDB0V0 |
| D7 | GAB0/IO01NDB0V0 |
| D8 | IO05PDB0V0 |
| D9 | IO10PDB0V1 |
| D10 | IO12PDB0V2 |
| D11 | IO16NDB0V2 |
| D12 | IO23NDB1V0 |
| D13 | IO23PDB1V0 |
| D14 | IO28NDB1V1 |
| D15 | IO28PDB1V1 |
| D16 | GBB1/IO34PDB1V1 |
| D17 | GBA0/IO35NDB1V1 |
| D18 | GBA1/IO35PDB1V1 |
| D19 | GND |
| D20 | NC |
| D21 | NC |
| D22 | NC |
| E1 | NC |
| E2 | NC |
| E3 | GND |
| E4 | GAB2/IO133PDB7V1 |
| E5 | GAA2/IO134PDB7V1 |
| E6 | GNDQ |
| E7 | GAB1/IO01PDB0V0 |
| E8 | IO05NDB0V0 |

| FG484 | |
|---|---|
| Pin Number | AGLE600 Function |
| E9 | IO10NDB0V1 |
| E10 | IO12NDB0V2 |
| E11 | IO16PDB0V2 |
| E12 | IO20NDB1V0 |
| E13 | IO24NDB1V0 |
| E14 | IO24PDB1V0 |
| E15 | GBC1/IO33PDB1V1 |
| E16 | GBB0/IO34NDB1V1 |
| E17 | GNDQ |
| E18 | GBA2/IO36PDB2V0 |
| E19 | IO42NDB2V0 |
| E20 | GND |
| E21 | NC |
| E22 | NC |
| F1 | NC |
| F2 | IO131NDB7V1 |
| F3 | IO131PDB7V1 |
| F4 | IO133NDB7V1 |
| F5 | IO134NDB7V1 |
| F6 | VMV7 |
| F7 | VCCPLA |
| F8 | GAC0/IO02NDB0V0 |
| F9 | GAC1/IO02PDB0V0 |
| F10 | IO15NDB0V2 |
| F11 | IO15PDB0V2 |
| F12 | IO20PDB1V0 |
| F13 | IO25NDB1V0 |
| F14 | IO27PDB1V0 |
| F15 | GBC0/IO33NDB1V1 |
| F16 | VCCPLB |
| F17 | VMV2 |
| F18 | IO36NDB2V0 |
| F19 | IO42PDB2V0 |
| F20 | NC |
| F21 | NC |

| FG484 | |
|---|---|
| Pin Number | AGLE600 Function |
| F22 | NC |
| G1 | IO127NDB7V1 |
| G2 | IO127PDB7V1 |
| G3 | NC |
| G4 | IO128PDB7V1 |
| G5 | IO129PDB7V1 |
| G6 | GAC2/IO132PDB7V1 |
| G7 | VCOMPLA |
| G8 | GNDQ |
| G9 | IO09NDB0V1 |
| G10 | IO09PDB0V1 |
| G11 | IO13PDB0V2 |
| G12 | IO21PDB1V0 |
| G13 | IO25PDB1V0 |
| G14 | IO27NDB1V0 |
| G15 | GNDQ |
| G16 | VCOMPLB |
| G17 | GBB2/IO37PDB2V0 |
| G18 | IO39PDB2V0 |
| G19 | IO39NDB2V0 |
| G20 | IO43PDB2V0 |
| G21 | IO43NDB2V0 |
| G22 | NC |
| H1 | NC |
| H2 | NC |
| H3 | VCC |
| H4 | IO128NDB7V1 |
| H5 | IO129NDB7V1 |
| H6 | IO132NDB7V1 |
| H7 | IO130PDB7V1 |
| H8 | VMV0 |
| H9 | VCCIB0 |
| H10 | VCCIB0 |
| H11 | IO13NDB0V2 |
| H12 | IO21NDB1V0 |

| FG484 | |
|---|---|
| **Pin Number** | **AGLE600 Function** |
| V3 | GND |
| V4 | GEA1/IO102PDB6V0 |
| V5 | GEA0/IO102NDB6V0 |
| V6 | GNDQ |
| V7 | GEC2/IO99PDB5V2 |
| V8 | IO95NPB5V1 |
| V9 | IO91NDB5V1 |
| V10 | IO91PDB5V1 |
| V11 | IO83NDB5V0 |
| V12 | IO83PDB5V0 |
| V13 | IO77NDB4V1 |
| V14 | IO77PDB4V1 |
| V15 | IO69NDB4V0 |
| V16 | GDB2/IO69PDB4V0 |
| V17 | TDI |
| V18 | GNDQ |
| V19 | TDO |
| V20 | GND |
| V21 | NC |
| V22 | IO63NDB3V1 |
| W1 | NC |
| W2 | NC |
| W3 | NC |
| W4 | GND |
| W5 | IO100NDB5V2 |
| W6 | FF/GEB2/IO100PDB5V2 |
| W7 | IO99NDB5V2 |
| W8 | IO88NDB5V0 |
| W9 | IO88PDB5V0 |
| W10 | IO89NDB5V0 |
| W11 | IO80NDB4V1 |
| W12 | IO81NDB4V1 |
| W13 | IO81PDB4V1 |
| W14 | IO70NDB4V0 |
| W15 | GDC2/IO70PDB4V0 |

| FG484 | |
|---|---|
| **Pin Number** | **AGLE600 Function** |
| W16 | IO68NDB4V0 |
| W17 | GDA2/IO68PDB4V0 |
| W18 | TMS |
| W19 | GND |
| W20 | NC |
| W21 | NC |
| W22 | NC |
| Y1 | VCCIB6 |
| Y2 | NC |
| Y3 | NC |
| Y4 | IO98NDB5V2 |
| Y5 | GND |
| Y6 | IO94NDB5V1 |
| Y7 | IO94PDB5V1 |
| Y8 | VCC |
| Y9 | VCC |
| Y10 | IO89PDB5V0 |
| Y11 | IO80PDB4V1 |
| Y12 | IO78NPB4V1 |
| Y13 | NC |
| Y14 | VCC |
| Y15 | VCC |
| Y16 | NC |
| Y17 | NC |
| Y18 | GND |
| Y19 | NC |
| Y20 | NC |
| Y21 | NC |
| Y22 | VCCIB3 |

# 5 – Datasheet Information

## List of Changes

The following table lists critical changes that were made in each revision of the IGLOOe datasheet.

| Revision | Changes | Page |
|---|---|---|
| Revision 13 (December 2012) | The "IGLOOe Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43176).<br>Also added the missing heading 'Supply Voltage' under V2. | III |
| | The note in Table 2-143 • IGLOOe CCC/PLL Specification and Table 2-144 • IGLOOe CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42568). | 2-91, 2-92 |
| | Live at Power-Up (LAPU) has been replaced with 'Instant On'. | NA |
| Revision 12 (September 2012) | The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data. | 1-2 |
| | Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40272). | N/A |
| Revision 11 (August 2012) | The drive strength, IOL, and IOH value for 3.3 V GTL and 2.5 V GTL was changed from 25 mA to 20 mA in the following tables (SAR 37180):<br>Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels,<br>Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings<br>Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings<br>Table 2-28 • I/O Output Buffer Maximum Resistances1<br>Table 2-73 • Minimum and Maximum DC Input and Output Levels<br>Table 2-77 • Minimum and Maximum DC Input and Output Levels<br>Also added note stating "*Output drive strength is below JEDEC specification.*" for Tables 2-25, 2-26, and 2-28.<br>Additionally, the IOL and IOH values for 3.3 V GTL+ and 2.5 V GTL+ were corrected from 51 to 35 (for 3.3 V GTL+) and from 40 to 33 (for 2.5 V GTL+) in table Table 2-21 (SAR 39713). | 2-20<br>2-25<br>2-26<br>2-28<br>2-51<br>2-53 |
| | In Table 2-117 • Minimum and Maximum DC Input and Output Levels, VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 37183). | 2-65 |
| | The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions and Packaging" section: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38318). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement. | 3-1 |