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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 75264 |
| Total RAM Bits | 516096 |
| Number of I/O | 341 |
| Number of Gates | 3000000 |
| Voltage - Supply | 1.14V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m1agle3000v2-fgg484i |

**Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature[1]**

| Product Grade | Programming Cycles | Program Retention (biased/unbiased) | Maximum Storage Temperature $T_{STG}$ (°C) [2] | Maximum Operating Junction Temperature $T_J$ (°C) [2] |
|---|---|---|---|---|
| Commercial | 500 | 20 years | 110 | 100 |
| Industrial | 500 | 20 years | 110 | 100 |

*Notes:*

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

**Table 2-4 • Overshoot and Undershoot Limits [1, 3]**

| VCCI | Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2] | Maximum Overshoot/ Undershoot[2] |
|---|---|---|
| 2.7 V or less | 10% | 1.4 V |
| | 5% | 1.49 V |
| 3 V | 10% | 1.1 V |
| | 5% | 1.19 V |
| 3.3 V | 10% | 0.79 V |
| | 5% | 0.88 V |
| 3.6 V | 10% | 0.45 V |
| | 5% | 0.54 V |

*Notes:*

1. *Based on reliability requirements at junction temperature at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
3. *This table does not provide PCI overshoot/undershoot limits.*

## I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOOe device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5.

There are five regions to consider during power-up.

IGLOOe I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

**VCCI Trip Point:**
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

**VCC Trip Point:**
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.

## Power per I/O Pin

***Table 2-13 •*** **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings**

| | VCCI (V) | Static Power PDC6 (mW)[1] | Dynamic Power PAC9 (µW/MHz)[2] |
|---|---|---|---|
| **Single-Ended** | | | |
| 3.3 V LVTTL/LVCMOS | 3.3 | – | 16.34 |
| 3.3 V LVTTL/LVCMOS – Schmitt trigger | 3.3 | – | 24.49 |
| 3.3 V LVCMOS Wide Range [3] | 3.3 | – | 16.34 |
| 3.3 V LVCMOS Wide Range – Schmitt trigger [3] | 3.3 | – | 24.49 |
| 2.5 V LVCMOS | 2.5 | – | 4.71 |
| 2.5 V LVCMOS | 2.5 | – | 6.13 |
| 1.8 V LVCMOS | 1.8 | – | 1.66 |
| 1.8 V LVCMOS – Schmitt trigger | 1.8 | – | 1.78 |
| 1.5 V LVCMOS (JESD8-11) | 1.5 | – | 1.01 |
| 1.5 V LVCMOS (JESD8-11) – Schmitt trigger | 1.5 | – | 0.97 |
| 1.2 V LVCMOS [4] | 1.2 | – | 0.60 |
| 1.2 V LVCMOS – Schmitt trigger [4] | 1.2 | – | 0.53 |
| 1.2 V LVCMOS Wide Range [4] | 1.2 | – | 0.60 |
| 1.2 V LVCMOS Wide Range – Schmitt trigger [4] | 1.2 | – | 0.53 |
| 3.3 V PCI | 3.3 | – | 17.76 |
| 3.3 V PCI – Schmitt trigger | 3.3 | – | 19.10 |
| 3.3 V PCI-X | 3.3 | – | 17.76 |
| 3.3 V PCI-X – Schmitt trigger | 3.3 | – | 19.10 |
| **Voltage-Referenced** | | | |
| 3.3 V GTL | 3.3 | 2.90 | 7.14 |
| 2.5 V GTL | 2.5 | 2.13 | 3.54 |
| 3.3 V GTL+ | 3.3 | 2.81 | 2.91 |
| 2.5 V GTL+ | 2.5 | 2.57 | 2.61 |
| HSTL (I) | 1.5 | 0.17 | 0.79 |
| HSTL (II) | 1.5 | 0.17 | .079 |
| SSTL2 (I) | 2.5 | 1.38 | 3.26 |
| SSTL2 (II) | 2.5 | 1.38 | 3.26 |
| SSTL3 (I) | 3.3 | 3.21 | 7.97 |
| SSTL3 (II) | 3.3 | 3.21 | 7.97 |
| **Differential** | | | |
| LVDS | 2.5 | 2.26 | 0.89 |
| LVPECL | 3.3 | 5.71 | 1.94 |

*Notes:*

1. *PDC6 is the static power (where applicable) measured on VCCI.*
2. *PAC9 is the total dynamic power measured on VCCI.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8b specification.*
4. *Applicable for IGLOOe V2 devices only.*

## Power Consumption of Various Internal Resources

**Table 2-15 • Different Components Contributing to the Dynamic Power Consumption in IGLOOe Devices For IGLOOe V2 or V5 Devices, 1.5 V DC Core Supply Voltage**

| Parameter | Definition | Device-Specific Dynamic Contributions (µW/MHz) | |
|---|---|---|---|
| | | AGLE600 | AGLE3000 |
| PAC1 | Clock contribution of a Global Rib | 19.7 | 12.77 |
| PAC2 | Clock contribution of a Global Spine | 4.16 | 1.85 |
| PAC3 | Clock contribution of a VersaTile row | 0.88 | |
| PAC4 | Clock contribution of a VersaTile used as a sequential module | 0.11 | |
| PAC5 | First contribution of a VersaTile used as a sequential module | 0.057 | |
| PAC6 | Second contribution of a VersaTile used as a sequential module | 0.207 | |
| PAC7 | Contribution of a VersaTile used as a combinatorial module | 0.207 | |
| PAC8 | Average contribution of a routing net | 0.7 | |
| PAC9 | Contribution of an I/O input pin (standard-dependent) | See Table 2-13 on page 2-9. | |
| PAC10 | Contribution of an I/O output pin (standard-dependent) | See Table 2-14 on page 2-10. | |
| PAC11 | Average contribution of a RAM block during a read operation | 25.00 | |
| PAC12 | Average contribution of a RAM block during a write operation | 30.00 | |
| PAC13 | Dynamic contribution for PLL | 2.70 | |

*Note: For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power calculator or SmartPower in Libero SoC software.*

**Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO Devices For IGLOOe V2 or V5 Devices, 1.5 V DC Core Supply Voltage**

| Parameter | Definition | Device Specific Static Power (mW) | |
|---|---|---|---|
| | | AGLE600 | AGLE3000 |
| PDC1 | Array static power in Active mode | See Table 2-12 on page 2-8. | |
| PDC2 | Array static power in Static (Idle) mode | See Table 2-11 on page 2-7. | |
| PDC3 | Array static power in Flash*Freeze mode | See Table 2-9 on page 2-7. | |
| PDC4 | Static PLL contribution | 1.84 | |
| PDC5 | Bank quiescent power (VCCI-dependent) | See Table 2-12 on page 2-8. | |
| PDC6 | I/O input pin static power (standard-dependent) | See Table 2-13 on page 2-9. | |
| PDC7 | I/O output pin static power (standard-dependent) | See Table 2-14 on page 2-10. | |

**Table 2-24 • I/O AC Parameter Definitions**

| Parameter | Definition |
|---|---|
| $t_{DP}$ | Data to Pad delay through the Output Buffer |
| $t_{PY}$ | Pad to Data delay through the Input Buffer with Schmitt trigger disabled |
| $t_{DOUT}$ | Data to Output Buffer delay through the I/O interface |
| $t_{EOUT}$ | Enable to Output Buffer Tristate Control delay through the I/O interface |
| $t_{DIN}$ | Input Buffer to Data delay through the I/O interface |
| $t_{PYS}$ | Pad to Data delay through the Input Buffer with Schmitt trigger enabled |
| $t_{HZ}$ | Enable to Pad delay through the Output Buffer—HIGH to Z |
| $t_{ZH}$ | Enable to Pad delay through the Output Buffer—Z to HIGH |
| $t_{LZ}$ | Enable to Pad delay through the Output Buffer—LOW to Z |
| $t_{ZL}$ | Enable to Pad delay through the Output Buffer—Z to LOW |
| $t_{ZHS}$ | Enable to Pad delay through the Output Buffer with delayed enable—Z to HIGH |
| $t_{ZLS}$ | Enable to Pad delay through the Output Buffer with delayed enable—Z to LOW |

## Detailed I/O DC Characteristics

**Table 2-27 • Input Capacitance**

| Symbol | Definition | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | VIN = 0, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on the clock pin | VIN = 0, f = 1.0 MHz | | 8 | pF |

**Table 2-28 • I/O Output Buffer Maximum Resistances[1]**

| Standard | Drive Strength | $R_{PULL\text{-}DOWN}$ (Ω)[2] | $R_{PULL\text{-}UP}$ (Ω)[3] |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 4 mA | 100 | 300 |
| | 8 mA | 50 | 150 |
| | 12 mA | 25 | 75 |
| | 16 mA | 17 | 50 |
| | 24 mA | 11 | 33 |
| 3.3 V LVCMOS Wide Range | 100 µA | Same as regular 3.3 V LVCMOS | Same as regular 3.3 V LVCMOS |
| 2.5 V LVCMOS | 4 mA | 100 | 200 |
| | 8 mA | 50 | 100 |
| | 12 mA | 25 | 50 |
| | 16 mA | 20 | 40 |
| | 24 mA | 11 | 22 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| | 6 mA | 50 | 56 |
| | 8 mA | 50 | 56 |
| | 12 mA | 20 | 22 |
| | 16 mA | 20 | 22 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |
| | 4 mA | 100 | 112 |
| | 6 mA | 67 | 75 |
| | 8 mA | 33 | 37 |
| | 12 mA | 33 | 37 |
| 1.2 V LVCMOS[4] | 2 mA | 158 | 164 |
| 1.2 V LVCMOS Wide Range[4] | 100 µA | Same as regular 1.2 V LVCMOS | Same as regular 1.2 V LVCMOS |

*Notes:*

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website at http://www.microsemi.com/soc/techdocs/models/ibis.html.*
2. *$R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / IOLspec*
3. *$R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / IOHspec*
4. *Applicable to IGLOOe V2 devices operating in the 1.2 V core range ONLY.*
5. *Output drive strength is below JEDEC specification.*

**Table 2-30 • I/O Short Currents IOSH/IOSL**

| | Drive Strength | IOSH (mA)* | IOSL (mA)* |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 4 mA | 25 | 27 |
| | 8 mA | 51 | 54 |
| | 12 mA | 103 | 109 |
| | 16 mA | 132 | 127 |
| | 24 mA | 268 | 181 |
| 3.3 V LVCMOS Wide Range | 100 µA | Same as regular 3.3 V LVCMOS | Same as regular 3.3 V LVCMOS |
| 2.5 V LVCMOS | 4 mA | 16 | 18 |
| | 8 mA | 32 | 37 |
| | 12 mA | 65 | 74 |
| | 16 mA | 83 | 87 |
| | 24 mA | 169 | 124 |
| 1.8 V LVCMOS | 2 mA | 9 | 11 |
| | 4 mA | 17 | 22 |
| | 6 mA | 35 | 44 |
| | 8 mA | 45 | 51 |
| | 12 mA | 91 | 74 |
| | 16 mA | 91 | 74 |
| 1.5 V LVCMOS | 2 mA | 13 | 16 |
| | 4 mA | 25 | 33 |
| | 6 mA | 32 | 39 |
| | 8 mA | 66 | 55 |
| | 12 mA | 66 | 55 |
| 1.2 V LVCMOS | 2 mA | 20 | 26 |
| 1.2 V LVCMOS Wide Range | 100 µA | 20 | 26 |
| 3.3 V PCI/PCIX | Per PCI/PCI-X Specification | Per PCI Curves | |
| 3.3 V GTL | 25 mA | 268 | 181 |
| 2.5 V GTL | 25 mA | 169 | 124 |
| 3.3 V GTL+ | 35 mA | 268 | 181 |
| 2.5 V GTL+ | 33 mA | 169 | 124 |
| HSTL (I) | 8 mA | 32 | 39 |
| HSTL (II) | 15 mA | 66 | 55 |
| SSTL2 (I) | 15 mA | 83 | 87 |
| SSTL2 (II) | 18 mA | 169 | 124 |
| SSTL3 (I) | 14 mA | 51 | 54 |
| SSTL3 (II) | 21 mA | 103 | 109 |

*Note: $T_J$ = 100°C*

### 2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

**Table 2-46 • Minimum and Maximum DC Input and Output Levels**

| 2.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 4 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 4 | 4 | 16 | 18 | 10 | 10 |
| 8 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 | 32 | 37 | 10 | 10 |
| 12 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 12 | 12 | 65 | 74 | 10 | 10 |
| 16 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 16 | 16 | 83 | 87 | 10 | 10 |
| 24 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 24 | 24 | 169 | 124 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

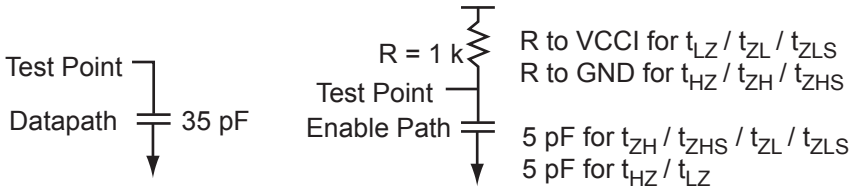


**Figure 2-8 • AC Loading**

**Table 2-47 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|
| 0 | 2.5 | 1.2 | – | 5 |

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

### 1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

**Table 2-58 • Minimum and Maximum DC Input and Output Levels**

| 1.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 13 | 16 | 10 | 10 |
| 4 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 4 | 4 | 25 | 33 | 10 | 10 |
| 6 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 6 | 6 | 32 | 39 | 10 | 10 |
| 8 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 8 | 8 | 66 | 55 | 10 | 10 |
| 12 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 | 66 | 55 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

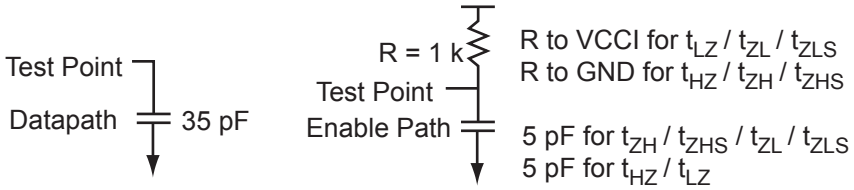


**Figure 2-10 • AC Loading**

**Table 2-59 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|
| 0 | 1.5 | 0.75 | – | 5 |

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

### HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). IGLOOe devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

**Table 2-89 • Minimum and Maximum DC Input and Output Levels**

| HSTL Class I | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 8 mA | –0.3 | VREF – 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI – 0.4 | 8 | 8 | 32 | 39 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

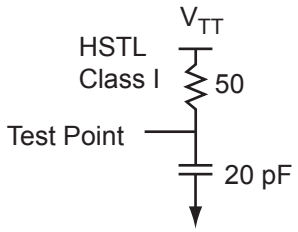


**Figure 2-17 • AC Loading**

**Table 2-90 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|---|
| VREF – 0.1 | VREF + 0.1 | 0.75 | 0.75 | 0.75 | 20 |

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

#### Timing Characteristics

##### 1.5 V DC Core Voltage

**Table 2-91 • HSTL Class I – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V,**
**Worst-Case VCCI = 1.4 V VREF = 0.75 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.98 | 2.74 | 0.19 | 1.77 | 0.67 | 2.79 | 2.73 | | | 6.42 | 6.36 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

##### 1.2 V DC Core Voltage

**Table 2-92 • HSTL Class I – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V,**
**Worst-Case VCCI = 1.4 V VREF = 0.75 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 1.55 | 3.10 | 0.26 | 1.94 | 1.10 | 3.12 | 3.10 | | | 8.93 | 8.91 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

### Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

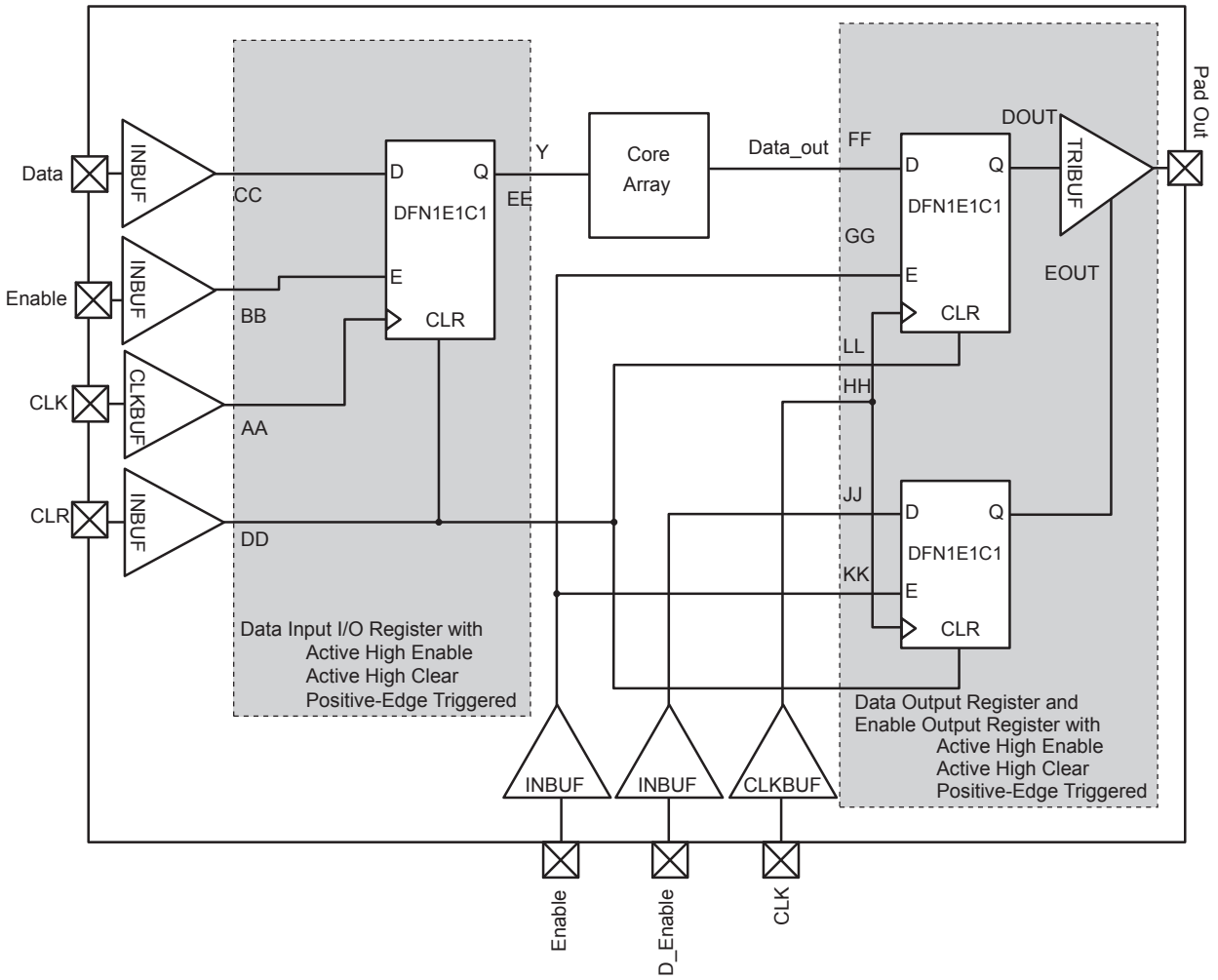


***Figure 2-27 •*** **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

### 1.2 V DC Core Voltage

**Table 2-126 • Output Data Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | 1.52 | ns |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | 1.15 | ns |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | 0.00 | ns |
| $t_{OSUE}$ | Enable Setup Time for the Output Data Register | 1.11 | ns |
| $t_{OHE}$ | Enable Hold Time for the Output Data Register | 0.00 | ns |
| $t_{OCLR2Q}$ | Asynchronous Clear-to-Q of the Output Data Register | 1.96 | ns |
| $t_{OPRE2Q}$ | Asynchronous Preset-to-Q of the Output Data Register | 1.96 | ns |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | 0.24 | ns |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | 0.24 | ns |
| $t_{OWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Data Register | 0.19 | ns |
| $t_{OWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Data Register | 0.19 | ns |
| $t_{OCKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output Data Register | 0.31 | ns |
| $t_{OCKMPWL}$ | Clock Minimum Pulse Width LOW for the Output Data Register | 0.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

### 1.2 V DC Core Voltage

**Table 2-128 • Output Enable Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | 1.10 | ns |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | 1.15 | ns |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | 0.00 | ns |
| $t_{OESUE}$ | Enable Setup Time for the Output Enable Register | 1.22 | ns |
| $t_{OEHE}$ | Enable Hold Time for the Output Enable Register | 0.00 | ns |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | 1.65 | ns |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | 1.65 | ns |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | 0.24 | ns |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | 0.24 | ns |
| $t_{OEWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Enable Register | 0.19 | ns |
| $t_{OEWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.19 | ns |
| $t_{OECKMPWH}$ | Clock Minimum Pulse Width HIGH for the Output Enable Register | 0.31 | ns |
| $t_{OECKMPWL}$ | Clock Minimum Pulse Width LOW for the Output Enable Register | 0.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

## Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-91. Table 2-139 and Table 2-141 present minimum and maximum global clock delays within the device. Minimum and maximum delays are measured with minimum and maximum loading.

### Timing Characteristics

#### 1.5 V DC Core Voltage

**Table 2-139 • AGLE600 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 1.48 | 1.82 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.52 | 1.94 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.18 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.15 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.42 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

**Table 2-140 • AGLE3000 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 2.00 | 2.34 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 2.09 | 2.51 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.18 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.15 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.42 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## Timing Waveforms

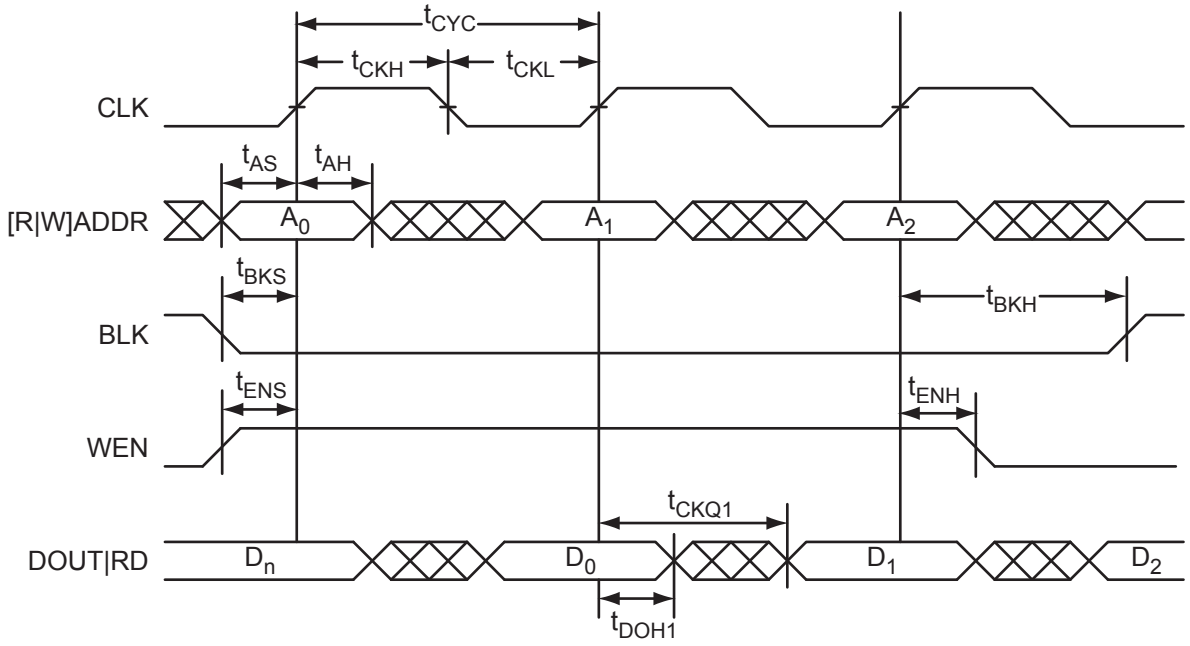


***Figure 2-42 •*** **RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512X18.**

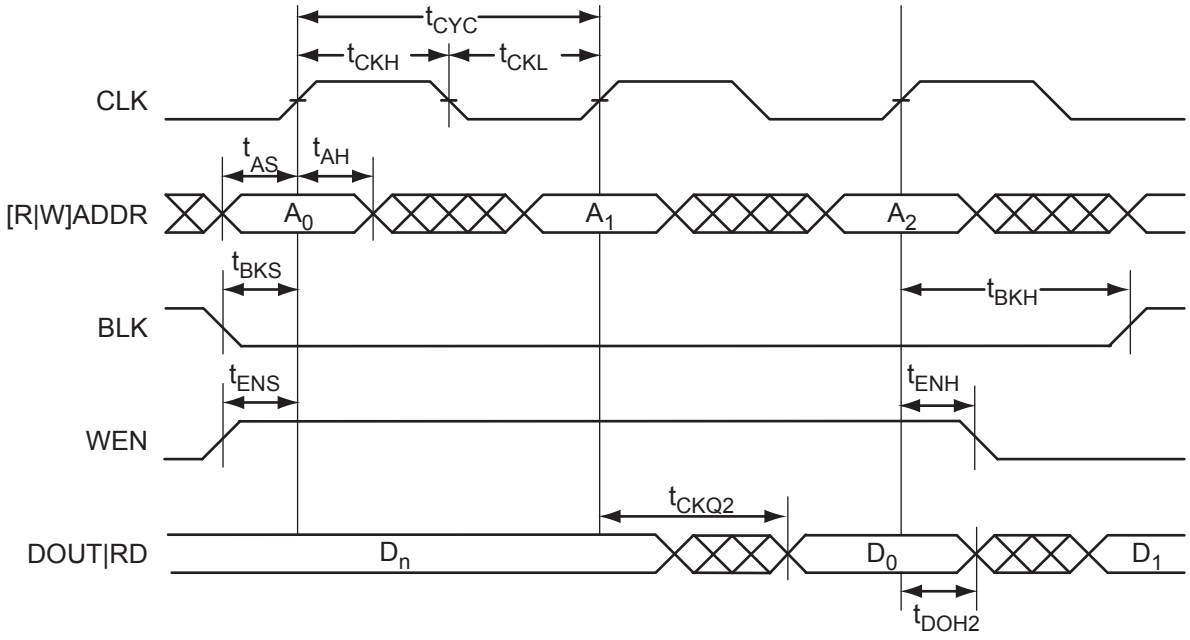


***Figure 2-43 •*** **RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512X18.**

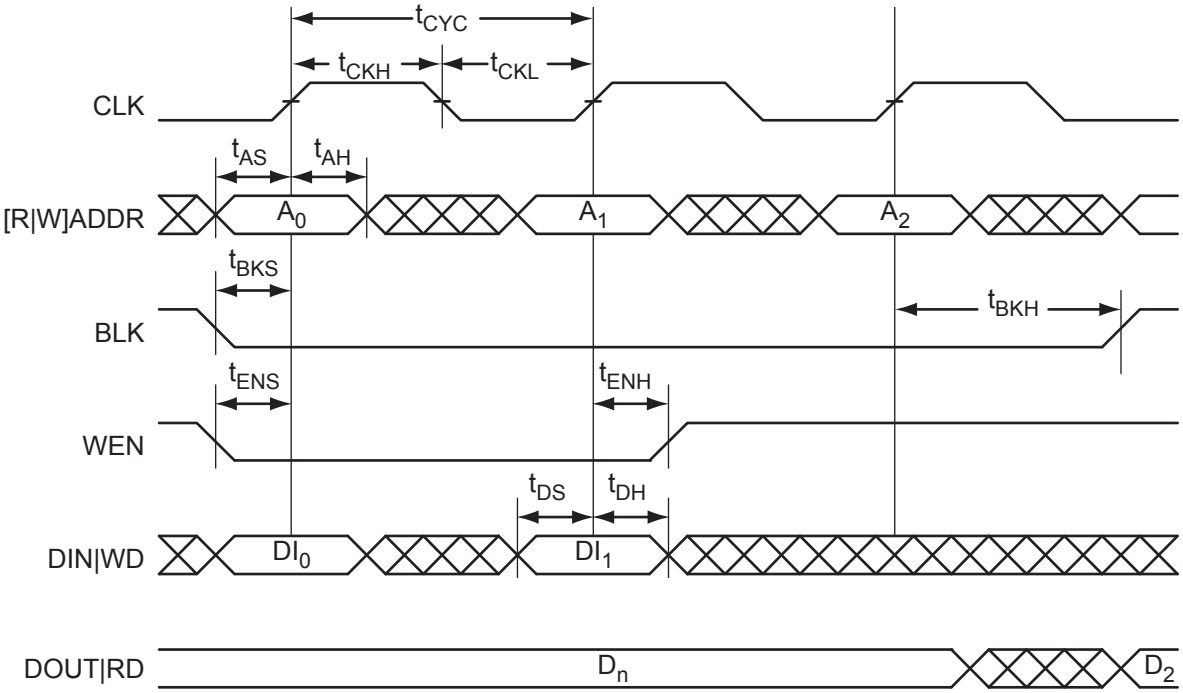


***Figure 2-44 •*** **RAM Write, Output Retained. Applicable to both RAM4K9 and RAM512X18.**

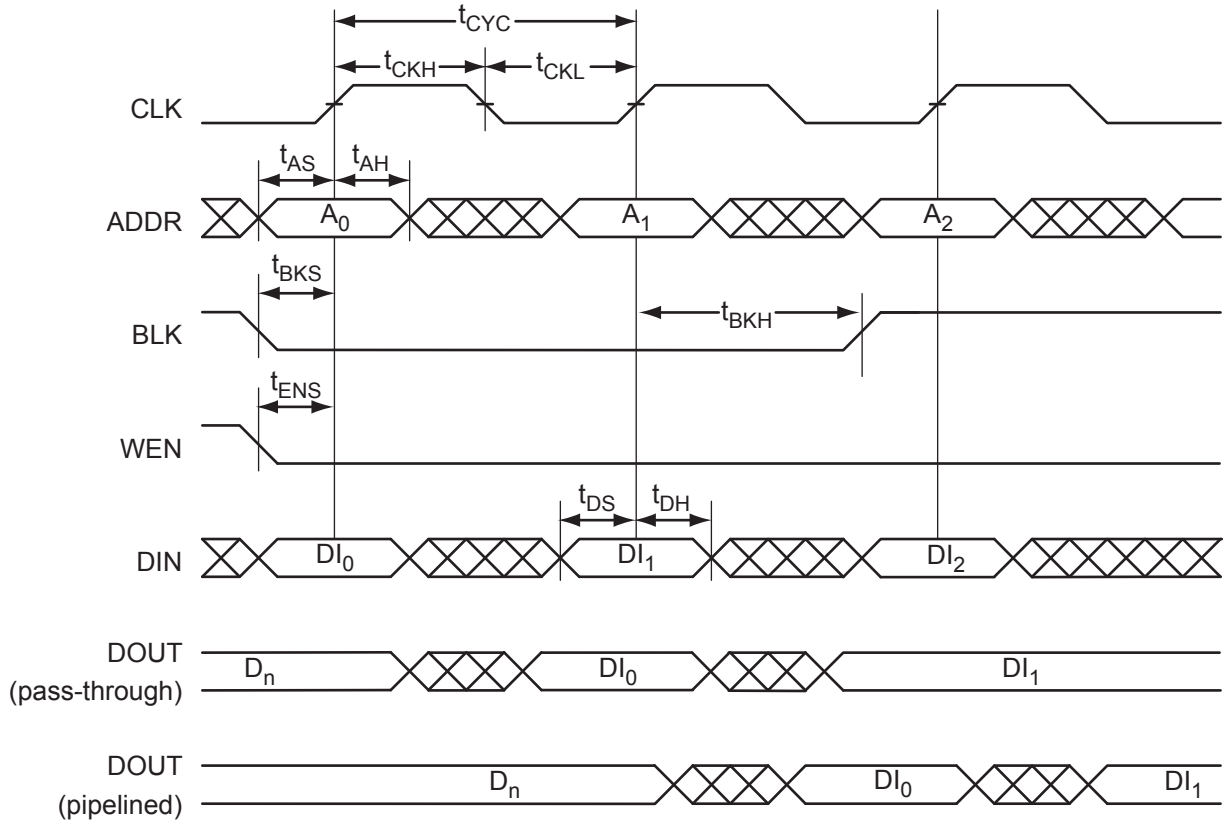


***Figure 2-45 •*** **RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 Only.**

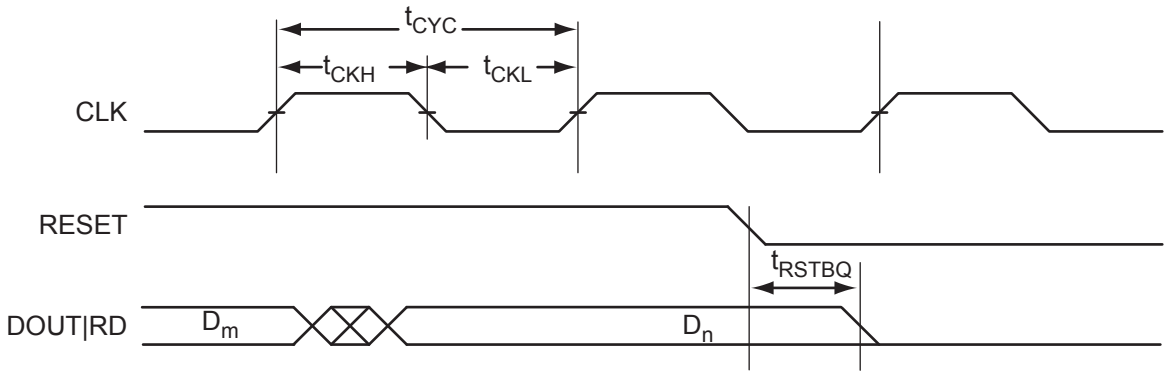


***Figure 2-46 •*** **RAM Reset**

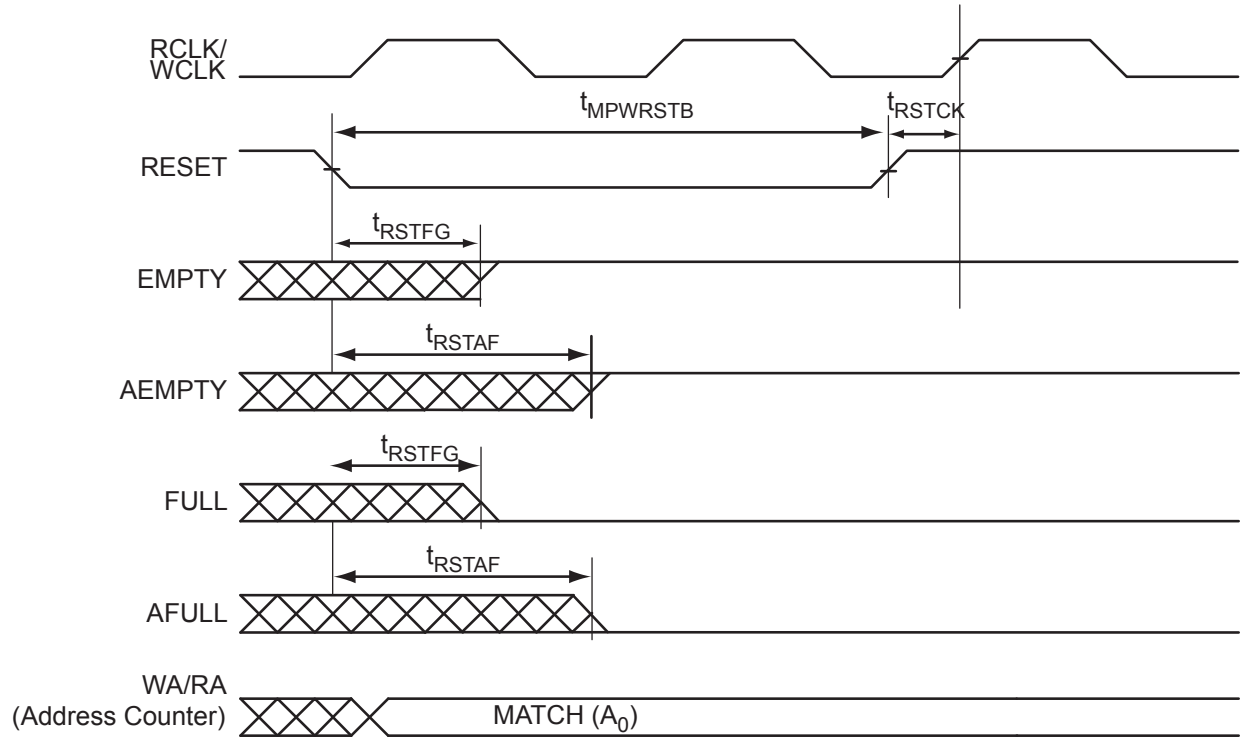


***Figure 2-50 •*** **FIFO Reset**

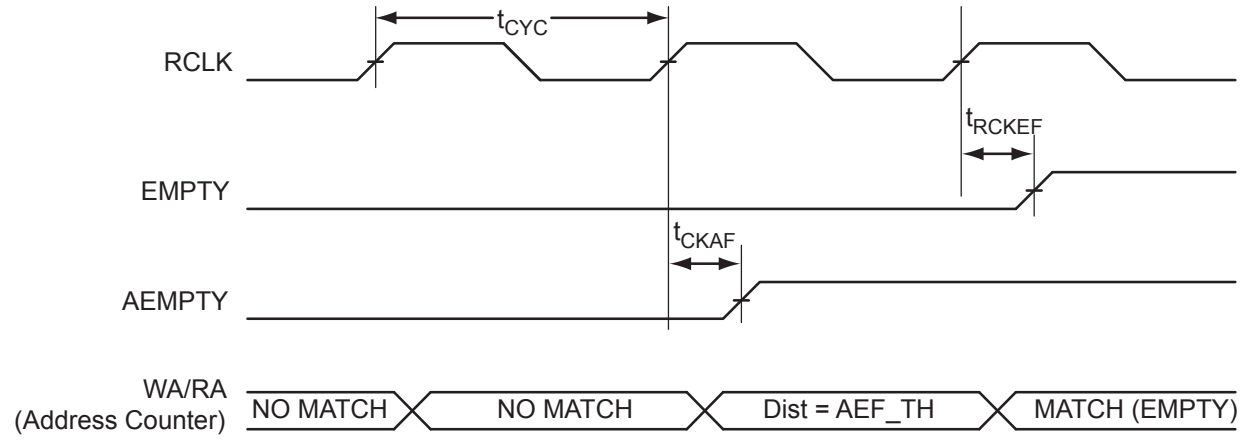


***Figure 2-51 •*** **FIFO EMPTY Flag and AEMPTY Flag Assertion**

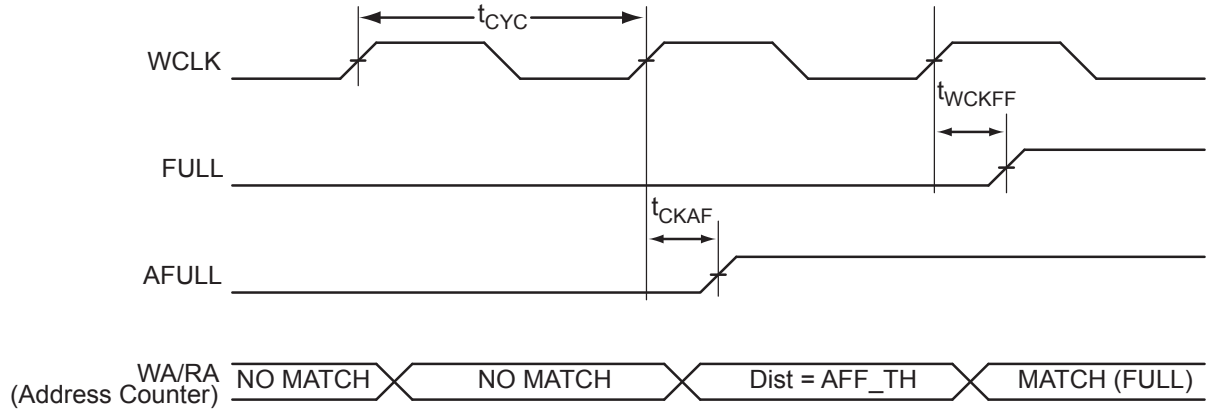


***Figure 2-52 •*** **FIFO FULL Flag and AFULL Flag Assertion**

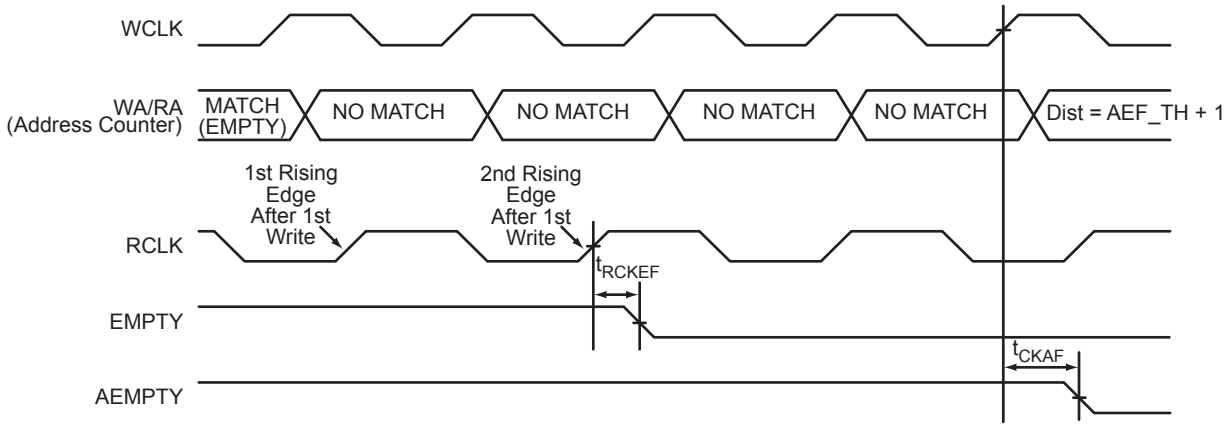


***Figure 2-53 •*** **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

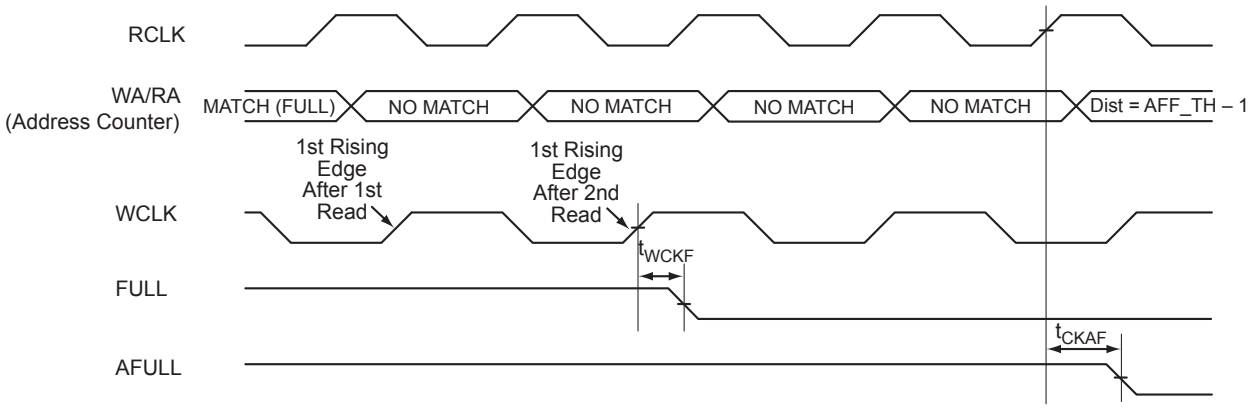


***Figure 2-54 •*** **FIFO FULL Flag and AFULL Flag Deassertion**