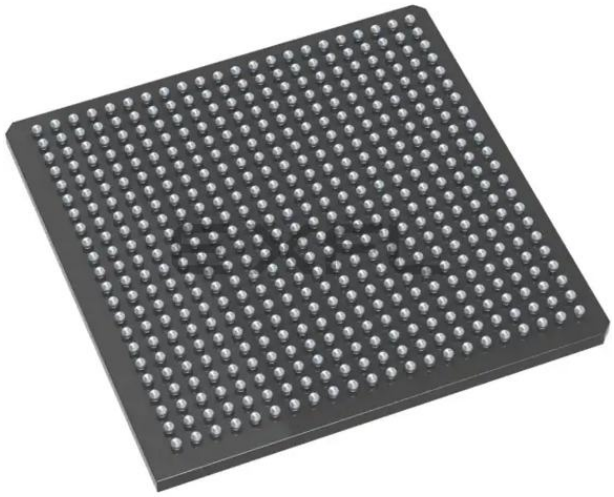

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	75264
Total RAM Bits	516096
Number of I/O	341
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1agle3000v5-fg484

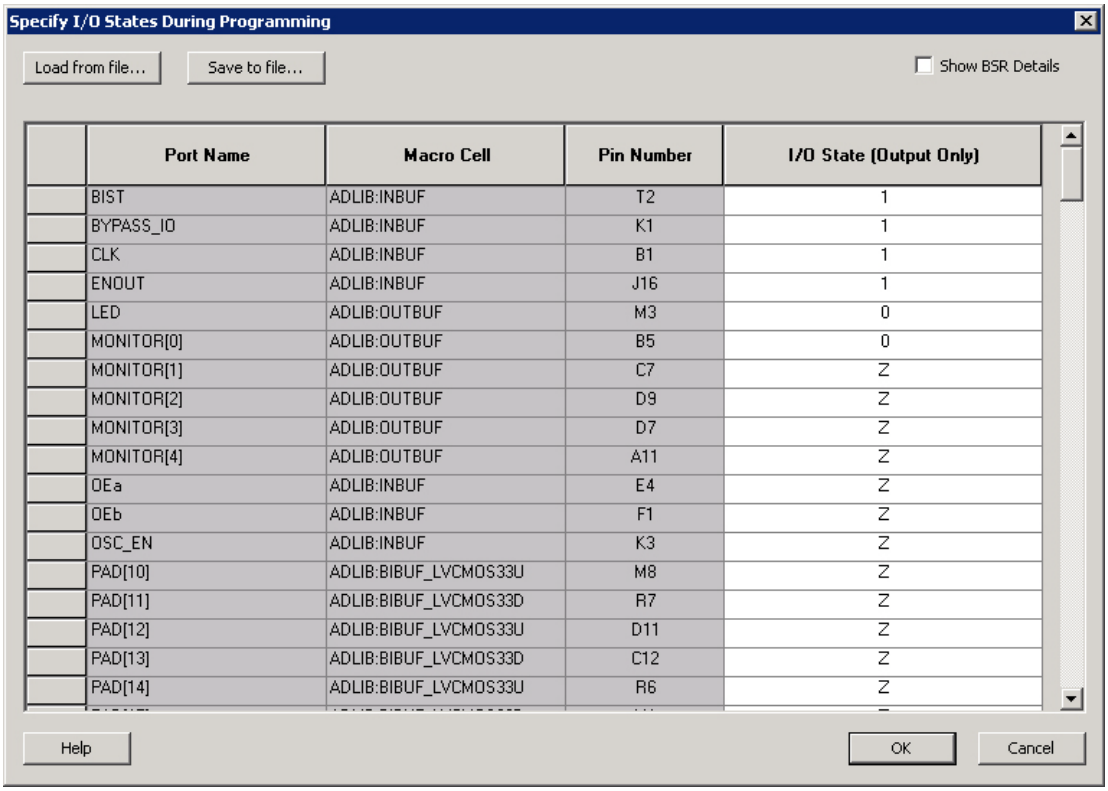

Figure 1-4 • **I/O States During Programming Window**

6. Click OK to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature[1]

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

Table 2-4 • Overshoot and Undershoot Limits [1, 3]

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at junction temperature at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
3. *This table does not provide PCI overshoot/undershoot limits.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOOe device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5.

There are five regions to consider during power-up.

IGLOOe I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.

**Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings
Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI (per standard)**

I/O Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option[1] (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12	12	High	5	–	0.97	2.12	0.18	1.08	1.34	0.66	2.17	1.69	2.71	3.08	5.76	5.28	ns
3.3 V LVCMOS Wide Range[1, 2]	100 µA	12	High	5	–	0.97	2.96	0.18	1.42	1.84	0.66	2.98	2.28	3.86	4.36	6.58	5.87	ns
2.5 V LVCMOS	12	12	High	5	–	.097	2.15	0.18	1.31	1.41	0.66	2.20	1.85	2.78	2.98	5.80	5.45	ns
1.8 V LVCMOS	12	12	High	5	–	0.97	2.37	0.18	1.27	1.59	0.66	2.42	2.03	3.07	3.57	6.02	5.62	ns
1.5 V LVCMOS	12	12	High	5	–	0.97	2.69	0.18	1.47	1.77	0.66	2.75	2.30	3.24	3.67	6.35	5.89	ns
3.3 V PCI	Per PCI spec	–	High	10	25 [3]	0.97	2.38	0.18	0.96	1.42	0.66	2.43	1.80	2.72	3.08	6.03	5.39	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 [3]	0.97	2.38	0.19	0.92	1.34	0.66	2.43	1.80	2.72	3.08	6.03	5.39	ns
3.3 V GTL	20[4]	–	High	10	25	0.97	1.78	0.19	2.35	–	0.66	1.80	1.78	–	–	5.39	5.38	ns
2.5 V GTL	20[4]	–	High	10	25	0.97	1.85	0.19	1.98	–	0.66	1.89	1.82	–	–	5.49	5.42	ns
3.3 V GTL+	35	–	High	10	25	0.97	1.80	0.19	1.32	–	0.66	1.84	1.77	–	–	5.44	5.36	ns
2.5 V GTL+	33	–	High	10	25	0.97	1.92	0.19	1.26	–	0.66	1.96	1.80	–	–	5.56	5.40	ns
HSTL (I)	8	–	High	20	50	0.97	2.67	0.18	1.72	–	0.66	2.72	2.67	–	–	6.32	6.26	ns
HSTL (II)	15	–	High	20	25	0.97	2.55	0.18	1.72	–	0.66	2.60	2.34	–	–	6.20	5.93	ns
SSTL2 (I)	15	–	High	30	50	0.97	1.86	0.19	1.12	–	0.66	1.90	1.68	–	–	5.50	5.28	ns
SSTL2 (II)	18	–	High	30	25	0.97	1.89	0.19	1.12	–	0.66	1.93	1.62	–	–	5.53	5.22	ns
SSTL3 (I)	14	–	High	30	50	0.97	2.00	0.19	1.06	–	0.66	2.04	1.67	–	–	5.64	5.27	ns
SSTL3 (II)	21	–	High	30	25	0.97	1.81	0.19	1.06	–	0.66	1.85	1.55	–	–	5.45	5.14	ns
LVDS	24	–	High	–	–	0.97	1.73	0.19	1.62	–	–	–	–	–	–	–	–	ns
LVPECL	24	–	High	–	–	0.97	1.65	0.18	1.42	–	–	–	–	–	–	–	–	ns

Notes:

1. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
3. *Resistance is used to measure I/O propagation delays as defined in PCI Specifications. See Figure 2-12 on page 2-49 for connectivity. This resistor is not required during normal operation.*
4. *Output drive strength is below JEDEC specification.*
5. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings (continued)
Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI (per standard)

I/O Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option[1] (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
LVDS	24	–	High	–	–	1.55	2.26	0.25	1.95	–	–	–	–	–	–	–	–	ns
LVPECL	24	–	High	–	–	1.55	2.17	0.25	1.70	–	–	–	–	–	–	–	–	ns

Notes:

1. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
3. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*
4. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-49 for connectivity. This resistor is not required during normal operation.*
5. *Output drive strength is below JEDEC specification.*
6. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-36 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.97	4.90	0.18	1.08	1.34	0.66	5.00	3.99	2.27	2.16	8.60	7.59	ns
8 mA	Std.	0.97	4.05	0.18	1.08	1.34	0.66	4.13	3.45	2.53	2.65	7.73	7.05	ns
12 mA	Std.	0.97	3.44	0.18	1.08	1.34	0.66	3.51	3.05	2.71	2.95	7.11	6.64	ns
16 mA	Std.	0.97	3.27	0.18	1.08	1.34	0.66	3.34	2.96	2.74	3.04	6.93	6.55	ns
24 mA	Std.	0.97	3.18	0.18	1.08	1.34	0.66	3.24	2.97	2.79	3.36	6.84	6.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-37 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.97	2.85	0.18	1.08	1.34	0.66	2.92	2.27	2.27	2.27	6.51	5.87	ns
8 mA	Std.	0.97	2.39	0.18	1.08	1.34	0.66	2.44	1.88	2.53	2.76	6.03	5.47	ns
12 mA	Std.	0.97	2.12	0.18	1.08	1.34	0.66	2.17	1.69	2.71	3.08	5.76	5.28	ns
16 mA	Std.	0.97	2.08	0.18	1.08	1.34	0.66	2.12	1.65	2.75	3.17	5.72	5.25	ns
24 mA	Std.	0.97	2.10	0.18	1.08	1.34	0.66	2.14	1.60	2.80	3.49	5.74	5.20	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-42 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	4 mA	Std.	0.97	7.26	0.18	1.42	1.84	0.66	7.28	5.78	3.18	2.93	10.88	9.38	ns
100 µA	8 mA	Std.	0.97	5.94	0.18	1.42	1.84	0.66	5.96	4.96	3.59	3.69	9.56	8.56	ns
100 µA	12 mA	Std.	0.97	5.00	0.18	1.42	1.84	0.66	5.02	4.34	3.86	4.16	8.62	7.94	ns
100 µA	16 mA	Std.	0.97	4.73	0.18	1.42	1.84	0.66	4.75	4.21	3.92	4.29	8.35	7.81	ns
100 µA	24 mA	Std.	0.97	4.59	0.18	1.42	1.84	0.66	4.61	4.23	3.99	4.78	8.21	7.82	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-43 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	4 mA	Std.	0.97	4.10	0.18	1.42	1.84	0.66	4.12	3.17	3.18	3.11	7.71	6.77	ns
100 µA	8 mA	Std.	0.97	3.37	0.18	1.42	1.84	0.66	3.39	2.57	3.59	3.87	6.99	6.16	ns
100 µA	12 mA	Std.	0.97	2.96	0.18	1.42	1.84	0.66	2.98	2.28	3.86	4.36	6.58	5.87	ns
100 µA	16 mA	Std.	0.97	2.90	0.18	1.42	1.84	0.66	2.92	2.22	3.93	4.49	6.51	5.82	ns
100 µA	24 mA	Std.	0.97	2.92	0.18	1.42	1.84	0.66	2.94	2.15	4.00	4.99	6.54	5.75	ns

Notes:

1. *The minimum drive strength for any or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
3. *Software default selection highlighted in gray.*

1.8 V LVCMOS

Low-Voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-52 • Minimum and Maximum DC Input and Output Levels

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	17	22	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	6	6	35	44	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	8	8	45	51	10	10
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12	91	74	10	10
16 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	16	16	91	74	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

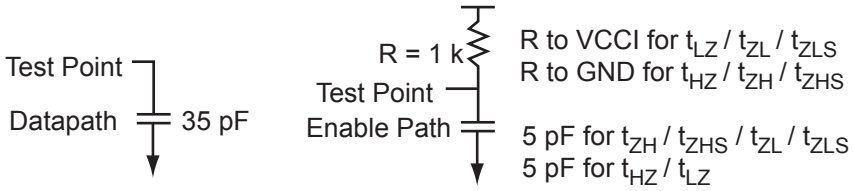

Figure 2-9 • AC Loading

Table 2-53 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	1.8	0.9	–	5

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

Timing Characteristics

1.2 V DC Core Voltage

Table 2-66 • 1.2 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	9.92	0.26	2.09	2.95	1.10	9.53	7.48	4.02	3.67	15.31	13.26	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Table 2-67 • 1.2 LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	4.06	0.26	2.09	2.95	1.10	3.92	3.46	4.01	3.79	9.71	9.24	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

1.2 V LVCMOS Wide Range

Table 2-68 • Minimum and Maximum DC Input and Output Levels

1.2 V LVCMOS Wide Range[1]		VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[2]	IIH[3]
Drive Strength	Equivalent Software Default Drive Strength Option[4]	Min. (V)	Max. (V)	Min. (V)	Max (V)	Max. (V)	Min. (V)	µA	µA	Max. (mA)[5]	Max. (mA)[5]	µA[6]	µA[6]
100 µA	2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	100	100	20	26	10	10

Notes:

1. *Applicable to V2 devices ONLY.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI . Input current is larger when operating outside recommended ranges.*
4. *The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
5. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
6. *Currents are measured at 85°C junction temperature.*
7. *Software default selection highlighted in gray.*

Timing Characteristics

Refer to LVCMOS 1.2 V (normal range) "Timing Characteristics" on page 2-48 for worst-case timing.

SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). IGLOOe devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-101 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
18 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18	169	124	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operating conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

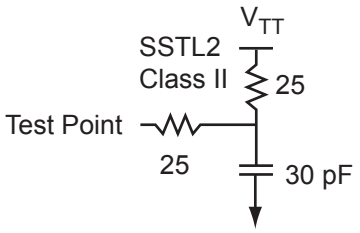

Figure 2-20 • AC Loading

Table 2-102 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input HIGH (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-103 • SSTL 2 Class II – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 2.3 V VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	1.94	0.19	1.15	0.67	1.97	1.66			5.60	5.29	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-104 • SSTL 2 Class II – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V,
Worst-Case VCCI = 2.3 V VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.20	0.26	1.39	1.10	2.24	1.97			8.05	7.78	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

***Table 2-121* • Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: See Figure 2-26 on page 2-66 for more information.

Input Register

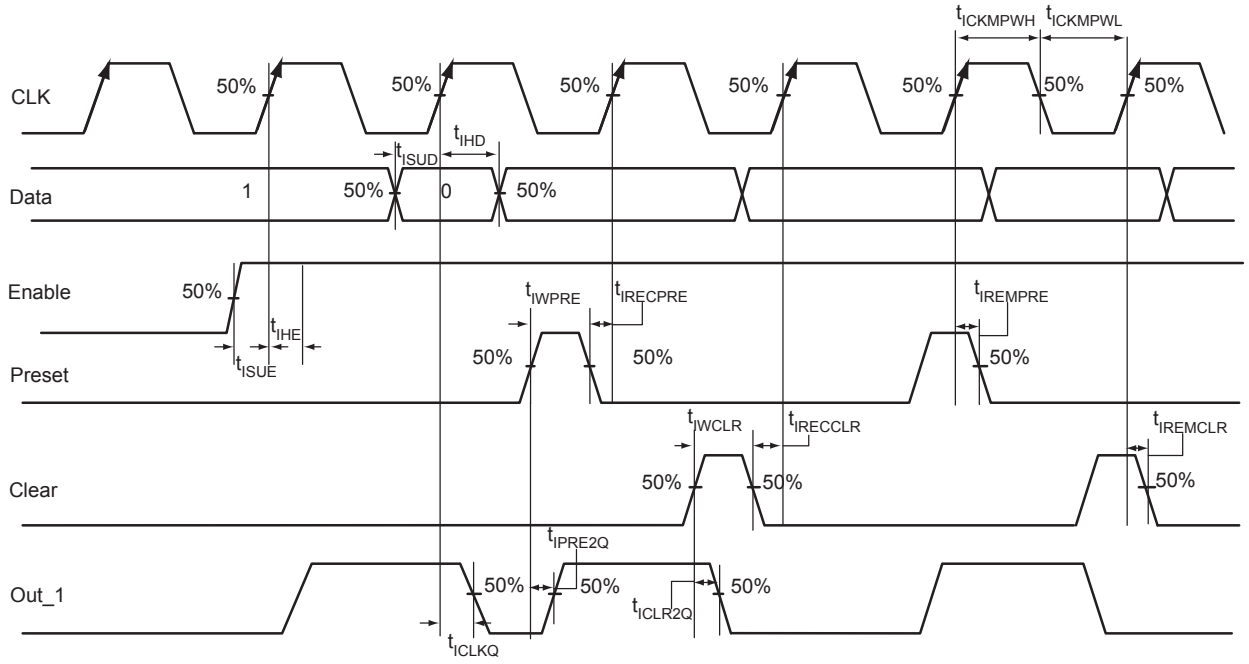

Figure 2-28 • **Input Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-123 • **Input Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.42	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.47	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.67	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.79	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.79	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The IGLOOe library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

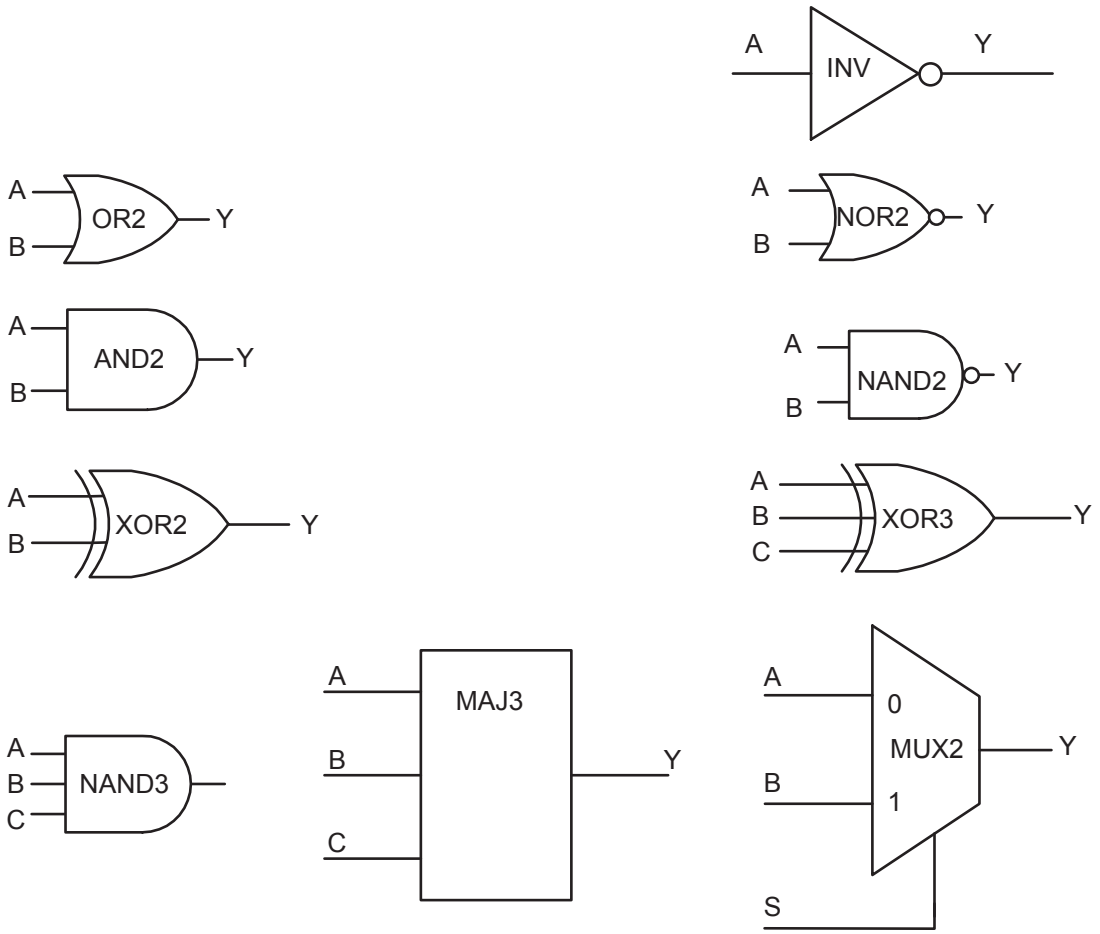

Figure 2-35 • **Sample of Combinatorial Cells**

Applies to 1.2 V DC Core Voltage

Table 2-147 • RAM4K9
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{AS}	Address Setup Time	1.53	ns
t_{AH}	Address Hold Time	0.29	ns
t_{ENS}	REN, WEN Setup Time	1.50	ns
t_{ENH}	REN, WEN Hold Time	0.29	ns
t_{BKS}	BLK Setup Time	3.05	ns
t_{BKH}	BLK Hold Time	0.29	ns
t_{DS}	Input Data (DIN) Setup Time	1.33	ns
t_{DH}	Input Data (DIN) Hold Time	0.66	ns
t_{CKQ1}	Clock High to New Data Valid on DOUT (output retained, WMODE = 0)	6.61	ns
	Clock High to New Data Valid on DOUT (flow-through, WMODE = 1)	5.72	ns
t_{CKQ2}	Clock High to New Data Valid on DOUT (pipelined)	3.38	ns
t_{C2CWWL}[1]	Address collision clk-to-clk delay for reliable write after write on same address; applicable to closing edge	0.30	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.89	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	1.01	ns
t_{RSTBQ}	RESET Low to Data Out Low on DOUT (pass-through)	3.86	ns
	RESET Low to Data Out Low on DOUT (pipelined)	3.86	ns
$t_{REMRSTB}$	RESET Removal	1.12	ns
$t_{RECRSTB}$	RESET Recovery	5.93	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	1.18	ns
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency	92	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 3-3* • TRST and TCK Pull-Down Recommendations**

VJTAG	Tie-Off Resistance*
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Note: Equivalent parallel resistance if more than one device is on the JTAG chain

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-2 and must satisfy the parallel resistance value requirement. The values in Table 3-2 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements.

Special Function Pins

NC No Connect

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC Do Not Connect

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Packaging

Semiconductor technology is constantly shrinking in size while growing in capability and functional integration. To enable next-generation silicon technologies, semiconductor packages have also evolved to provide improved performance and flexibility.

Microsemi consistently delivers packages that provide the necessary mechanical and environmental protection to ensure consistent reliability and performance. Microsemi IC packaging technology efficiently supports high-density FPGAs with large-pin-count Ball Grid Arrays (BGAs), but is also flexible enough to accommodate stringent form factor requirements for Chip Scale Packaging (CSP). In addition, Microsemi offers a variety of packages designed to meet your most demanding application and economic requirements for today's embedded and mobile systems.

FG484	
Pin Number	AGLE600 Function
N8	VCCIB6
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB3
N16	IO54NPB3V0
N17	IO57NPB3V0
N18	IO55NPB3V0
N19	IO57PPB3V0
N20	NC
N21	IO56NDB3V0
N22	IO58PDB3V0
P1	NC
P2	IO111PDB6V1
P3	IO115NPB6V1
P4	IO113NPB6V1
P5	IO109PPB6V0
P6	IO108PDB6V0
P7	IO108NDB6V0
P8	VCCIB6
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB3
P16	GDB0/IO66NPB3V1
P17	IO60NDB3V1
P18	IO60PDB3V1
P19	IO61PDB3V1
P20	NC

FG484	
Pin Number	AGLE600 Function
P21	IO59PDB3V0
P22	IO58NDB3V0
R1	NC
R2	IO110PDB6V0
R3	VCC
R4	IO109NPB6V0
R5	IO106NDB6V0
R6	IO106PDB6V0
R7	GEC0/IO104NPB6V0
R8	VMV5
R9	VCCIB5
R10	VCCIB5
R11	IO84NDB5V0
R12	IO84PDB5V0
R13	VCCIB4
R14	VCCIB4
R15	VMV3
R16	VCCPLD
R17	GDB1/IO66PPB3V1
R18	GDC1/IO65PDB3V1
R19	IO61NDB3V1
R20	VCC
R21	IO59NDB3V0
R22	IO62PDB3V1
T1	NC
T2	IO110NDB6V0
T3	NC
T4	IO105PDB6V0
T5	IO105NDB6V0
T6	GEC1/IO104PPB6V0
T7	VCOMPLE
T8	GNDQ
T9	GEA2/IO101PPB5V2
T10	IO92NDB5V1
T11	IO90NDB5V1

FG484	
Pin Number	AGLE600 Function
T12	IO82NDB5V0
T13	IO74NDB4V1
T14	IO74PDB4V1
T15	GNDQ
T16	VCOMPLD
T17	VJTAG
T18	GDC0/IO65NDB3V1
T19	GDA1/IO67PDB3V1
T20	NC
T21	IO64PDB3V1
T22	IO62NDB3V1
U1	NC
U2	IO107PDB6V0
U3	IO107NDB6V0
U4	GEB1/IO103PDB6V0
U5	GEB0/IO103NDB6V0
U6	VMV6
U7	VCCPLE
U8	IO101NPB5V2
U9	IO95PPB5V1
U10	IO92PDB5V1
U11	IO90PDB5V1
U12	IO82PDB5V0
U13	IO76NDB4V1
U14	IO76PDB4V1
U15	VMV4
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO67NDB3V1
U20	NC
U21	IO64NDB3V1
U22	IO63PDB3V1
V1	NC
V2	NC

FG484	
Pin Number	**AGLE600 Function**
V3	GND
V4	GEA1/IO102PDB6V0
V5	GEA0/IO102NDB6V0
V6	GNDQ
V7	GEC2/IO99PDB5V2
V8	IO95NPB5V1
V9	IO91NDB5V1
V10	IO91PDB5V1
V11	IO83NDB5V0
V12	IO83PDB5V0
V13	IO77NDB4V1
V14	IO77PDB4V1
V15	IO69NDB4V0
V16	GDB2/IO69PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO63NDB3V1
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO100NDB5V2
W6	FF/GEB2/IO100PDB5V2
W7	IO99NDB5V2
W8	IO88NDB5V0
W9	IO88PDB5V0
W10	IO89NDB5V0
W11	IO80NDB4V1
W12	IO81NDB4V1
W13	IO81PDB4V1
W14	IO70NDB4V0
W15	GDC2/IO70PDB4V0

FG484	
Pin Number	**AGLE600 Function**
W16	IO68NDB4V0
W17	GDA2/IO68PDB4V0
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB6
Y2	NC
Y3	NC
Y4	IO98NDB5V2
Y5	GND
Y6	IO94NDB5V1
Y7	IO94PDB5V1
Y8	VCC
Y9	VCC
Y10	IO89PDB5V0
Y11	IO80PDB4V1
Y12	IO78NPB4V1
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB3

FG484	
Pin Number	AGLE3000 Function
C18	GND
C19	IO76PPB1V4
C20	IO88NDB2V0
C21	IO94PPB2V1
C22	VCCIB2
D1	IO293PDB7V2
D2	IO303NDB7V3
D3	IO305NDB7V3
D4	GND
D5	GAA0/IO00NDB0V0
D6	GAA1/IO00PDB0V0
D7	GAB0/IO01NDB0V0
D8	IO20PDB0V2
D9	IO22PDB0V2
D10	IO30PDB0V3
D11	IO38NDB0V4
D12	IO52NDB1V1
D13	IO52PDB1V1
D14	IO66NDB1V3
D15	IO66PDB1V3
D16	GBB1/IO80PDB1V4
D17	GBA0/IO81NDB1V4
D18	GBA1/IO81PDB1V4
D19	GND
D20	IO88PDB2V0
D21	IO90PDB2V1
D22	IO94NPB2V1
E1	IO293NDB7V2
E2	IO299PPB7V3
E3	GND
E4	GAB2/IO308PDB7V4
E5	GAA2/IO309PDB7V4
E6	GNDQ
E7	GAB1/IO01PDB0V0
E8	IO20NDB0V2

FG484	
Pin Number	AGLE3000 Function
E9	IO22NDB0V2
E10	IO30NDB0V3
E11	IO38PDB0V4
E12	IO44NDB1V0
E13	IO58NDB1V2
E14	IO58PDB1V2
E15	GBC1/IO79PDB1V4
E16	GBB0/IO80NDB1V4
E17	GNDQ
E18	GBA2/IO82PDB2V0
E19	IO86NDB2V0
E20	GND
E21	IO90NDB2V1
E22	IO98PDB2V2
F1	IO299NPB7V3
F2	IO301NDB7V3
F3	IO301PDB7V3
F4	IO308NDB7V4
F5	IO309NDB7V4
F6	VMV7
F7	VCCPLA
F8	GAC0/IO02NDB0V0
F9	GAC1/IO02PDB0V0
F10	IO32NDB0V3
F11	IO32PDB0V3
F12	IO44PDB1V0
F13	IO50NDB1V1
F14	IO60PDB1V2
F15	GBC0/IO79NDB1V4
F16	VCCPLB
F17	VMV2
F18	IO82NDB2V0
F19	IO86PDB2V0
F20	IO96PDB2V1
F21	IO96NDB2V1

FG484	
Pin Number	AGLE3000 Function
F22	IO98NDB2V2
G1	IO289NDB7V1
G2	IO289PDB7V1
G3	IO291PPB7V2
G4	IO295PDB7V2
G5	IO297PDB7V2
G6	GAC2/IO307PDB7V4
G7	VCOMPLA
G8	GNDQ
G9	IO26NDB0V3
G10	IO26PDB0V3
G11	IO36PDB0V4
G12	IO42PDB1V0
G13	IO50PDB1V1
G14	IO60NDB1V2
G15	GNDQ
G16	VCOMPLB
G17	GBB2/IO83PDB2V0
G18	IO92PDB2V1
G19	IO92NDB2V1
G20	IO102PDB2V2
G21	IO102NDB2V2
G22	IO105NDB2V2
H1	IO286PSB7V1
H2	IO291NPB7V2
H3	VCC
H4	IO295NDB7V2
H5	IO297NDB7V2
H6	IO307NDB7V4
H7	IO287PDB7V1
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO36NDB0V4
H12	IO42NDB1V0

FG896	
Pin Number	AGLE3000 Function
H11	IO18PDB0V2
H12	IO26NPB0V3
H13	IO28NDB0V3
H14	IO28PDB0V3
H15	IO38PPB0V4
H16	IO42NDB1V0
H17	IO52NDB1V1
H18	IO52PDB1V1
H19	IO62NDB1V2
H20	IO62PDB1V2
H21	IO70NDB1V3
H22	IO70PDB1V3
H23	GND
H24	VCOMPLB
H25	GBC2/IO84PDB2V0
H26	IO84NDB2V0
H27	IO96PDB2V1
H28	IO96NDB2V1
H29	IO89PDB2V0
H30	IO89NDB2V0
J1	IO290NDB7V2
J2	IO290PDB7V2
J3	IO302NDB7V3
J4	IO302PDB7V3
J5	IO295NDB7V2
J6	IO299NDB7V3
J7	VCCIB7
J8	VCCPLA
J9	VCC
J10	IO04NPB0V0
J11	IO18NDB0V2
J12	IO20NDB0V2
J13	IO20PDB0V2
J14	IO32NDB0V3
J15	IO32PDB0V3

FG896	
Pin Number	AGLE3000 Function
J16	IO42PDB1V0
J17	IO44NDB1V0
J18	IO44PDB1V0
J19	IO54NDB1V1
J20	IO54PDB1V1
J21	IO76NPB1V4
J22	VCC
J23	VCCPLB
J24	VCCIB2
J25	IO90PDB2V1
J26	IO90NDB2V1
J27	GBB2/IO83PDB2V0
J28	IO83NDB2V0
J29	IO91PDB2V1
J30	IO91NDB2V1
K1	IO288NDB7V1
K2	IO288PDB7V1
K3	IO304NDB7V3
K4	IO304PDB7V3
K5	GAB2/IO308PDB7V4
K6	IO308NDB7V4
K7	IO301PDB7V3
K8	IO301NDB7V3
K9	GAC2/IO307PPB7V4
K10	VCC
K11	IO04PPB0V0
K12	VCCIB0
K13	VCCIB0
K14	VCCIB0
K15	VCCIB0
K16	VCCIB1
K17	VCCIB1
K18	VCCIB1
K19	VCCIB1
K20	IO76PPB1V4

FG896	
Pin Number	AGLE3000 Function
K21	VCC
K22	IO78PPB1V4
K23	IO88NDB2V0
K24	IO88PDB2V0
K25	IO94PDB2V1
K26	IO94NDB2V1
K27	IO85PDB2V0
K28	IO85NDB2V0
K29	IO93PDB2V1
K30	IO93NDB2V1
L1	IO286NDB7V1
L2	IO286PDB7V1
L3	IO298NDB7V3
L4	IO298PDB7V3
L5	IO283PDB7V1
L6	IO291NDB7V2
L7	IO291PDB7V2
L8	IO293PDB7V2
L9	IO293NDB7V2
L10	IO307NPB7V4
L11	VCC
L12	VCC
L13	VCC
L14	VCC
L15	VCC
L16	VCC
L17	VCC
L18	VCC
L19	VCC
L20	VCC
L21	IO78NPB1V4
L22	IO104NPB2V2
L23	IO98NDB2V2
L24	IO98PDB2V2
L25	IO87PDB2V0

Revision	Changes	Page
Revision 3 (cont'd)	Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings1 was updated to change PDC3 to PDC7. The table notes were updated to reflect that power was measured on VCCI. Table note 4 is new.	2-10
	Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO Devices and Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO Devices were updated to add PDC6 and PDC7, and to change the definition for PDC5 to bank quiescent power.	2-11, 2-12
	A table subtitle was added for Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO Devices.	2-12
	The "Total Static Power Consumption—PSTAT" section was updated to revise the calculation of P_{STAT}, including PDC6 and PDC7.	2-13
	Footnote 1 was updated to include information about P_{AC13}. The PLL Contribution equation was changed from: $P_{PLL} = P_{AC13} + P_{AC14} * FCLKOUT$ to $PPLL = P_{DC4} + P_{AC13} * F_{CLKOUT}$.	2-14
	The "Timing Model" was updated to be consistent with the revised timing numbers.	2-16
	In Table 2-22 • Summary of Maximum and Minimum DC Input Levels, T_J was changed to T_A in notes 1 and 2.	2-22
	Table 2-22 • Summary of Maximum and Minimum DC Input Levels was updated to included a hysteresis value for 1.2 V LVCMOS (Schmitt trigger mode).	2-22
	All AC Loading figures for single-ended I/O standards were changed from Datapaths at 35 pF to 5 pF.	N/A
	The "1.2 V LVCMOS (JESD8-12A)" section is new.	2-47
Revision 2 (Jun 2008) Product Brief v1.0	The product brief section of the datasheet was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.	N/A
Revision 2 (cont'd) Packaging v1.1	The naming conventions changed for the following pins in the "FG484" for the A3GLE600: Pin Number — New Function Name J19 — IO45PPB2V1 K20 — IO45NPB2V1 M2 — IO114NPB6V1 N1 — IO114PPB6V1 N4 — GFC2/IO115PPB6V1 P3 — IO115NPB6V1	4-6
Revision 1 (Mar 2008) Product Brief rev. 1	The "Low Power" section was updated to change "1.2 V and 1.5 V Core Voltage" to "1.2 V and 1.5 V Core and I/O Voltage." The text "(from 25 µW)" was removed from "Low Power Active FPGA Operation." 1.2_V was added to the list of core and I/O voltages in the "Pro (Professional) I/O" and "Pro I/Os with Advanced I/O Standards" section sections.	I I, 1-7
Revision 0 (Jan 2008)	This document was previously in datasheet Advance v0.4. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is 51700096-001-0.	N/A