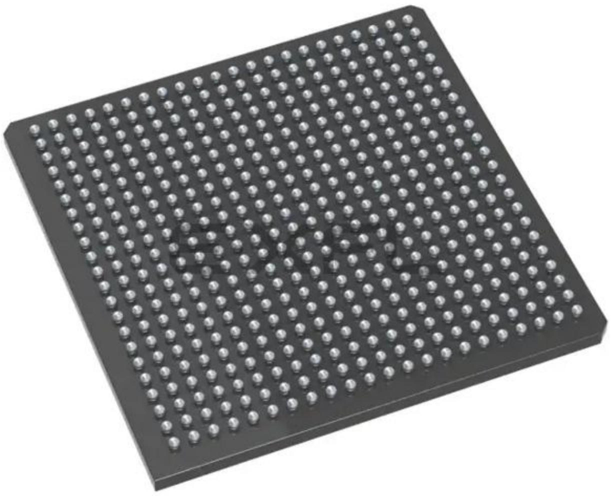

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	75264
Total RAM Bits	516096
Number of I/O	341
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1agle3000v5-fg484i

1 – IGLOOe Device Family Overview

General Description

The IGLOOe family of flash FPGAs, based on a 130-nm flash process, offers the lowest power FPGA, a single-chip solution, small footprint packages, reprogrammability, and an abundance of advanced features.

The Flash*Freeze technology used in IGLOOe devices enables entering and exiting an ultra-low power mode while retaining SRAM and register data. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low power consumption while the IGLOOe device is completely functional in the system. This allows the IGLOOe device to control system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOOe devices the advantage of being a secure, low power, single-chip solution that is Instant On. IGLOOe is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOOe devices offer 1 kbit of on-chip, programmable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on 6 integrated phase-locked loops (PLLs). IGLOOe devices have up to 3 million system gates, supported with up to 504 kbits of true dual-port SRAM and up to 620 user I/Os.

M1 IGLOOe devices support the high-performance, 32-bit Cortex-M1 processor developed by ARM for implementation in FPGAs. Cortex-M1 is a soft processor that is fully implemented in the FPGA fabric. It has a three-stage pipeline that offers a good balance between low power consumption and speed when implemented in an M1 IGLOOe device. The processor runs the ARMv6-M instruction set, has a configurable nested interrupt controller, and can be implemented with or without the debug block. Cortex-M1 is available for free from Microsemi for use in M1 IGLOOe FPGAs.

The ARM-enabled devices have Microsemi ordering numbers that begin with M1AGLE and do not support AES decryption.

Flash*Freeze Technology

The IGLOOe device offers unique Flash*Freeze technology, allowing the device to enter and exit ultra-low power Flash*Freeze mode. IGLOOe devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOOe V2 devices to support a wide range of core voltage (1.2 V to 1.5 V) allows further reduction in power consumption, thus achieving the lowest total system power.

When the IGLOOe device enters Flash*Freeze mode, the device automatically shuts off the clocks and inputs to the FPGA core; when the device exits Flash*Freeze mode, all activity resumes and data is retained.

The availability of low power modes, combined with reprogrammability, a single-chip and single-voltage solution, and availability of small-footprint, high pin-count packages, make IGLOOe devices the best fit for portable electronics.

Table 2-2 • Recommended Operating Conditions [1]

Symbol	Parameter		Commercial	Industrial	Units
T_A	Ambient Temperature		0 to +70	–40 to +85	°C
T_J	Junction Temperature[2]		0 to + 85	–40 to +100	°C
VCC [3]	1.5 V DC core supply voltage[4]		1.425 to 1.575	1.425 to 1.575	V
	1.2 V–1.5 V wide range DC core voltage[5, 6]		1.14 to 1.575	1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage[6]	Programming Mode	3.15 to 3.45	3.15 to 3.45	V
		Operation[7]	0 to 3.6	0 to 3.6	V
VCCPLL[8]	Analog power supply (PLL)	1.5 V DC core supply voltage[4]	1.425 to 1.575	1.425 to 1.575	V
		1.2 V–1.5 V DC core supply voltage[5]	1.14 to 1.575	1.14 to 1.575	V
VCCI and VMV[9]	1.2 V DC supply voltage[5]		1.14 to 1.26	1.14 to 1.26	V
	1.2 V wide range DC supply voltage[5]		1.14 to 1.575	1.14 to 1.575	V
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.0 V DC supply voltage[10]		2.7 to 3.6	2.7 to 3.6	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microsemi recommends that the user follow best design practices using Microsemi's timing and power simulation tools.*
3. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-21 on page 2-20. VCCI should be at the same voltage within a given I/O bank.*
4. *For IGLOOe V5 devices*
5. *For IGLOOe V2 devices only, operating at VCCI ≥ VCC*
6. *All IGLOOe devices (V5 and V2) must be programmed with the VCC core voltage at 1.5 V. Applications using the V2 devices powered by a 1.2 V supply must switch the core supply to 1.5 V for in-system programming.*
7. *VPUMP can be left floating during operation (not programming mode).*
8. *VCCPLL pins should be tied to VCC pins. See the "VCCPLA/B/C/D/E/F PLL Supply Voltage" section for further information.*
9. *VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section for further information.*
10. *3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.*

Calculating Power Dissipation

Quiescent Supply Current

Quiescent supply current (IDD) calculation depends on multiple factors, including operating voltages (VCC, VCCI, and VJTAG), operating temperature, system clock frequency, and power modes usage. Microsemi recommends using the PowerCalculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

Table 2-8 • **Power Supply State per Mode**

	Power Supply Configurations				
Modes/power supplies	**VCC**	**VCCPLL**	**VCCI**	**VJTAG**	**VPUMP**
Flash*Freeze	On	On	On	On	On/off/floating
Sleep	Off	Off	On	Off	Off
Shutdown	Off	Off	Off	Off	Off
No Flash*Freeze	On	On	On	On	On/off/floating

Note: Off: Power supply level = 0 V

Table 2-9 • **Quiescent Supply Current (IDD), IGLOOe Flash*Freeze Mode***

	Core Voltage	AGLE600	AGLE3000	Units
Typical (25°C)	1.2 V	34	95	µA
	1.5 V	72	310	µA

*Note: *IDD includes VCC, VPUMP, VCCI, VCCPLL, and VMV currents. Values do not include I/O static contribution, which is shown in Table 2-13 on page 2-9 and Table 2-14 on page 2-10 (PDC6 and PDC7).*

Table 2-10 • **Quiescent Supply Current (IDD) Characteristics, IGLOOe Sleep Mode***

	Core Voltage	AGLE600	AGLE3000	Units
VCCI/VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	µA
VCCI/VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	µA
VCCI/VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	µA
VCCI/VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	µA
VCCI/VJTAG= 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	µA

*Note: *IDD = N_{BANKS} × ICCI. Values do not include I/O static contribution, which is shown in Table 2-13 on page 2-9 and Table 2-14 on page 2-10 (PDC6 and PDC7).*

Table 2-11 • **Quiescent Supply Current (IDD) Characteristics, IGLOOe Shutdown Mode***

	Core Voltage	AGLE600	AGLE3000	Units
Typical (25°C)	1.2 V / 1.5 V	0	0	µA

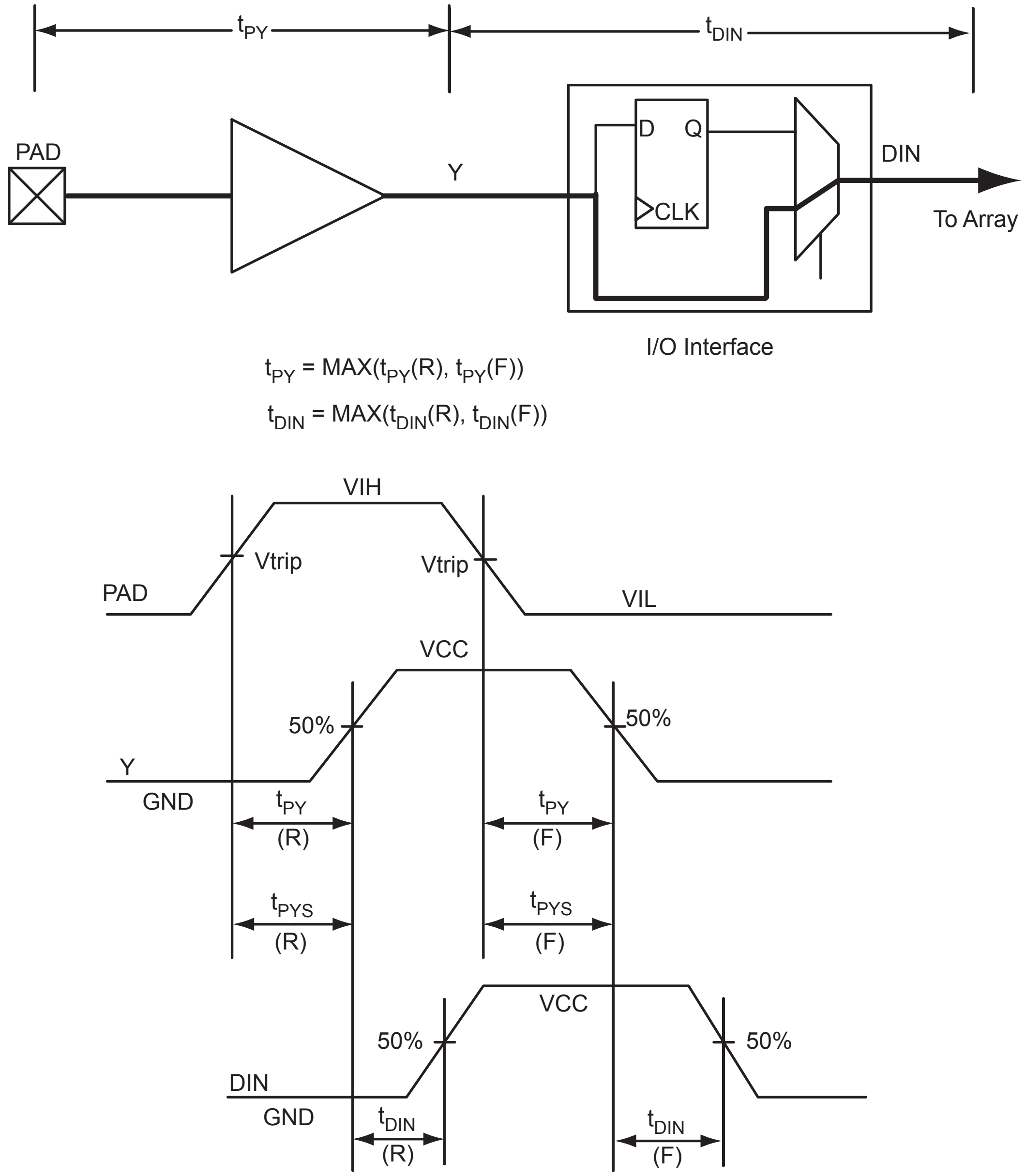


Figure 2-4 • **Input Buffer Timing Model and Delays (example)**

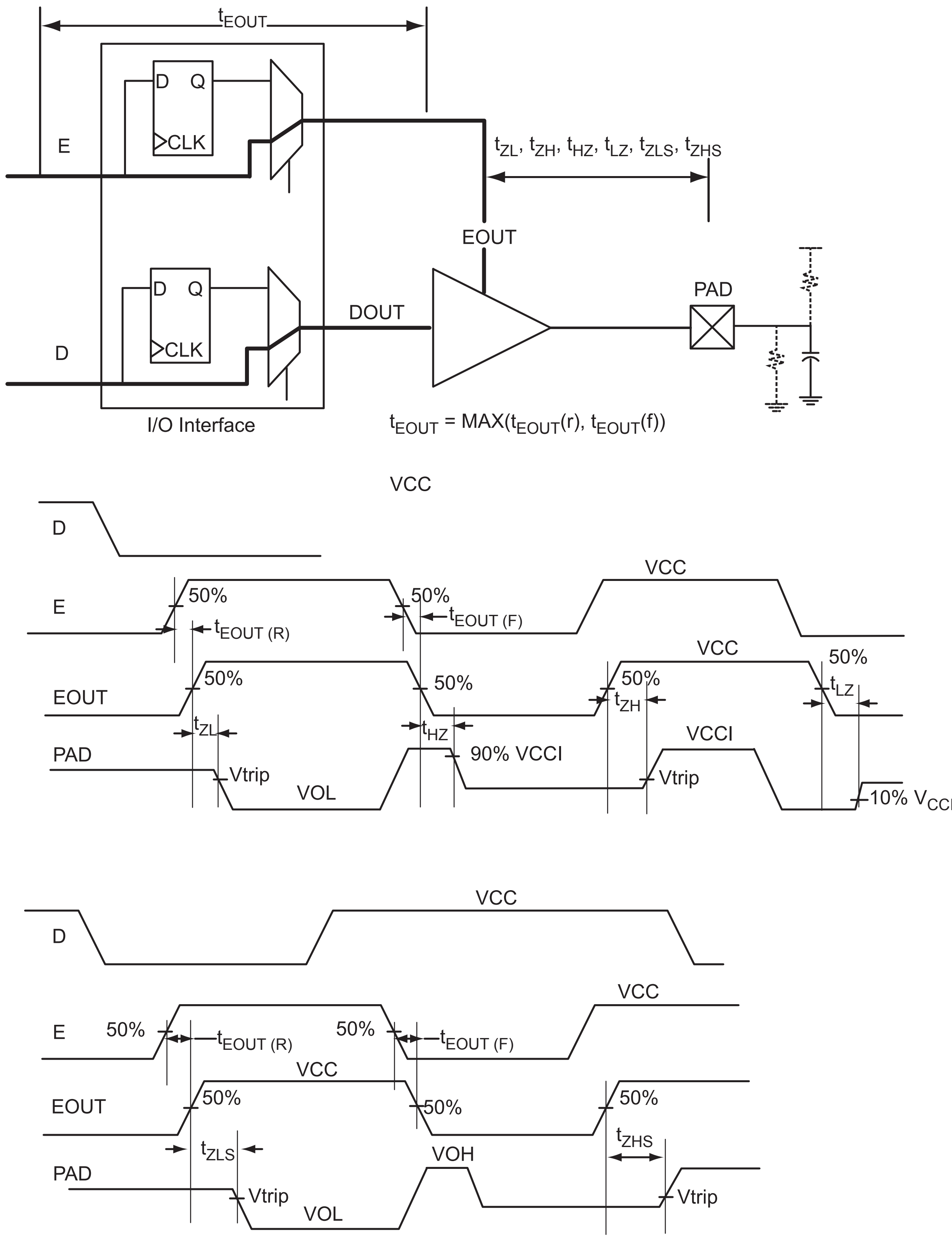


Figure 2-6 • Tristate Output Buffer Timing Model and Delays (example)

Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings
Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI (per standard)

I/O Standard	Drive Strength (mA)	Equivalent Software Default Drive Strength Option[1] (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12	12	High	5	–	1.55	2.47	0.26	1.31	1.58	1.10	2.51	2.04	3.28	3.97	8.29	7.82	ns
3.3 V LVCMOS Wide Range[1,2]	100 µA	12	High	35	–	1.55	3.40	0.26	1.66	2.14	1.10	3.40	2.68	4.55	5.49	9.19	8.46	ns
2.5 V LVCMOS	12	12	High	5	–	1.55	2.51	0.26	1.55	1.77	1.10	2.54	2.22	3.36	3.85	8.33	8.00	ns
1.8 V LVCMOS	12	12	High	5	–	1.55	2.75	0.26	1.53	1.96	1.10	2.78	2.40	3.68	4.56	8.57	8.19	ns
1.5 V LVCMOS	12	12	High	5	–	1.55	3.10	0.26	1.72	2.16	1.10	3.15	2.70	3.86	4.68	8.93	8.49	ns
1.2 V LVCMOS	2	2	High	5	–	1.55	4.06	0.26	2.09	2.95	1.10	3.92	3.46	4.01	3.79	9.71	9.24	ns
1.2 V LVCMOS Wide Range[1,3]	100 µA	2	High	5	–	1.55	4.06	0.26	2.09	2.95	1.10	3.92	3.46	4.01	3.79	9.71	9.24	ns
3.3 V PCI	Per PCI spec	–	High	10	25[4]	1.55	2.76	0.26	1.19	1.63	1.10	2.79	2.16	3.29	3.97	8.58	7.94	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25[4]	1.55	2.76	0.25	1.22	1.58	1.10	2.79	2.16	3.29	3.97	8.58	7.94	ns
3.3 V GTL	20[5]	–	High	10	25	1.55	2.08	0.25	2.76	–	1.10	2.09	2.08	–	–	7.88	7.87	ns
2.5 V GTL	20[5]	–	High	10	25	1.55	2.17	0.25	2.35	–	1.10	2.20	2.13	–	–	7.99	7.91	ns
3.3 V GTL+	35	–	High	10	25	1.55	2.12	0.25	1.62	–	1.10	2.14	2.07	–	–	7.93	7.85	ns
2.5 V GTL+	33	–	High	10	25	1.55	2.25	0.25	1.55	–	1.10	2.27	2.10	–	–	8.06	7.89	ns
HSTL (I)	8	–	High	20	50	1.55	3.09	0.25	1.95	–	1.10	3.11	3.09	–	–	8.90	8.88	ns
HSTL (II)	15	–	High	20	25	1.55	2.94	0.25	1.95	–	1.10	2.98	2.74	–	–	8.77	8.53	ns
SSTL2 (I)	15	–	High	30	50	1.55	2.18	0.25	1.40	–	1.10	2.21	2.03	–	–	7.99	7.82	ns
SSTL2 (II)	18	–	High	30	25	1.55	2.21	0.25	1.40	–	1.10	2.24	1.97	–	–	8.03	7.76	ns
SSTL3 (I)	14	–	High	30	50	1.55	2.33	0.25	1.33	–	1.10	2.36	2.02	–	–	8.15	7.81	ns
SSTL3 (II)	21	–	High	30	25	1.55	2.13	0.25	1.33	–	1.10	2.16	1.89	–	–	7.94	7.67	ns

Notes:

1. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
3. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*
4. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-49 for connectivity. This resistor is not required during normal operation.*
5. *Output drive strength is below JEDEC specification.*
6. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-48 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.97	5.55	0.18	1.31	1.41	0.66	5.66	4.75	2.28	1.96	9.26	8.34	ns
8 mA	Std.	0.97	4.58	0.18	1.31	1.41	0.66	4.67	4.07	2.58	2.53	8.27	7.66	ns
12 mA	Std.	0.97	3.89	0.18	1.31	1.41	0.66	3.97	3.58	2.78	2.91	7.56	7.17	ns
16 mA	Std.	0.97	3.68	0.18	1.31	1.41	0.66	3.75	3.47	2.82	3.01	7.35	7.06	ns
24 mA	Std.	0.97	3.59	0.18	1.31	1.41	0.66	3.66	3.48	2.88	3.37	7.26	7.08	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-49 • 2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.97	2.94	0.18	1.31	1.41	0.66	3.00	2.68	2.28	2.03	6.60	6.27	ns
8 mA	Std.	0.97	2.45	0.18	1.31	1.41	0.66	2.50	2.12	2.58	2.62	6.10	5.72	ns
12 mA	Std.	0.97	2.15	0.18	1.31	1.41	0.66	2.20	1.85	2.78	2.98	5.80	5.45	ns
16 mA	Std.	0.97	2.10	0.18	1.31	1.41	0.66	2.15	1.80	2.82	3.08	5.75	5.40	ns
24 mA	Std.	0.97	2.11	0.18	1.31	1.41	0.66	2.16	1.74	2.88	3.47	5.75	5.33	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

1.2 V DC Core Voltage

Table 2-62 • 1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	8.53	0.26	1.72	2.16	1.10	8.67	7.05	3.39	3.09	14.46	12.83	ns
4 mA	Std.	1.55	7.34	0.26	1.72	2.16	1.10	7.46	6.22	3.70	3.73	13.25	12.01	ns
6 mA	Std.	1.55	6.91	0.26	1.72	2.16	1.10	7.03	6.07	3.77	3.90	12.82	11.85	ns
8 mA	Std.	1.55	6.83	0.26	1.72	2.16	1.10	6.94	6.07	2.91	4.54	12.73	11.86	ns
12 mA	Std.	1.55	6.83	0.26	1.72	2.16	1.10	6.94	6.07	2.91	4.54	12.73	11.86	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-63 • 1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.72	0.26	1.72	2.16	1.10	3.78	3.45	3.38	3.19	9.56	9.24	ns
4 mA	Std.	1.55	3.23	0.26	1.72	2.16	1.10	3.27	2.92	3.69	3.83	9.06	8.71	ns
6 mA	Std.	1.55	3.13	0.26	1.72	2.16	1.10	3.18	2.82	3.76	4.01	8.96	8.61	ns
8 mA	Std.	1.55	3.10	0.26	1.72	2.16	1.10	3.15	2.70	3.86	4.68	8.93	8.49	ns
12 mA	Std.	1.55	3.10	0.26	1.72	2.16	1.10	3.15	2.70	3.86	4.68	8.93	8.49	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer.

Table 2-64 • **Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

1.2 V LVCMOS[1]	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[2]	IIH[3]
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[4]**	**Max. mA[4]**	**μA[5]**	**μA[5]**
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	20	26	10	10

Notes:

1. *Applicable to V2 devices ONLY.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
4. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

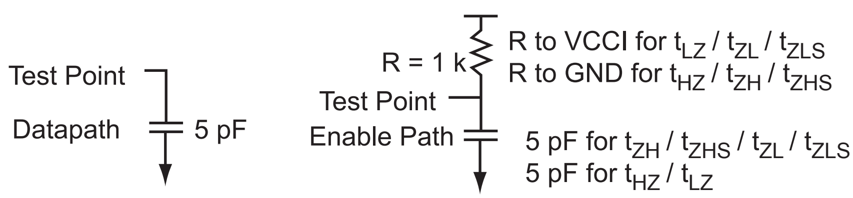


Figure 2-11 • **AC Loading**

Table 2-65 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	1.2	0.6	–	5

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-23 for a complete table of trip points.*

Timing Characteristics

1.2 V DC Core Voltage

Table 2-66 • 1.2 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	9.92	0.26	2.09	2.95	1.10	9.53	7.48	4.02	3.67	15.31	13.26	ns

Notes:
1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Table 2-67 • 1.2 LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	4.06	0.26	2.09	2.95	1.10	3.92	3.46	4.01	3.79	9.71	9.24	ns

Notes:
1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

1.2 V LVCMOS Wide Range

Table 2-68 • Minimum and Maximum DC Input and Output Levels

1.2 V LVCMOS Wide Range[1]		VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[2]	IIH[3]
Drive Strength	Equivalent Software Default Drive Strength Option[4]	Min. (V)	Max. (V)	Min. (V)	Max (V)	Max. (V)	Min. (V)	µA	µA	Max. (mA)[5]	Max. (mA)[5]	µA[6]	µA[6]
100 µA	2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	100	100	20	26	10	10

Notes:
1. *Applicable to V2 devices ONLY.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
4. *The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
5. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
6. *Currents are measured at 85°C junction temperature.*
7. *Software default selection highlighted in gray.*

Timing Characteristics

Refer to LVCMOS 1.2 V (normal range) "Timing Characteristics" on page 2-48 for worst-case timing.

Input Register

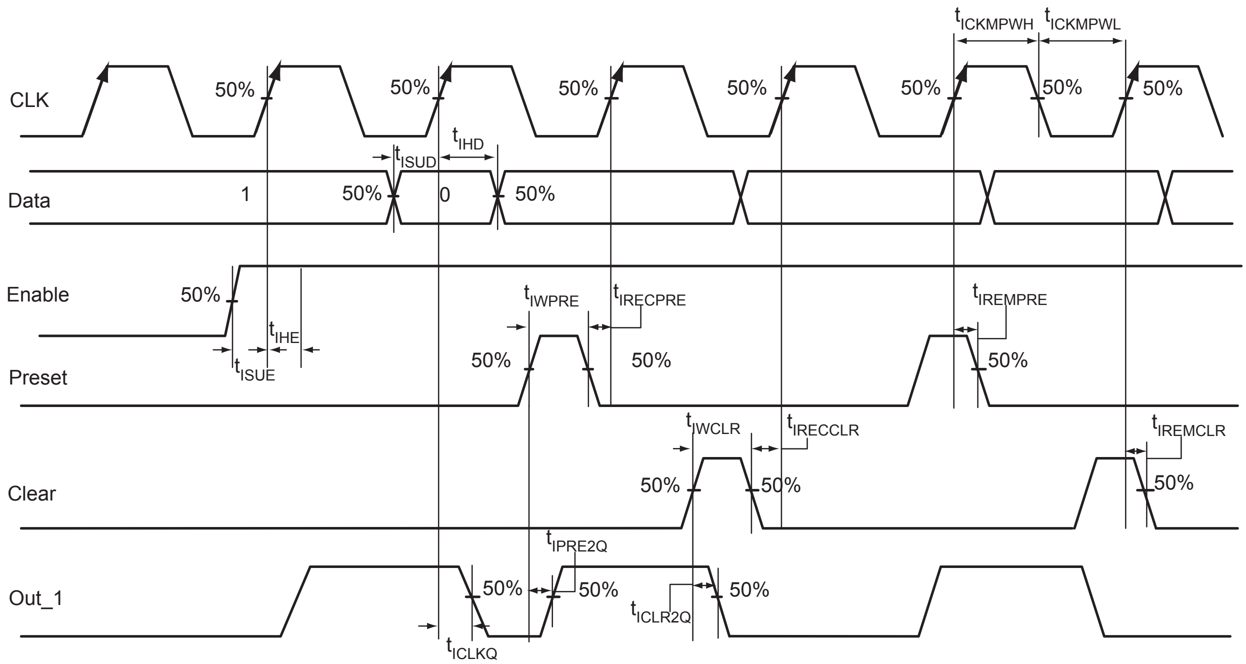


Figure 2-28 • Input Register Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-123 • Input Data Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.42	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.47	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.67	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.79	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.79	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

DDR Module Specifications

Input DDR Module

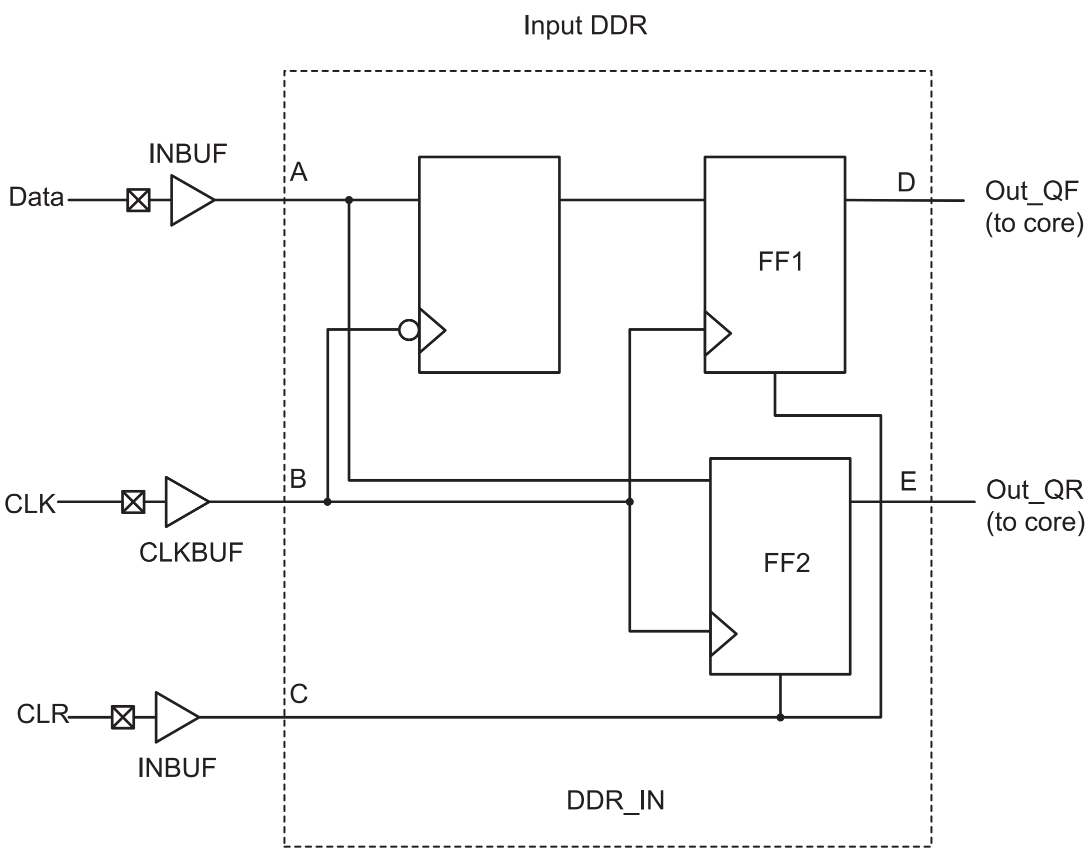


Figure 2-31 **• Input DDR Timing Model**

Table 2-129 **• Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

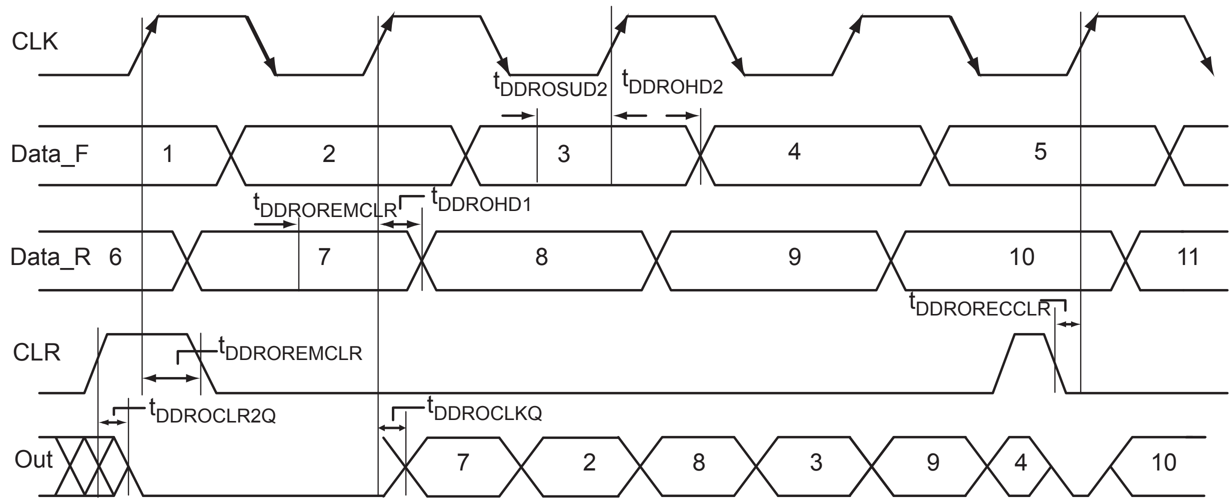


Figure 2-34 • **Output DDR Timing Diagram**

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-91. Table 2-139 and Table 2-141 present minimum and maximum global clock delays within the device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-139* • AGLE600 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.48	1.82	ns
t_{RCKH}	Input High Delay for Global Clock	1.52	1.94	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.42	ns

Notes:

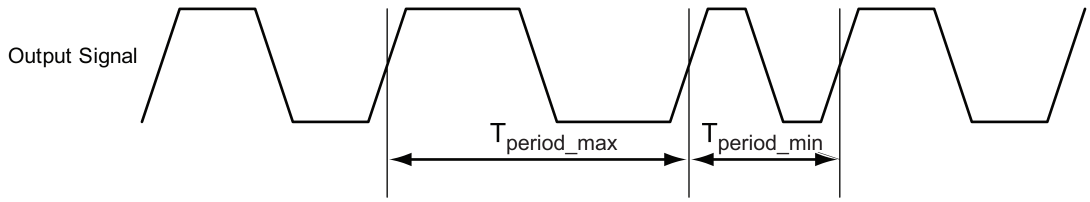
1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-140* • AGLE3000 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.00	2.34	ns
t_{RCKH}	Input High Delay for Global Clock	2.09	2.51	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.42	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*



Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} – T_{period\_min}$.

Figure 2-40 • **Peak-to-Peak Jitter Definition**

3 – Pin Descriptions and Packaging

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V for IGLOOe V5 devices, and 1.2 V or 1.5 V for IGLOOe V2 devices. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

For IGLOOe V2 devices, VCC can be switched dynamically from 1.2 V to 1.5 V or vice versa. This allows in-system programming (ISP) when VCC is at 1.5 V and the benefit of low power operation when VCC is at 1.2 V.

VCCIBx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on IGLOOe devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

VMVx **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V or 1.2 V, depending on the device.

- 1.5 V for IGLOOe devices
- 1.2 V or 1.5 V for IGLOOe V2 devices

When the PLLs are not used, the place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section in the "Clock Conditioning Circuits in Low Power Flash FPGAs and Mixed Signal FPGAs" chapter in the *IGLOOe FPGA Fabric User's Guide* for a complete board solution for the PLL analog power supply and ground.

There are six VCCPLX pins on IGLOOe devices.

Table 3-1 shows the Flash*Freeze pin location on the available packages. The Flash*Freeze pin location is independent of device (except for a PQ208 package), allowing migration to larger or smaller IGLOO devices while maintaining the same pin location on the board. Refer to the "Flash*Freeze Technology and Low Power Modes" chapter of the *IGLOOe FPGA Fabric User's Guide* for more information on I/O states during Flash*Freeze mode.

***Table 3-1* • Flash*Freeze Pin Locations for IGLOOe Devices**

Package	Flash*Freeze Pin
FG256	T3
FG484	W6
FG896	AH4

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 3-2 for more information.

***Table 3-2* • Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance [1,2]
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *The TCK pin can be pulled-up or pulled-down.*
2. *The TRST pin is pulled-down.*
3. *Equivalent parallel resistance if more than one device is on the JTAG chain*

FG484		FG484		FG484	
Pin Number	AGLE600 Function	Pin Number	AGLE600 Function	Pin Number	AGLE600 Function
C18	GND	E9	IO10NDB0V1	F22	NC
C19	NC	E10	IO12NDB0V2	G1	IO127NDB7V1
C20	NC	E11	IO16PDB0V2	G2	IO127PDB7V1
C21	NC	E12	IO20NDB1V0	G3	NC
C22	VCCIB2	E13	IO24NDB1V0	G4	IO128PDB7V1
D1	NC	E14	IO24PDB1V0	G5	IO129PDB7V1
D2	NC	E15	GBC1/IO33PDB1V1	G6	GAC2/IO132PDB7V1
D3	NC	E16	GBB0/IO34NDB1V1	G7	VCOMPLA
D4	GND	E17	GNDQ	G8	GNDQ
D5	GAA0/IO00NDB0V0	E18	GBA2/IO36PDB2V0	G9	IO09NDB0V1
D6	GAA1/IO00PDB0V0	E19	IO42NDB2V0	G10	IO09PDB0V1
D7	GAB0/IO01NDB0V0	E20	GND	G11	IO13PDB0V2
D8	IO05PDB0V0	E21	NC	G12	IO21PDB1V0
D9	IO10PDB0V1	E22	NC	G13	IO25PDB1V0
D10	IO12PDB0V2	F1	NC	G14	IO27NDB1V0
D11	IO16NDB0V2	F2	IO131NDB7V1	G15	GNDQ
D12	IO23NDB1V0	F3	IO131PDB7V1	G16	VCOMPLB
D13	IO23PDB1V0	F4	IO133NDB7V1	G17	GBB2/IO37PDB2V0
D14	IO28NDB1V1	F5	IO134NDB7V1	G18	IO39PDB2V0
D15	IO28PDB1V1	F6	VMV7	G19	IO39NDB2V0
D16	GBB1/IO34PDB1V1	F7	VCCPLA	G20	IO43PDB2V0
D17	GBA0/IO35NDB1V1	F8	GAC0/IO02NDB0V0	G21	IO43NDB2V0
D18	GBA1/IO35PDB1V1	F9	GAC1/IO02PDB0V0	G22	NC
D19	GND	F10	IO15NDB0V2	H1	NC
D20	NC	F11	IO15PDB0V2	H2	NC
D21	NC	F12	IO20PDB1V0	H3	VCC
D22	NC	F13	IO25NDB1V0	H4	IO128NDB7V1
E1	NC	F14	IO27PDB1V0	H5	IO129NDB7V1
E2	NC	F15	GBC0/IO33NDB1V1	H6	IO132NDB7V1
E3	GND	F16	VCCPLB	H7	IO130PDB7V1
E4	GAB2/IO133PDB7V1	F17	VMV2	H8	VMV0
E5	GAA2/IO134PDB7V1	F18	IO36NDB2V0	H9	VCCIB0
E6	GNDQ	F19	IO42PDB2V0	H10	VCCIB0
E7	GAB1/IO01PDB0V0	F20	NC	H11	IO13NDB0V2
E8	IO05NDB0V0	F21	NC	H12	IO21NDB1V0

FG484		FG484		FG484	
Pin Number	AGLE600 Function	Pin Number	AGLE600 Function	Pin Number	AGLE600 Function
H13	VCCIB1	K4	IO124NDB7V0	L17	GCA0/IO52NPB3V0
H14	VCCIB1	K5	IO125NDB7V0	L18	VCOMPLC
H15	VMV1	K6	IO126NDB7V0	L19	GCB0/IO51NPB2V1
H16	GBC2/IO38PDB2V0	K7	GFC1/IO120PPB7V0	L20	IO49PPB2V1
H17	IO37NDB2V0	K8	VCCIB7	L21	IO47NDB2V1
H18	IO41NDB2V0	K9	VCC	L22	IO47PDB2V1
H19	IO41PDB2V0	K10	GND	M1	NC
H20	VCC	K11	GND	M2	IO114NPB6V1
H21	NC	K12	GND	M3	IO117NDB6V1
H22	NC	K13	GND	M4	GFA2/IO117PDB6V1
J1	IO123NDB7V0	K14	VCC	M5	GFA1/IO118PDB6V1
J2	IO123PDB7V0	K15	VCCIB2	M6	VCCPLF
J3	NC	K16	GCC1/IO50PPB2V1	M7	IO116NDB6V1
J4	IO124PDB7V0	K17	IO44NDB2V1	M8	GFB2/IO116PDB6V1
J5	IO125PDB7V0	K18	IO44PDB2V1	M9	VCC
J6	IO126PDB7V0	K19	IO49NPB2V1	M10	GND
J7	IO130NDB7V1	K20	IO45NPB2V1	M11	GND
J8	VCCIB7	K21	IO48NDB2V1	M12	GND
J9	GND	K22	IO46NDB2V1	M13	GND
J10	VCC	L1	NC	M14	VCC
J11	VCC	L2	IO122PDB7V0	M15	GCB2/IO54PPB3V0
J12	VCC	L3	IO122NDB7V0	M16	GCA1/IO52PPB3V0
J13	VCC	L4	GFB0/IO119NPB7V0	M17	GCC2/IO55PPB3V0
J14	GND	L5	GFA0/IO118NDB6V1	M18	VCCPLC
J15	VCCIB2	L6	GFB1/IO119PPB7V0	M19	GCA2/IO53PDB3V0
J16	IO38NDB2V0	L7	VCOMPLF	M20	IO53NDB3V0
J17	IO40NDB2V0	L8	GFC0/IO120NPB7V0	M21	IO56PDB3V0
J18	IO40PDB2V0	L9	VCC	M22	NC
J19	IO45PPB2V1	L10	GND	N1	IO114PPB6V1
J20	NC	L11	GND	N2	IO111NDB6V1
J21	IO48PDB2V1	L12	GND	N3	NC
J22	IO46PDB2V1	L13	GND	N4	GFC2/IO115PPB6V1
K1	IO121NDB7V0	L14	VCC	N5	IO113PPB6V1
K2	IO121PDB7V0	L15	GCC0/IO50NPB2V1	N6	IO112PDB6V1
K3	NC	L16	GCB1/IO51PPB2V1	N7	IO112NDB6V1

FG896	
Pin Number	AGLE3000 Function
L26	IO87NDB2V0
L27	IO97PDB2V1
L28	IO101PDB2V2
L29	IO103PDB2V2
L30	IO119NDB3V0
M1	IO282NDB7V1
M2	IO282PDB7V1
M3	IO292NDB7V2
M4	IO292PDB7V2
M5	IO283NDB7V1
M6	IO285PDB7V1
M7	IO287PDB7V1
M8	IO289PDB7V1
M9	IO289NDB7V1
M10	VCCIB7
M11	VCC
M12	GND
M13	GND
M14	GND
M15	GND
M16	GND
M17	GND
M18	GND
M19	GND
M20	VCC
M21	VCCIB2
M22	NC
M23	IO104PPB2V2
M24	IO102PDB2V2
M25	IO102NDB2V2
M26	IO95PDB2V1
M27	IO97NDB2V1
M28	IO101NDB2V2
M29	IO103NDB2V2
M30	IO119PDB3V0

FG896	
Pin Number	AGLE3000 Function
N1	IO276PDB7V0
N2	IO278PDB7V0
N3	IO280PDB7V0
N4	IO284PDB7V1
N5	IO279PDB7V0
N6	IO285NDB7V1
N7	IO287NDB7V1
N8	IO281NDB7V0
N9	IO281PDB7V0
N10	VCCIB7
N11	VCC
N12	GND
N13	GND
N14	GND
N15	GND
N16	GND
N17	GND
N18	GND
N19	GND
N20	VCC
N21	VCCIB2
N22	IO106NDB2V3
N23	IO106PDB2V3
N24	IO108PDB2V3
N25	IO108NDB2V3
N26	IO95NDB2V1
N27	IO99NDB2V2
N28	IO99PDB2V2
N29	IO107PDB2V3
N30	IO107NDB2V3
P1	IO276NDB7V0
P2	IO278NDB7V0
P3	IO280NDB7V0
P4	IO284NDB7V1
P5	IO279NDB7V0

FG896	
Pin Number	AGLE3000 Function
P6	GFC1/IO275PDB7V0
P7	GFC0/IO275NDB7V0
P8	IO277PDB7V0
P9	IO277NDB7V0
P10	VCCIB7
P11	VCC
P12	GND
P13	GND
P14	GND
P15	GND
P16	GND
P17	GND
P18	GND
P19	GND
P20	VCC
P21	VCCIB2
P22	GCC1/IO112PDB2V3
P23	IO110PDB2V3
P24	IO110NDB2V3
P25	IO109PPB2V3
P26	IO111NPB2V3
P27	IO105PDB2V2
P28	IO105NDB2V2
P29	GCC2/IO117PDB3V0
P30	IO117NDB3V0
R1	GFC2/IO270PDB6V4
R2	GFB1/IO274PPB7V0
R3	VCOMPLF
R4	GFA0/IO273NDB6V4
R5	GFB0/IO274NPB7V0
R6	IO271NDB6V4
R7	GFB2/IO271PDB6V4
R8	IO269PDB6V4
R9	IO269NDB6V4
R10	VCCIB7