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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HC11
Core Size	8-Bit
Speed	4MHz
Connectivity	MI Bus, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	50
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.29x29.29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc711p2cfne4

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2.10 MODA and MODB (MODA/$\overline{\text{LIR}}$ and MODB/VSTBY)

During reset, MODA and MODB select one of the four operating modes. Refer to **Operating Modes and On-Chip Memory**.

After the operating mode has been selected, the $\overline{\text{LIR}}$ pin provides an open-drain output to indicate that execution of an instruction has begun. The $\overline{\text{LIR}}$ pin is normally configured for wired-OR operation (only pulls low). In order to detect consecutive instructions in a high-speed application, this signal can be made to drive high for a short time to prevent false triggering. A series of E clock cycles occurs during execution of each instruction. The $\overline{\text{LIR}}$ signal goes low during the first E clock cycle of each instruction (opcode fetch). This output is provided for assistance in program debugging and its operation is controlled by the LIRDV bit in the OPT2 register.

The VSTBY pin is used to input RAM stand-by power. The MCU is powered from the VDD pin unless the difference between the level of VSTBY and VDD is greater than one MOS threshold (about 0.7 volts). When these voltages differ by more than 0.7 volts, the internal 1024-byte RAM and part of the reset logic are powered from VSTBY rather than VDD. This allows RAM contents to be retained without VDD power applied to the MCU. Reset must be driven low before V_{DD} is removed and must remain low until V_{DD} has been restored to a valid level.

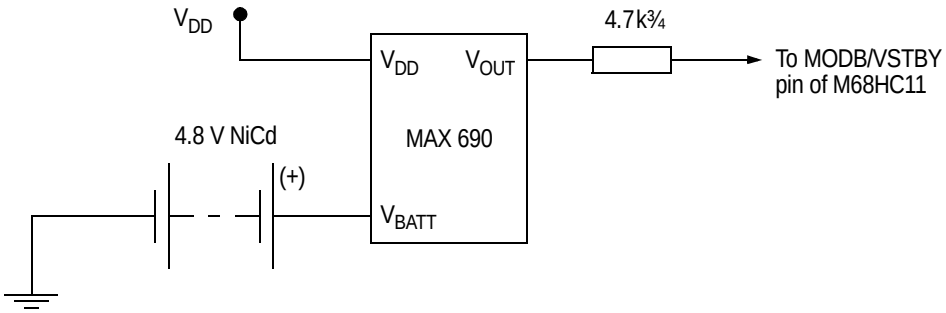

Figure 2-5. RAM stand-by connections

The CWOM control bit in the OPT2 register disables port C's P-channel output drivers. Because the N-channel driver is not affected by CWOM, setting CWOM causes port C to become an open-drain-type output port suitable for wired-OR operation. In wired-OR mode (PORTC bits at logic level zero), the pins are actively driven low by the N-channel driver. When a port C bit is at logic level one, the associated pin is in a high impedance state as neither the N-channel nor the P-channel devices are active. It is customary to have an external pull-up resistor on lines that are driven by open-drain devices. Port C can only be configured for wired-OR operation when the MCU is in single chip mode. For further information, refer to **Parallel Input/Output**.

2.13.4 Port D

Port D, a 6-bit general-purpose I/O port, has a data register (PORTD) and a data direction register (DDRD). The six port D lines (D[5:0]) can be used for general-purpose I/O, for one of the serial communications interfaces (SCI1, bits [0:1]) and for the serial peripheral interface (SPI, bits [2:5]) subsystem.

PORTD can be read at any time: inputs return the pin level; outputs return the pin driver input level. If PORTD is written, the data is stored in internal latches and are driven only if port D is configured for general-purpose output.

For further information, refer to **Parallel Input/Output**, **Serial Communications Interface (SCI)** and **Serial Peripheral Interface (SPI)**.

2.13.5 Port E

Port E, PE/AD[7:0], is an input-only port that can also be used as the analog inputs for the analog-to-digital converter.

For further information, refer to **Parallel Input/Output** and **Analog-to-Digital Converter**.

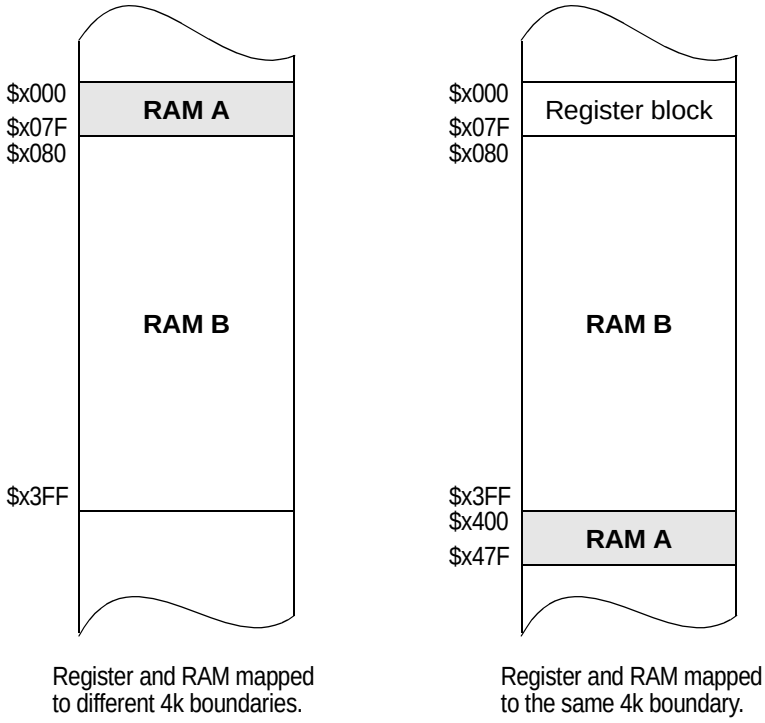

Figure 3-2. RAM and register overlap

3.5.2.3 INIT2 — EEPROM mapping and MI BUS delay register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
EEPROM mapping (INIT2)	$0037	EE3	EE2	EE1	EE0	M3DL1	M3DL0	M2DL1	M2DL0	0000 0000

This register determines the location of EEPROM in the memory map. INIT2 may be read at any time but bits 7–4 may be written only once after reset in normal modes (bits 3–0 may be written at any time).

EE[3:0] — EEPROM map position

EEPROM is located at $xD80–$xFFF, where x is the hexadecimal digit represented by EE[3:0]. Refer to **Table 3-6**.

3.6.2.1 PPROG — EEPROM programming control register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
EEPROM programming (PPROG)	$003B	ODD	EVEN	0	BYTE	ROW	ERASE	EELAT	EEPGM	0000 0000

NOTE: *Writes to EEPROM addresses are inhibited while EEPGM is one. A write to a different EEPROM location is prevented while a program or erase operation is in progress.*

ODD — Program odd rows in half of EEPROM (Test)

EVEN — Program even rows in half of EEPROM (Test)

If both ODD and EVEN are set to one then all odd and even rows in half of the EEPROM will be programmed with the same data, within one programming cycle.

Bit 5 — Not implemented; always reads zero.

BYTE — EEPROM byte erase mode
1 = Erase only one byte of EEPROM.
0 = Row or bulk erase mode used.

ROW — EEPROM row/bulk erase mode (only valid when BYTE = 0)
1 = Erase only one 16 byte row of EEPROM.
0 = Erase all 640 bytes of EEPROM.

Table 3-8. Erase mode selection

Byte	Row	Action
0	0	Bulk erase (all 640 bytes)
0	1	Row erase (16 bytes)
1	0	Byte erase
1	1	Byte erase

ERASE — Erase/normal control for EEPROM
1 = Erase mode.
0 = Normal read or program mode.

4.6.2 DDRD — Data direction register for port D

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Data direction D (DDRD)	$0009	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	0000 0000

Bits [7:6] — Reserved; always read zero

DDD[5:0] — Data direction for port D

1 = The corresponding pin is configured as an output.

0 = The corresponding pin is configured as an input.

4.7 Port E

Port E is an 8-bit input-only port. In addition to their input capability, port E pins are shared with A/D functions, as shown in the following table.

Pin	Alternate function
PE0	AD0
PE1	AD1
PE2	AD2
PE3	AD3
PE4	AD4
PE5	AD5
PE6	AD6
PE7	AD7

See **Analog-to-Digital Converter** for more information.

On reset the pins are configured as general purpose high-impedance inputs.

Section 5. Serial Communications Interface (SCI)

5.1 Contents

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5.3 Data format 88
5.4 Transmit operation 89
5.5 Receive operation 89
5.6 Wakeup feature 91
5.7 SCI error detection 92
5.8 SCI registers 93
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5.10 Additional SCI subsystems 104

5.2 Introduction

The serial communications interface (SCI) is a universal asynchronous receiver transmitter (UART). It has a non-return to zero (NRZ) format (one start, eight or nine data, and one stop bit) that is compatible with standard RS-232 systems.

The MC68HC11P2 contains three serial communications interfaces, all having similar operation. For ease of reference, a full description of SCI1 (PD0/RXD1, PD1/TXD1) is given first, followed by summaries for **SCI2** and **SCI3**, detailing their differences.

The OR is cleared when the SCSR is read (with OR set), followed by a read of the SCI data registers.

The noise flag (NF) bit is set if there is noise on any of the received bits, including the start and stop bits. The NF bit is not set until the RDRF flag is set. The NF bit is cleared when the SCSR is read (with FE equal to one) followed by a read of the SCI data registers.

When no stop bit is detected in the received data character, the framing error (FE) bit is set. FE is set at the same time as the RDRF. If the byte received causes both framing and overrun errors, the processor only recognizes the overrun error. The framing error flag inhibits further transfer of data into the SCI data registers until it is cleared. The FE bit is cleared when the SCSR is read (with FE equal to one) followed by a read of the SCI data registers.

The parity error flag (PF) is set if received data has incorrect parity. The flag is cleared by a read of SCSR1 with PE set, followed by a read of SCDR.

5.8 SCI registers

There are eight addressable registers in the SCI. SCBDH, SCBDL, SCCR1, and SCCR2 are control registers. The contents of these registers control functions and indicate conditions within the SCI. The status registers SCSR1 and SCSR2 contain bits that indicate certain conditions within the SCI. SCDRH and SCDRL are SCI data registers. These double buffered registers are used for the transmission and reception of data, and are used to form the 9-bit data word for the SCI. If the SCI is being used with 7 or 8-bit data, only SCDRL needs to be accessed. Note that if 9-bit data format is used, the upper register should be written first to ensure that it is transferred to the transmitter shift register with the lower register.

5.10.1.1 S2BDH, S2BDL — SCI2/3 baud rate control registers

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
SCI/MI 2/3 baud high (S2BDH)	$0050	B2TST	B2SPL	0	S2B12	S2B11	S2B10	S2B9	S2B8	0000 0000
SCI/MI 2/3 baud low (S2BDL)	$0051	S2B7	S2B6	S2B5	S2B4	S2B3	S2B2	S2B1	S2B0	0000 0100

The contents of this register determine the baud rate for both SCI2 and SCI3. For details of the bits and the corresponding baud rates see **SCBDH, SCBDL — SCI baud rate control registers**. This register also controls the MI BUS clock rate (see **Motorola Interconnect Bus (MI BUS)**).

5.10.1.2 S2CR1 — SCI2 control register 1

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
SCI/MI 2 control 1 (S2CR1)	$0052	LOPS2	WOMS 2	MIE2	M2	WAKE 2	ILT2	PE2	PT2	0000 0000

The S2CR1 register provides the control bits that determine word length and select the method used for the wakeup feature. Bit 5 has an MI BUS control function detailed below (for details of the other bits see **SCCR1 — SCI control register 1**).

MIE2 — Motorola interface bus enable 2

1 = MI BUS is enabled for this subsystem.

0 = The SCI functions normally.

When MIE2 is set, the SCI2 registers, bits and pins assume the functionality required for MI BUS.

5.10.1.3 S2CR2 — SCI2 control register 2

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
SCI/MI 2 control 2 (S2CR2)	$0053	TIE2	TCIE2	RIE2	ILIE2	TE2	RE2	RWU2	SBK2	0000 0000

The S2CR2 register provides the control bits that enable or disable individual SCI functions. For details of the bits, see **SCCR2 — SCI**

6.8 Interfacing to MI BUS

Physically the MI BUS consists of only a single wire. In the example shown in **Figure 6-4**, only a single transistor and a few passive components are required to connect up the MC68HC11P2 for full MI BUS operation.

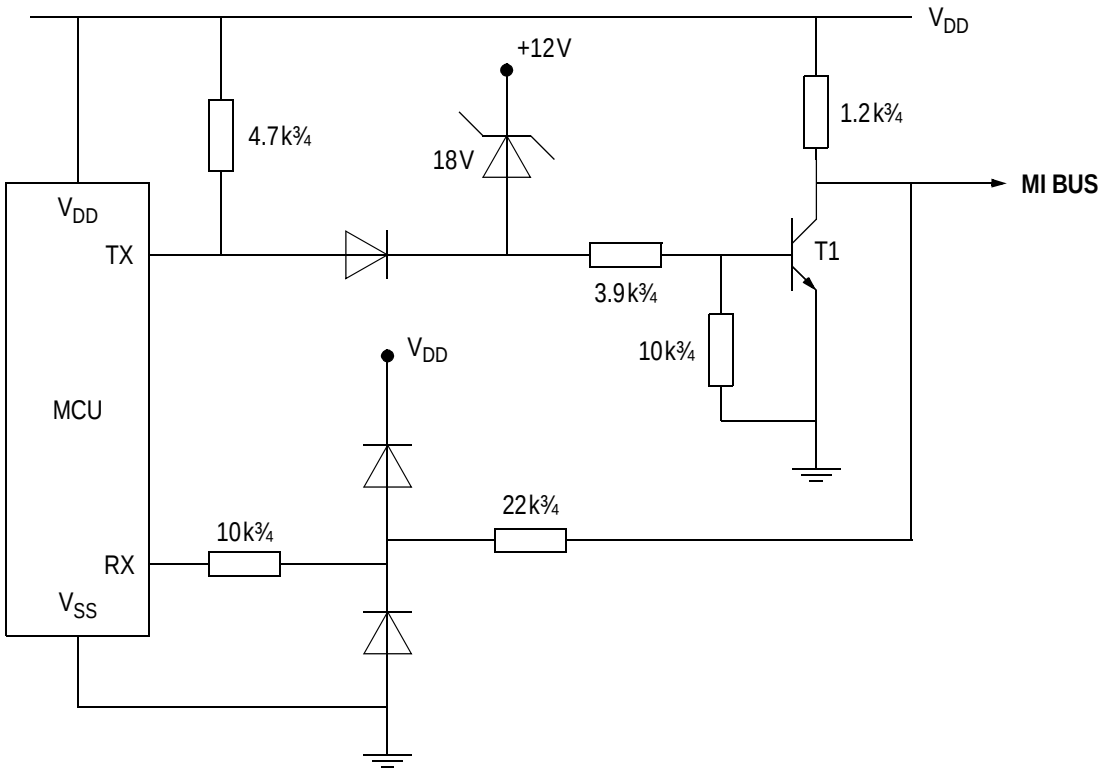


Figure 6-4. A typical interface between the MC68HC11P2 and the MI BUS

The transistor serves both to drive the MI BUS during the push field and to protect the MCU TX pin from voltage transients generated in the wiring. Without the transistor, EMI could damage the TX pin. Similarly, the input pin (RX) is protected from EMI by clamping it to the MCU supply rails with two diodes. When a load dump occurs, the zener diode (18V) is switched on and hence turns the transistor on; this generates the logic '0' state on the MI BUS. After eight time slots (200ms) of continuous '0' state, all devices on the MI BUS will have their outputs disabled.

optionally be used to indicate a multiple master bus contention. Refer to **Figure 7-2**.

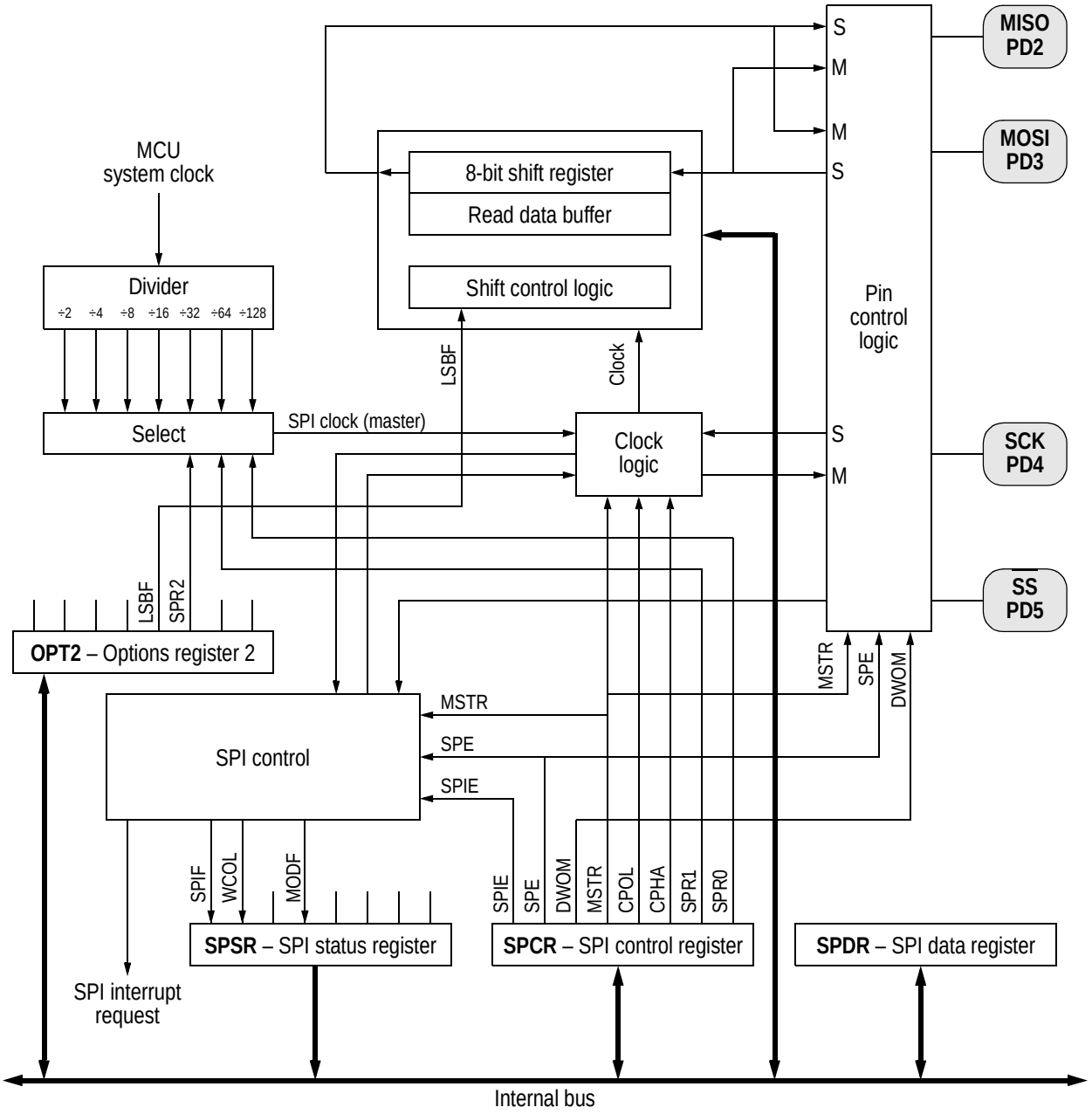


Figure 7-1. SPI block diagram

IC1F–IC3F — Input capture x flag

1 = Selected edge has been detected on corresponding port pin.

0 = Selected edge has not been detected on corresponding port pin.

These flags are set each time a selected active edge is detected on the ICx input line

8.5.9 TMSK2 — Timer interrupt mask register 2

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Timer interrupt mask 2 (TMSK2)	$0024	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0	0000 0000

Use this 8-bit register to enable or inhibit timer overflow and real-time interrupts. The timer prescaler control bits are included in this register.

NOTE: *Bits in TMSK2 correspond bit for bit with flag bits in TFLG2. Ones in TMSK2 enable the corresponding interrupt sources.*

TOI — Timer overflow interrupt enable

1 = Timer overflow interrupt requested when TOF is set.

0 = TOF interrupts disabled.

RTII — Real-time interrupt enable (refer to **Real-time interrupt**)

PAOVI — Pulse accumulator overflow interrupt enable (refer to **Pulse accumulator status and interrupt bits**)

PAII — Pulse accumulator input edge interrupt enable (refer to **Pulse accumulator status and interrupt bits**)

PR[1:0] — Timer prescaler select

PR[1:0]	Prescaler
0 0	1
0 1	4
1 0	8
1 1	16

Bits [5:4] — Not implemented; always read zero

PWEN[4:1] — Pulse width channels 4–1
1 = Channel enabled on the associated port pin.
0 = Channel disabled.

8.9.6 PWCNT1–4 — PWM timer counter registers 1 to 4

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Pulse width count 1 (PWCNT1)	$0064	(bit 7)	(6)	(5)	(4)	(3)	(2)	(1)	(bit 0)	0000 0000
Pulse width count 2 (PWCNT2)	$0065	(bit 7)	(6)	(5)	(4)	(3)	(2)	(1)	(bit 0)	0000 0000
Pulse width count 3 (PWCNT3)	$0066	(bit 7)	(6)	(5)	(4)	(3)	(2)	(1)	(bit 0)	0000 0000
Pulse width count 4 (PWCNT4)	$0067	(bit 7)	(6)	(5)	(4)	(3)	(2)	(1)	(bit 0)	0000 0000

Each channel has its own counter which can be read at any time without affecting the count or the operation of the PWM channel. Writing to a counter causes it to be reset to $00; this is generally done before the counter is enabled. A counter may also be written to whilst it is enabled; this may cause a truncated PWM period.

8.9.7 PWPER1–4 — PWM timer period registers 1 to 4

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Pulse width period 1 (PWPER1)	$0068	(bit 7)	(6)	(5)	(4)	(3)	(2)	(1)	(bit 0)	1111 1111
Pulse width period 2 (PWPER2)	$0069	(bit 7)	(6)	(5)	(4)	(3)	(2)	(1)	(bit 0)	1111 1111
Pulse width period 3 (PWPER3)	$006A	(bit 7)	(6)	(5)	(4)	(3)	(2)	(1)	(bit 0)	1111 1111
Pulse width period 4 (PWPER4)	$006B	(bit 7)	(6)	(5)	(4)	(3)	(2)	(1)	(bit 0)	1111 1111

There is one period register for each channel. The value in this register determines the period of the associated PWM timer channel. PWPERx is connected internally to a buffer which compares directly with the counter register. The period value in PWPERx is loaded into the buffer when the counter is cleared by the termination of the previous period or by a write to the counter. This register can be written at any time, and the written value will take effect from the start of the next PWM timer cycle.

10.3.1 Power-on reset

A positive transition on VDD generates a power-on reset (POR), which is used only for power-up conditions. POR cannot be used to detect drops in power supply voltages. A 4064 t_{CYC} (internal clock cycle) delay after the oscillator becomes active allows the clock generator to stabilize. If $\overline{\text{RESET}}$ is at logical zero at the end of 4064 t_{CYC}, the CPU remains in the reset condition until $\overline{\text{RESET}}$ goes to logical one.

It is important to protect the MCU during power transitions. Most M68HC11 systems need an external circuit that holds the $\overline{\text{RESET}}$ pin low whenever V_{DD} is below the minimum operating level. This external voltage level detector, or other external reset circuits, are the usual source of reset in a system. The POR circuit only initializes internal circuitry during cold starts. Refer to **Figure 2-2**.

10.3.2 External reset ($\overline{\text{RESET}}$)

The CPU distinguishes between internal and external reset conditions by sensing whether the reset pin rises to a logic one in less than two E clock cycles after an internal device releases reset. When a reset condition is sensed, the $\overline{\text{RESET}}$ pin is driven low by an internal device for four E clock cycles, then released. Two E clock cycles later it is sampled. If the pin is still held low, the CPU assumes that an external reset has occurred. If the pin is high, it indicates that the reset was initiated internally by either the COP system or the clock monitor. It is not advisable to connect an external resistor capacitor (RC) power-up delay circuit to the reset pin of M68HC11 devices because the circuit charge time constant can cause the device to misinterpret the type of reset that occurred.

10.3.3 COP reset

The MCU includes a COP system to help protect against software failures. When the COP is enabled, the software is responsible for keeping a free-running watchdog timer from timing out. When the

10.4.10 Analog-to-digital converter

The A/D converter configuration is indeterminate after reset. The ADPU bit is cleared by reset, which disables the A/D system. The conversion complete flag is cleared by reset.

10.4.11 System

The EEPROM programming controls are disabled, so the memory system is configured for normal read operation. PSEL[4:0] are initialized with the binary value %00110, causing the external $\overline{\text{IRQ}}$ pin to have the highest I-bit interrupt priority. The $\overline{\text{IRQ}}$ pin is configured for level-sensitive operation (for wired-OR systems). The RBOOT, SMOD, and MDA bits in the HPRIO register reflect the status of the MODB and MODA inputs at the rising edge of reset. The DLY control bit is set to specify that an oscillator start-up delay is imposed upon recovery from STOP mode. The clock monitor system is disabled because CME and FCME are cleared.

10.5 Reset and interrupt priority

Resets and interrupts have a hardware priority that determines which reset or interrupt is serviced first when simultaneous requests occur. Any maskable interrupt can be given priority over other maskable interrupts.

The first six interrupt sources are not maskable by the I-bit in the CCR. The priority arrangement for these sources is fixed and is as follows:

1. POR or $\overline{\text{RESET}}$ pin
2. Clock monitor reset
3. COP watchdog reset
4. $\overline{\text{XIRQ}}$ interrupt
   - Illegal opcode interrupt — see **Illegal opcode trap** for details of handling

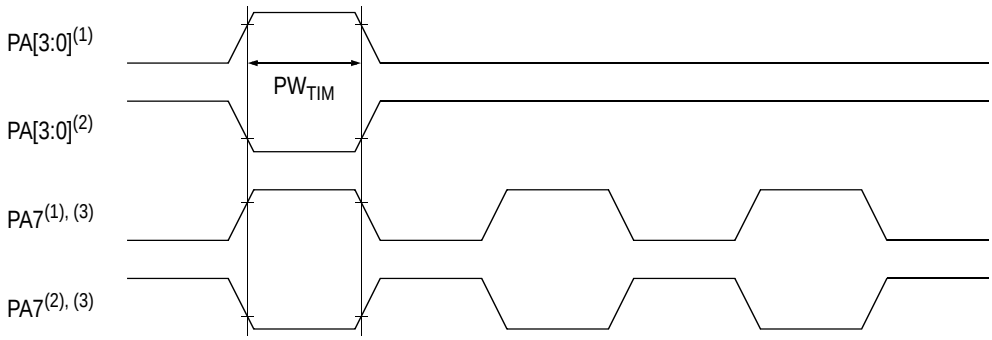
internal oscillator is being used, this delay is required; however, if a stable external oscillator is being used, the DLY control bit can be used to bypass this start-up delay. The DLY control bit is set by reset and can be optionally cleared during initialization. If the DLY equal to zero option is used to avoid start-up delay on recovery from STOP, then reset should not be used as the means of recovering from STOP, as this causes DLY to be set again by reset, imposing the restart delay. This same delay also applies to power-on-reset, regardless of the state of the DLY control bit, but does not apply to a reset while the clocks are running.

12.7 Control timing

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H)

Characteristic (1)	Symbol	2.0MHz		3.0MHz		4.0MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Frequency of operation	f_{OP}	0	2.0	0	3.0	0	4.0	MHz
E clock period	t_{CYC}	500	—	333	—	250	—	ns
Crystal frequency	f_{XTAL}	—	8.0	—	12.0	—	16.0	MHz
External oscillator frequency	$4f_{OP}$	0	8.0	0	12.0	0	16.0	MHz
Processor control set-up time (t_{PCSU} = t_{CYC}/4 + 50ns)	t_{PCSU}	175	—	133	—	112	—	ns
Reset input pulse width (2)	PW_{RSTL} (3) PW_{RSTL} (4)	8 1	— —	8 1	— —	8 1	— —	t_{CYC}
Mode programming set-up time	t_{MPS}	2	—	2	—	2	—	t_{CYC}
Mode programming hold time	t_{MPH}	10	—	10	—	10	—	ns
Interrupt pulse width ($\overline{IRQ}$ edge sensitive mode)	PW_{IRQ}	t_{CYC} +20	—	t_{CYC} +20	—	t_{CYC} +20	—	ns
Timer pulse width (Input capture and pulse accumulator inputs)	PW_{TIM}	t_{CYC} +20	—	t_{CYC} +20	—	t_{CYC} +20	—	ns
WAIT recovery start-up time	t_{WRS}	—	4	—	4	—	4	t_{CYC}
Clock monitor reset	f_{CMON}	10	200	10	200	10	200	kHz
PLL crystal frequency	f_{XTAL}	—	2.0	—	2.0	—	2.0	MHz
PLL stabilization time	t_{PLLS}	—	TBD	—	TBD	—	TBD	ms

1. All timing is given with respect to 20% and 70% of V_{DD}, unless otherwise noted.
2. Reset is recognized during the first clock cycle it is held low. Internal circuitry then drives the pin low for four clock cycles, releases the pin and samples the pin level two cycles later to determine the source of the interrupt. (See **Resets and Interrupts**.)
3. To guarantee an external reset vector.
4. This is the minimum input time; it can be pre-empted by an internal reset.



Notes
(1) Rising edge sensitive input.
(2) Falling edge sensitive input.
(3) Maximum pulse accumulator clocking rate is E clock frequency divided by two (E/2).

Section 13. Mechanical Data

13.1 Contents

13.2 Pin assignments 248

13.3 Package dimensions 249

illegal address — An address not within the memory map

illegal opcode — A nonexistent opcode.

I — The interrupt mask bit in the condition code register of the CPU08. When I is set, all interrupts are disabled.

index register (H:X) — A 16-bit register in the CPU08. The upper byte of H:X is called H. The lower byte is called X. In the indexed addressing modes, the CPU uses the contents of H:X to determine the effective address of the operand. H:X can also serve as a temporary data storage location.

input/output (I/O) — Input/output interfaces between a computer system and the external world. A CPU reads an input to sense the level of an external signal and writes to an output to change the level on an external signal.

instructions — Operations that a CPU can perform. Instructions are expressed by programmers as assembly language mnemonics. A CPU interprets an opcode and its associated operand(s) and instruction.

interrupt — A temporary break in the sequential execution of a program to respond to signals from peripheral devices by executing a subroutine.

interrupt request — A signal from a peripheral to the CPU intended to cause the CPU to execute a subroutine.

I/O — See “input/output (I/0).”

IRQ — See "external interrupt module (IRQ)."

jitter — Short-term signal instability.

latch — A circuit that retains the voltage level (logic 1 or logic 0) written to it for as long as power is applied to the circuit.

latency — The time lag between instruction completion and data movement.

least significant bit (LSB) — The rightmost digit of a binary number.

logic 1 — A voltage level approximately equal to the input power voltage (V_{DD}).

logic 0 — A voltage level approximately equal to the ground voltage (V_{SS}).

low byte — The least significant eight bits of a word.

low voltage inhibit module (LVI) — A module in the M68HC08 Family that monitors power

Revision History

15.4 Major Changes Between Revision 1.0 and Revision 0.0

The following table lists the major changes between the current revision of the MC68HC11P2 Technical Data Book, Rev 1.0, and the previous revision, Rev 0.0.

Section affected	Page number	Description of change
General Description	19	SCI2 pins TXD2 and RXD2 corrected to PH7 and PH6 SCI3 pins TXD3 and RXD3 corrected to PH5 and PH4
Pin Descriptions	35	
	22	
Parallel Input/Output	82	
Serial Communications Interface (SCI)	104	
Motorola Interconnect Bus (MI BUS)	110	
Mechanical Data	248	
Electrical Specifications	246	Min and max columns added to EPROM Characteristics