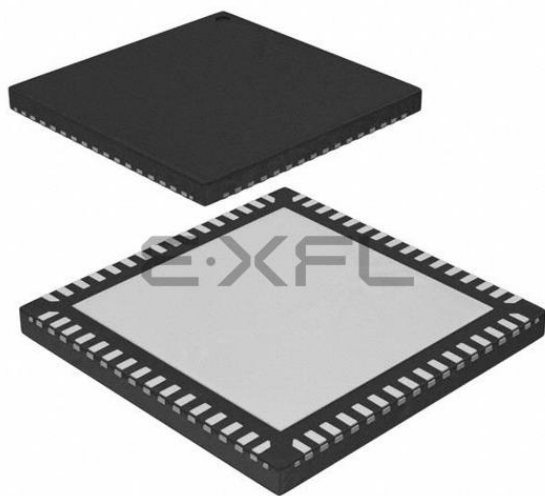




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Details

Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg840f8-qfn64

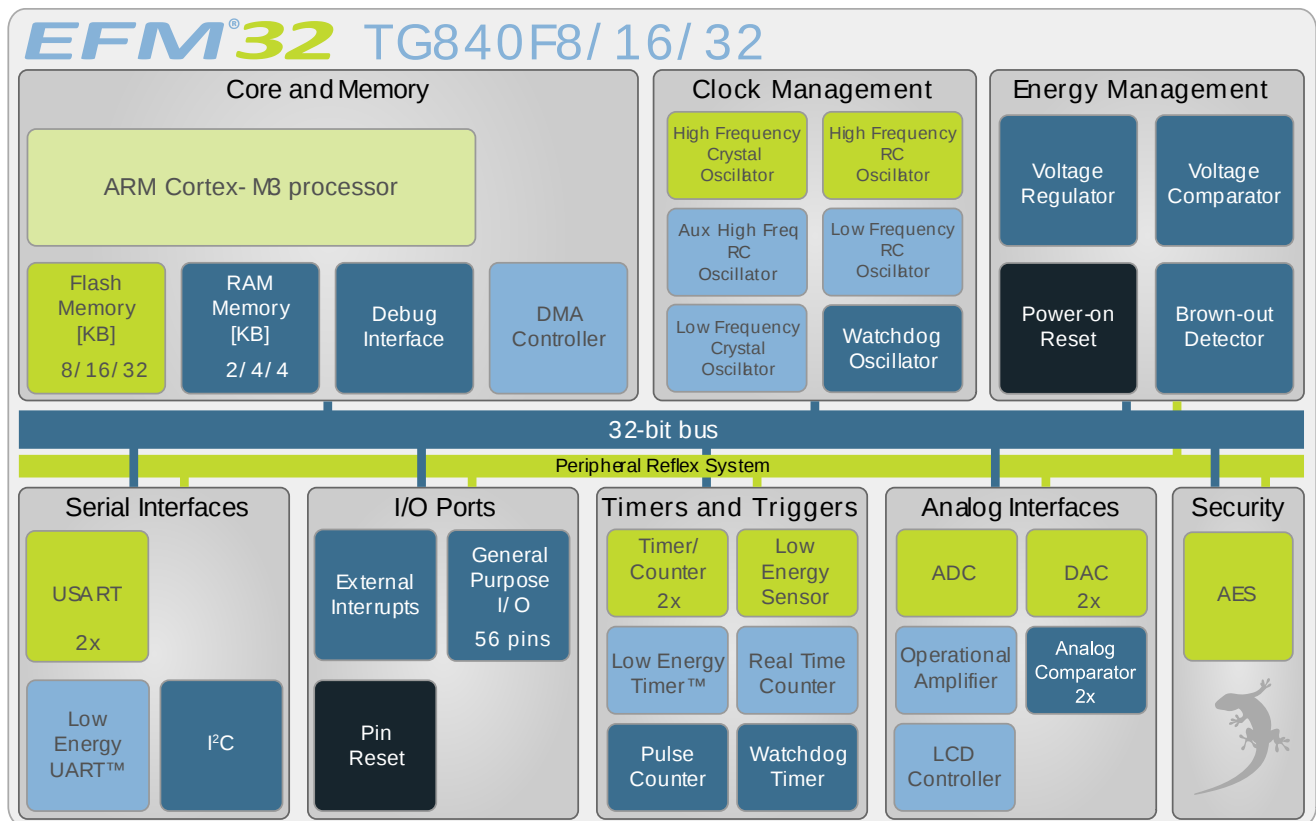
2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32TG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32TG840 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32TG Reference Manual*.

A block diagram of the EFM32TG840 is shown in Figure 2.1 (p. 3) .

Figure 2.1. Block Diagram



2.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep is included as well. The EFM32 implementation of the Cortex-M3 is described in detail in *EFM32 Cortex-M3 Reference Manual*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface . In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32TG microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is

2.1.26 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x20 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

2.2 Configuration Summary

The features of the EFM32TG840 is a subset of the feature set described in the EFM32TG Reference Manual. Table 2.1 (p. 7) describes device specific implementation of the features.

Table 2.1. Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
TIMER0	Full configuration	TIM0_CC[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:4], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:4], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA

3.4 Current Consumption

Table 3.3. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{EM0}	EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	32 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V		157		μA/ MHz
		28 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		150	170	μA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		153	172	μA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		155	175	μA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		157	178	μA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		162	183	μA/ MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		200	240	μA/ MHz
I _{EM1}	EM1 current (Production test condition = 14 MHz)	32 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V		53		μA/ MHz
		28 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		51	57	μA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		55	59	μA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		56	61	μA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		58	63	μA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		63	68	μA/ MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V _{DD} = 3.0 V		100	122	μA/ MHz
I _{EM2}	EM2 current	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V _{DD} = 3.0 V, T _{AMB} =25°C		1.0	1.2	μA
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V _{DD} = 3.0 V, T _{AMB} =85°C		2.4	5.0	μA
I _{EM3}	EM3 current	V _{DD} = 3.0 V, T _{AMB} =25°C		0.59	1.0	μA
		V _{DD} = 3.0 V, T _{AMB} =85°C		2.0	4.5	μA
I _{EM4}	EM4 current	V _{DD} = 3.0 V, T _{AMB} =25°C		0.02	0.055	μA
		V _{DD} = 3.0 V, T _{AMB} =85°C		0.25	0.70	μA

3.7 Flash

Table 3.6. Flash

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC _{FLASH}	Flash erase cycles before failure		20000			cycles
RET _{FLASH}	Flash data retention	T _{AMB} <150°C	10000			h
		T _{AMB} <85°C	10			years
		T _{AMB} <70°C	20			years
t _{W_PROG}	Word (32-bit) programming time		20			µs
t _{P_ERASE}	Page erase time		20	20.4	20.8	ms
t _{D_ERASE}	Device erase time		40	40.8	41.6	ms
I _{ERASE}	Erase current				7 ¹	mA
I _{WRITE}	Write current				7 ¹	mA
V _{FLASH}	Supply voltage during flash erase and write		1.98		3.8	V

¹Measured at 25°C

3.8 General Purpose Input Output

Table 3.7. GPIO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{IOIL}	Input low voltage				0.30V _{DD}	V
V _{IOIH}	Input high voltage		0.70V _{DD}			V
V _{IOOH}	Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sourcing 0.1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.80V _{DD}		V
		Sourcing 0.1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.90V _{DD}		V
		Sourcing 1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.85V _{DD}		V
		Sourcing 1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.90V _{DD}		V
		Sourcing 6 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.75V _{DD}			V
		Sourcing 6 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.85V _{DD}			V
		Sourcing 20 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.60V _{DD}			V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		$f_{\text{HFRCO}} = 14 \text{ MHz}$		104	120	μA
		$f_{\text{HFRCO}} = 11 \text{ MHz}$		94	110	μA
		$f_{\text{HFRCO}} = 6.6 \text{ MHz}$		63	90	μA
		$f_{\text{HFRCO}} = 1.2 \text{ MHz}$		22	32	μA
TUNESTEP _{H-FRCO}	Frequency step for LSB change in TUNING value			0.3 ³		%

¹For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

²For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

³The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

Figure 3.11. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature

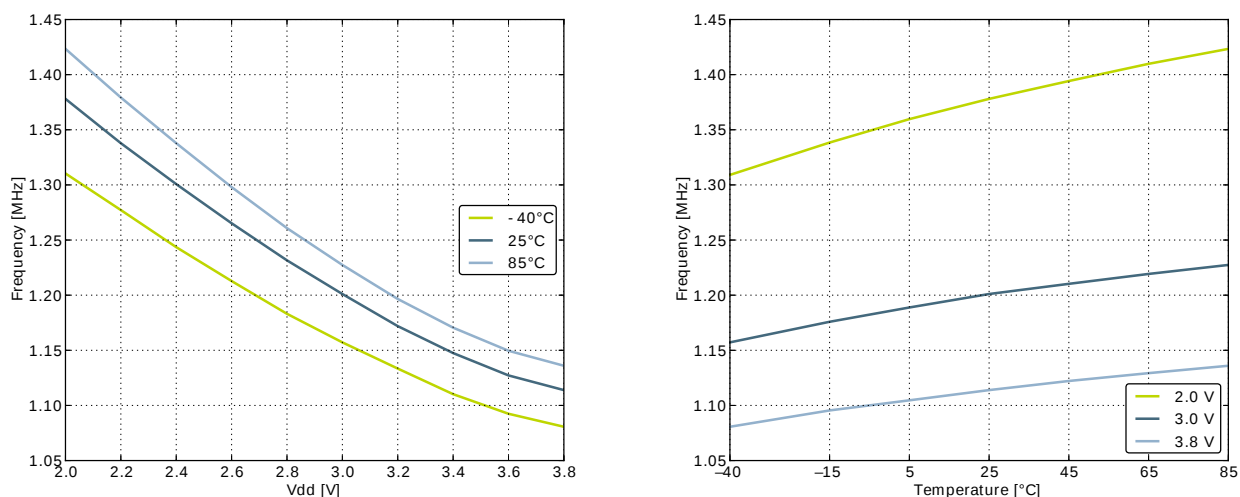


Figure 3.12. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature

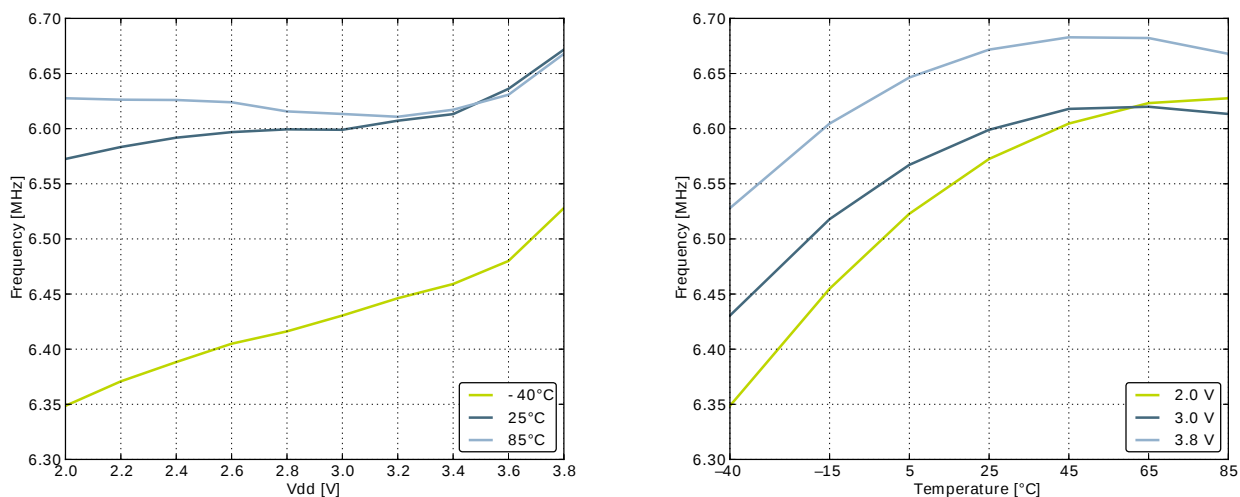
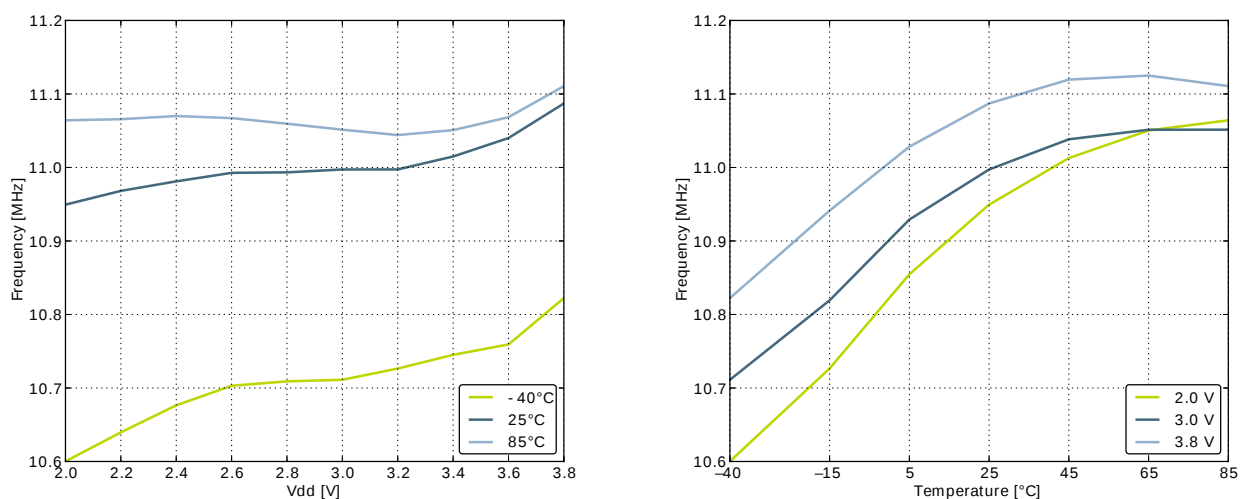
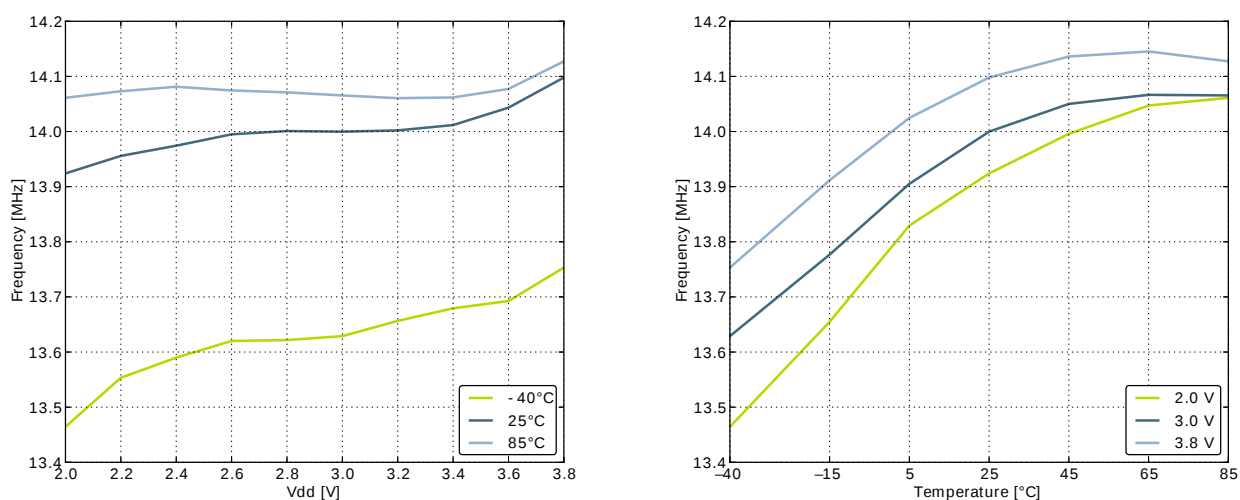
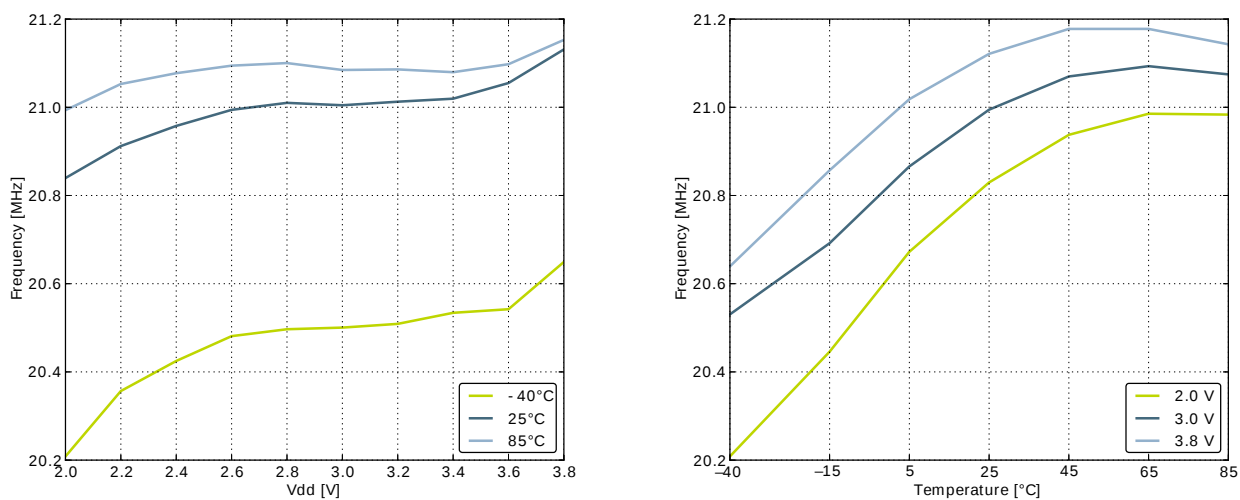
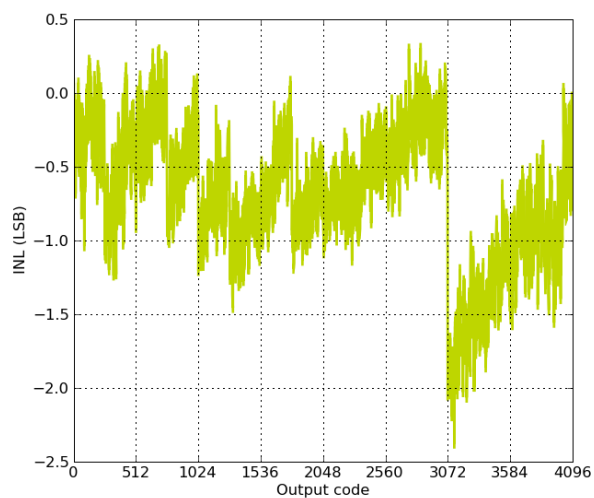
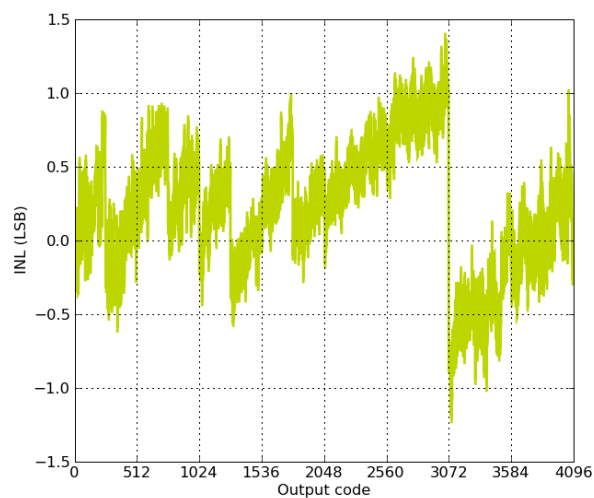
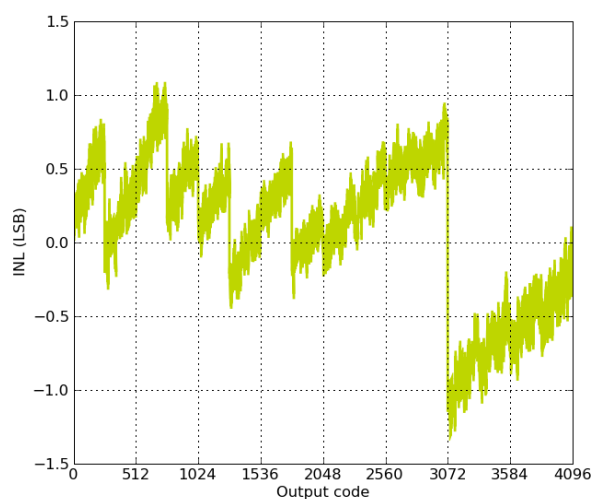
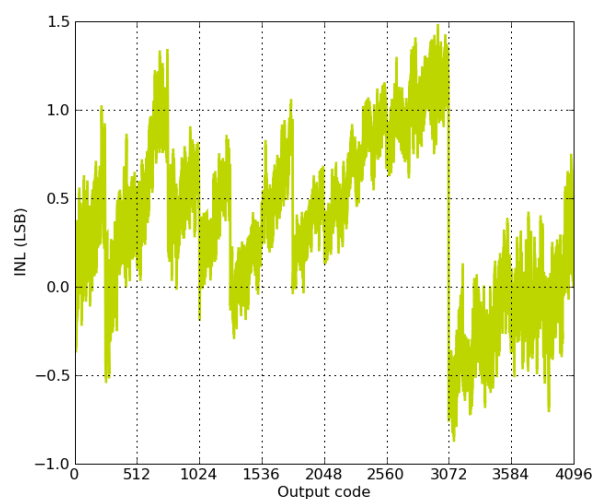
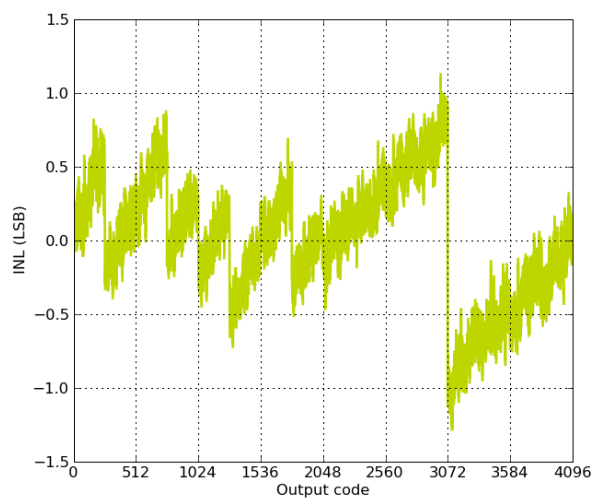


Figure 3.13. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature**Figure 3.14. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature****Figure 3.15. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{ADCCLK}	ADC Clock Frequency				13	MHz
t_{ADCCONV}	Conversion time	6 bit	7			ADC-CLK Cycles
		8 bit	11			ADC-CLK Cycles
		12 bit	13			ADC-CLK Cycles
t_{ADCACQ}	Acquisition time	Programmable	1		256	ADC-CLK Cycles
$t_{\text{ADCACQVDD3}}$	Required acquisition time for VDD/3 reference		2			μs
t_{ADCSTART}	Startup time of reference generator and ADC core in NORMAL mode			5		μs
	Startup time of reference generator and ADC core in KEEPADCWARM mode			1		μs
SNR_{ADC}	Signal to Noise Ratio (SNR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		59		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		65		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		65		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		67		dB
		1 MSamples/s, 12 bit, differential, $2 \times V_{\text{DD}}$ reference		69		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		62		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference	63	67		dB

Figure 3.20. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C**1.25V Reference****2.5V Reference****2XVDDVSS Reference****5VDIFF Reference****VDD Reference**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		RESSEL=7, 0.1 Hz<f<1 MHz, OPAxHCMDIS=1		2590		μV _{RMS}

Figure 3.24. OPAMP Common Mode Rejection Ratio

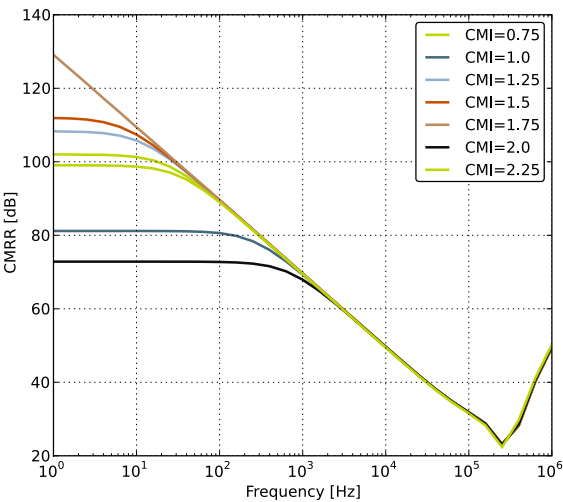
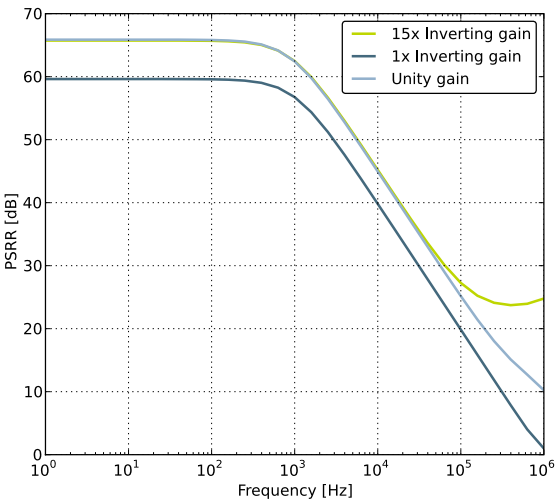


Figure 3.25. OPAMP Positive Power Supply Rejection Ratio



3.14 Voltage Comparator (VCMP)

Table 3.18. VCMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{VCMPIN}	Input voltage range			V _{DD}		V
V _{VCMP_{CM}}	VCMP Common Mode voltage range			V _{DD}		V
I _{VCMP}	Active current	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register		0.3	0.6	μA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0.		22	30	μA
t _{VCMPREF}	Startup time reference generator	NORMAL		10		μs
V _{VCMP_{OFFSET}}	Offset voltage	Single ended		10		mV
		Differential		10		mV
V _{VCMPHYST}	VCMP hysteresis			17		mV
t _{VCMPSTART}	Startup time				10	μs

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

VCMP Trigger Level as a Function of Level Setting

$$V_{DD} \text{ Trigger Level} = 1.667V + 0.034 \times \text{TRIGLEVEL} \quad (3.2)$$

3.16 I2C

Table 3.20. I2C Standard-mode (Sm)

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	0		100 ¹	kHz
t _{LOW}	SCL clock low time	4.7			μs
t _{HIGH}	SCL clock high time	4.0			μs
t _{SU,DAT}	SDA set-up time	250			ns
t _{HD,DAT}	SDA hold time	8		3450 ^{2,3}	ns
t _{SU,STA}	Repeated START condition set-up time	4.7			μs
t _{HD,STA}	(Repeated) START condition hold time	4.0			μs
t _{SU,STO}	STOP condition set-up time	4.0			μs
t _{BUF}	Bus free time between a STOP and START condition	4.7			μs

¹For the minimum HPPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32TG Reference Manual.

²The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

³When transmitting data, this number is guaranteed only when $I2Cn_CLKDIV < ((3450 \cdot 10^{-9} [s] \cdot f_{HPPERCLK} [Hz]) - 4)$.

Table 3.21. I2C Fast-mode (Fm)

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	0		400 ¹	kHz
t _{LOW}	SCL clock low time	1.3			μs
t _{HIGH}	SCL clock high time	0.6			μs
t _{SU,DAT}	SDA set-up time	100			ns
t _{HD,DAT}	SDA hold time	8		900 ^{2,3}	ns
t _{SU,STA}	Repeated START condition set-up time	0.6			μs
t _{HD,STA}	(Repeated) START condition hold time	0.6			μs
t _{SU,STO}	STOP condition set-up time	0.6			μs
t _{BUF}	Bus free time between a STOP and START condition	1.3			μs

¹For the minimum HPPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32TG Reference Manual.

²The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

³When transmitting data, this number is guaranteed only when $I2Cn_CLKDIV < ((900 \cdot 10^{-9} [s] \cdot f_{HPPERCLK} [Hz]) - 4)$.

4 Pinout and Package

Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32TG840.

4.1 Pinout

The *EFM32TG840* pinout is shown in Figure 4.1 (p. 46) and Table 4.1 (p. 46). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 4.1. EFM32TG840 Pinout (top view, not to scale)

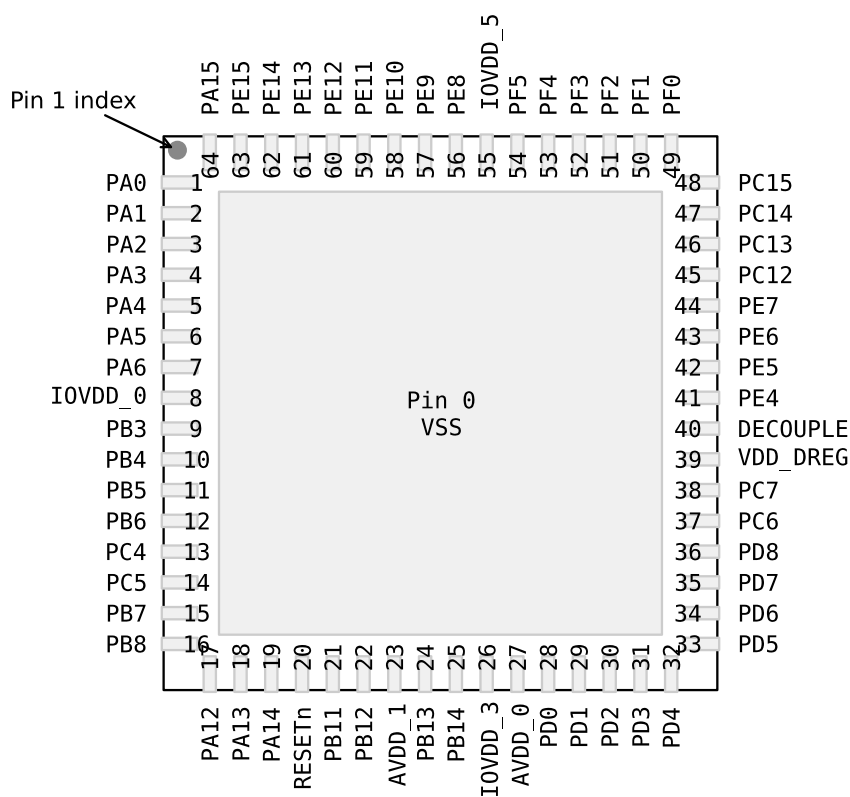
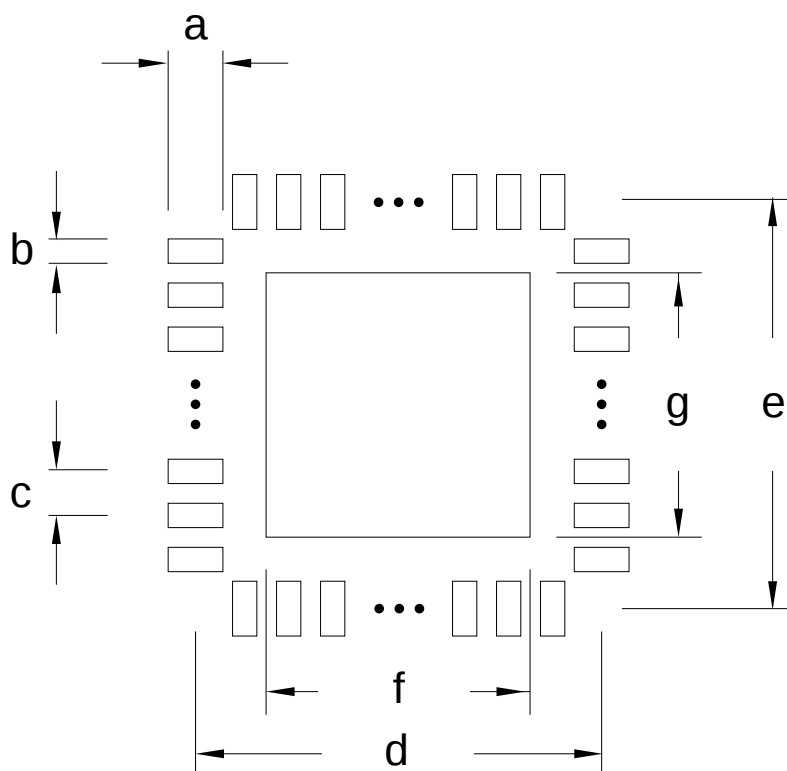


Table 4.1. Device Pinout

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	PA0	LCD_SEG13	TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
2	PA1	LCD_SEG14	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
		OPAMP_N2			
32	PD4	ADC0_CH4 OPAMP_P2		LEU0_TX #0	
33	PD5	ADC0_CH5 OPAMP_OUT2 #0		LEU0_RX #0	
34	PD6	ADC0_CH6 DAC0_P1 / OPAMP_P1	TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2
35	PD7	ADC0_CH7 DAC0_N1 / OPAMP_N1	TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2
36	PD8				CMU_CLK1 #1
37	PC6	ACMP0_CH6		I2C0_SDA #2	LES_CH6 #0
38	PC7	ACMP0_CH7		I2C0_SCL #2	LES_CH7 #0
39	VDD_DREG	Power supply for on-chip voltage regulator.			
40	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.			
41	PE4	LCD_COM0		US0_CS #1	
42	PE5	LCD_COM1		US0_CLK #1	
43	PE6	LCD_COM2		US0_RX #1	
44	PE7	LCD_COM3		US0_TX #1	
45	PC12	ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT			CMU_CLK0 #1 LES_CH12 #0
46	PC13	ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT	TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0		LES_CH13 #0
47	PC14	ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT	TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3	LES_CH14 #0
48	PC15	ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT	TIM1_CC2 #0	US0_CLK #3	LES_CH15 #0 DBG_SWO #1
49	PF0		TIM0_CC0 #5 LETIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1
50	PF1		TIM0_CC1 #5 LETIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1 GPIO_EM4WU3
51	PF2	LCD_SEG0	TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
52	PF3	LCD_SEG1			PRS_CH0 #1
53	PF4	LCD_SEG2			PRS_CH1 #1
54	PF5	LCD_SEG3			PRS_CH2 #1
55	IOVDD_5	Digital IO power supply 5.			
56	PE8	LCD_SEG4			PRS_CH3 #1
57	PE9	LCD_SEG5			
58	PE10	LCD_SEG6	TIM1_CC0 #1	US0_TX #0	BOOT_TX
59	PE11	LCD_SEG7	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
CMU_CLK0	PA2	PC12	PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8	PE12					Clock Management Unit, clock output number 1.
DAC0_N0 / OPAMP_N0	PC5							Operational Amplifier 0 external negative input.
DAC0_N1 / OPAMP_N1	PD7							Operational Amplifier 1 external negative input.
OPAMP_N2	PD3							Operational Amplifier 2 external negative input.
DAC0_OUT0 / OPAMP_OUT0	PB11							Digital to Analog Converter DAC0_OUT0 / OPAMP output channel number 0.
DAC0_OUT0ALT / OPAMP_OUT0ALT					PD0			Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0.
DAC0_OUT1 / OPAMP_OUT1	PB12							Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1.
DAC0_OUT1ALT / OPAMP_OUT1ALT	PC12	PC13	PC14	PC15	PD1			Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1.
OPAMP_OUT2	PD5	PD0						Operational Amplifier 2 output.
DAC0_P0 / OPAMP_P0	PC4							Operational Amplifier 0 external positive input.
DAC0_P1 / OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
OPAMP_P2	PD4							Operational Amplifier 2 external positive input.
DBG_SWCLK	PF0	PF0						Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1						Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15						Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7			PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6			PF0	PE12	I2C0 Serial Data input / output.
LCD_BCAP_N	PA13							LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12							LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14							LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled.

Figure 5.2. QFN64 PCB Solder Mask**Table 5.2. QFN64 PCB Solder Mask Dimensions (Dimensions in mm)**

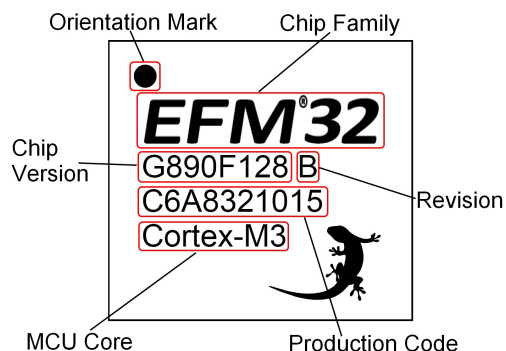
Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.97	e	8.90
b	0.42	f	7.32
c	0.50	g	7.32
d	8.90	-	-

6 Chip Marking, Revision and Errata

6.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 6.1. Example Chip Marking (top view)



6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 59) .

6.3 Errata

Please see the errata document for EFM32TG840 for description and resolution of device erratas. This document is available in Simplicity Studio and online at:

<http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit>

Added rising POR level and corrected Thermometer output gradient in Electrical Characteristics section.

Updated Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup.

Added Gain error drift and Offset error drift to ADC table.

Added reference to errata document.

7.9 Revision 0.92

July 22nd, 2011

Updated current consumption numbers from latest device characterization data.

Updated OPAMP electrical characteristics.

Made ADC plots render properly in Adobe Reader.

7.10 Revision 0.91

February 4th, 2011

Corrected max DAC sampling rate.

Increased max storage temperature.

Added data for <150°C and <70°C on Flash data retention.

Changed latch-up sensitivity test description.

Added IO leakage current.

Added Flash current consumption.

Updated HFRCO data.

Updated LFRCO data.

Added graph for ADC Absolute Offset over temperature.

Added graph for ADC Temperature sensor readout.

Updated OPAMP electrical characteristics.

7.11 Revision 0.90

December 1st, 2010

New peripherals added to pinout, including LESENSE and OpAmps.

7.12 Revision 0.50

May 25th, 2010

Block diagram update.

7.13 Revision 0.40

March 26th, 2010

B Contact Information

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Please visit the Silicon Labs Technical Support web page:

<http://www.silabs.com/support/pages/contacttechnicalsupport.aspx>

and register to submit a technical support request.

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