Infineon Technologies - SAF-XC164SM-16F20F BA Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	20MHz
Connectivity	SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	47
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 14x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc164sm-16f20f-ba

XC164SM

16-Bit Single-Chip Microcontroller with C166SV2 Core

Microcontrollers

Never stop thinking

2 General Device Information

The XC164SM derivatives are high-performance members of the Infineon XC166 Family of full featured single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 40 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. They also provide clock generation via PLL and various on-chip memory modules such as program Flash, program RAM, and data RAM.

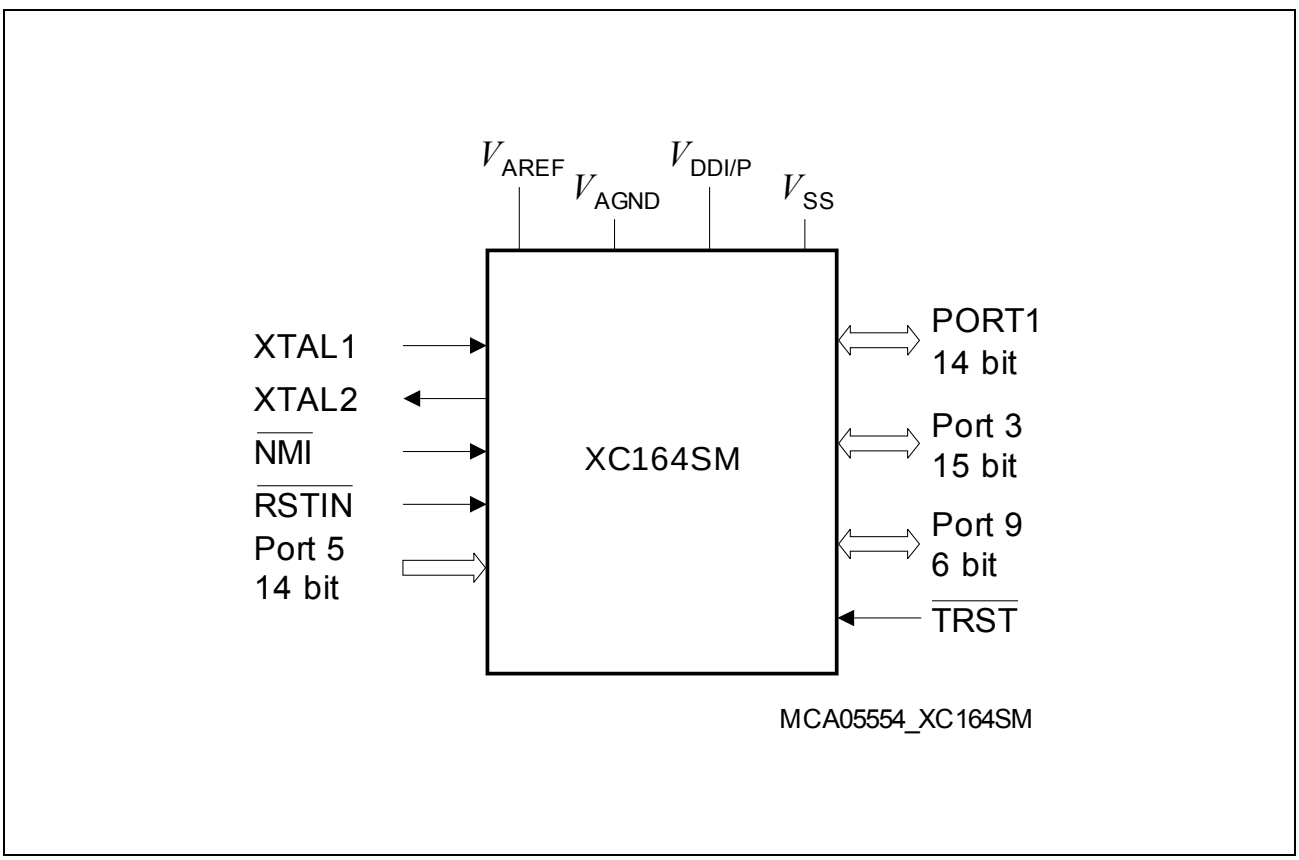

Figure 1 Logic Symbol

Table 1 XC164SM Derivative Synopsis

Derivative [1]	Temp. Range	Program Memory	On-Chip RAM	Interfaces
SAF-XC164SM-16F40F SAF-XC164SM-16F20F	-40 to 85 °C	128 Kbytes Flash	2 Kbytes DPRAM, 4 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1
SAF-XC164SM-8F40F SAF-XC164SM-8F20F	-40 to 85 °C	64 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1
SAF-XC164SM-4F40F SAF-XC164SM-4F20F	-40 to 85 °C	32 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1

1) This Data Sheet is valid for:
devices starting with and including design step BA for the -16F derivatives, and for
devices starting with and including design step AA for -4F/8F derivatives.

2 General Device Information

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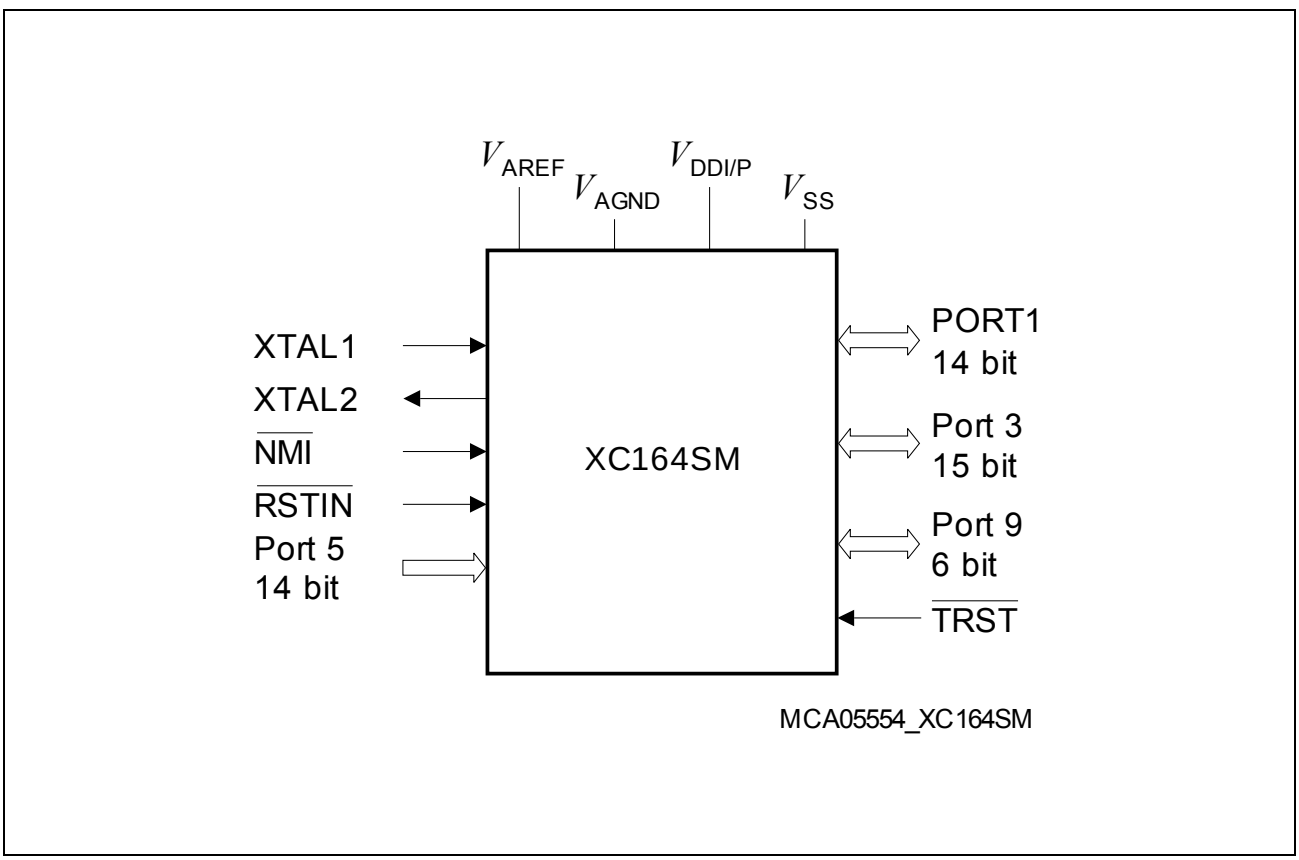

Figure 1 Logic Symbol

2.1 Pin Configuration and Definition

The pins of the XC164SM are described in detail in Table 2, including all their alternate functions. Figure 2 summarizes all pins in a condensed way, showing their location on the 4 sides of the package. E* marks pins to be used as alternate external interrupt inputs.

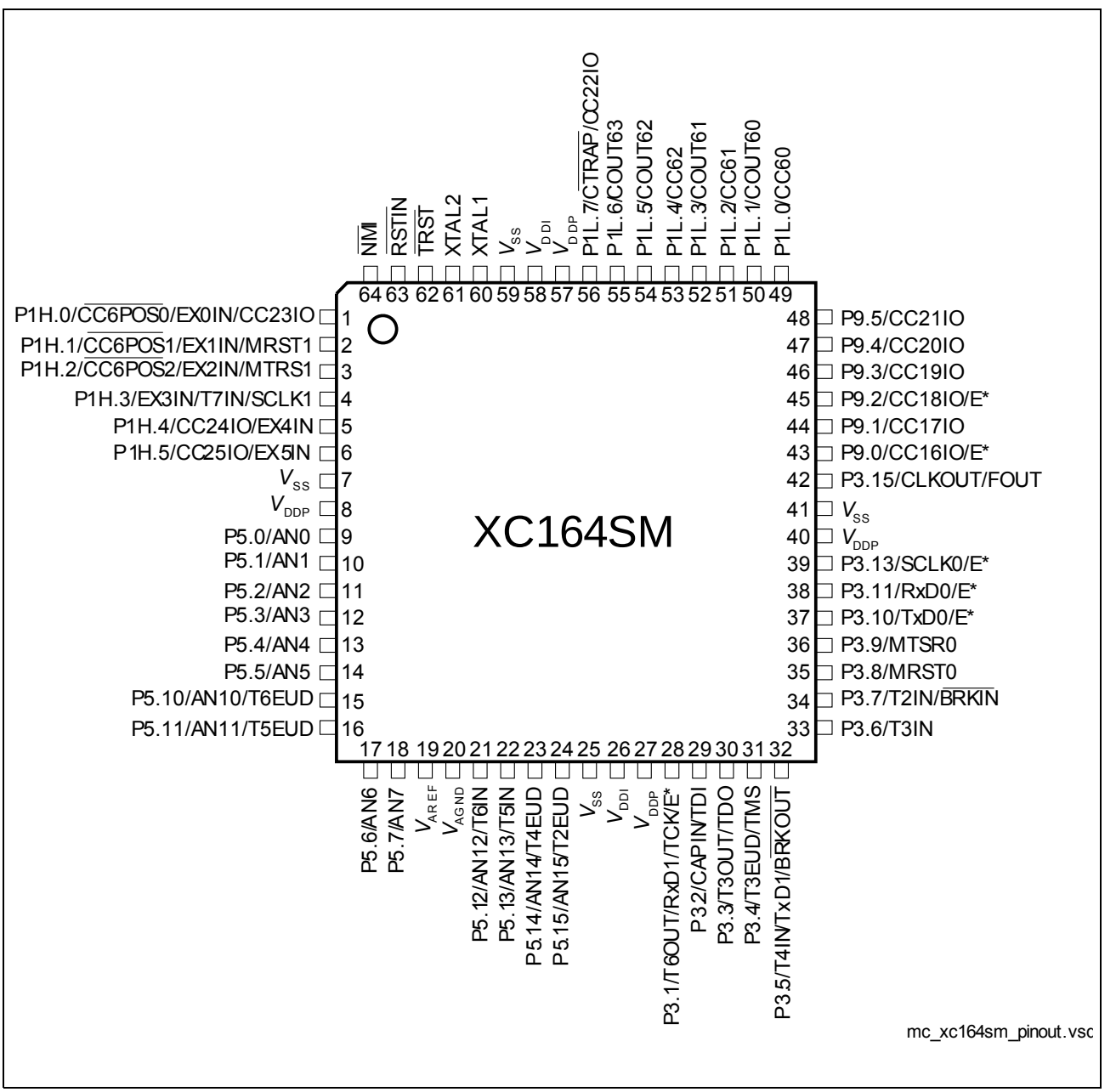

Figure 2 Pin Configuration (top view)

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
PORT1	1-6, 49-56	IO	PORT1 consists of one 8-bit and one 6-bit bidirectional I/O port P1L and P1H. Each pin can be programmed for input (output driver in high-impedance state) or output. The following PORT1 pins also serve for alt. functions:
P1L.0	49	I/O	CC60: [CAPCOM6] Input / Output of Channel 0
P1L.1	50	O	COUT60: [CAPCOM6] Output of Channel 0
P1L.2	51	I/O	CC61: [CAPCOM6] Input / Output of Channel 1
P1L.3	52	O	COUT61: [CAPCOM6] Output of Channel 1
P1L.4	53	I/O	CC62: [CAPCOM6] Input / Output of Channel 2
P1L.5	54	O	COUT62: [CAPCOM6] Output of Channel 2
P1L.6	55	O	COUT63: Output of 10-bit Compare Channel
P1L.7	56	I	CTRAP: [CAPCOM6] Trap Input CTRAP is an input pin with an internal pull-up resistor. A low level on this pin switches the CAPCOM6 compare outputs to the logic level defined by software (if enabled).
		I/O	CC22IO: [CAPCOM2] CC22 Capture Inp./Compare Outp.
P1H.0	1	I	CC6POS0: [CAPCOM6] Position 0 Input,
		I	EX0IN: [Fast External Interrupt 0] Input (default pin),
		I/O	CC23IO: [CAPCOM2] CC23 Capture Inp./Compare Outp.
P1H.1	2	I	CC6POS1: [CAPCOM6] Position 1 Input,
		I	EX1IN: [Fast External Interrupt 1] Input (default pin),
		I/O	MRST1: [SSC1] Master-Receive/Slave-Transmit In/Out.
P1H.2	3	I	CC6POS2: [CAPCOM6] Position 2 Input,
		I	EX2IN: [Fast External Interrupt 2] Input (default pin),
		I/O	MTSR1: [SSC1] Master-Transmit/Slave-Receive Out/Inp.
P1H.3	3	I	T7IN: [CAPCOM2] Timer T7 Count Input,
		I/O	SCLK1: [SSC1] Master Clock Output / Slave Clock Input,
		I	EX3IN: [Fast External Interrupt 3] Input (default pin),
P1H.4	5	I/O	CC24IO: [CAPCOM2] CC24 Capture Inp./Compare Outp.,
		I	EX4IN: [Fast External Interrupt 4] Input (default pin)
P1H.5	6	I/O	CC25IO: [CAPCOM2] CC25 Capture Inp./Compare Outp.,
		I	EX5IN: [Fast External Interrupt 5] Input (default pin)
			Note: At the end of an external reset P1H.4 and P1H.5 also may input startup configuration values

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
XTAL2 XTAL1	61 60	O I	XTAL2: Output of the oscillator amplifier circuit XTAL1: Input to the oscillator amplifier and input to the internal clock generator To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed. *Note: Input pin XTAL1 belongs to the core voltage domain. Therefore, input voltages must be within the range defined for V_{DDI}.*
V_{AREF}	19	–	Reference voltage for the A/D converter
V_{AGND}	20	–	Reference ground for the A/D converter
V_{DDI}	26, 58	–	Digital Core Supply Voltage (On-Chip Modules): +2.5 V during normal operation and idle mode. Please refer to the Operating Condition Parameters
V_{DDP}	8, 27, 40, 57	–	Digital Pad Supply Voltage (Pin Output Drivers): +5 V during normal operation and idle mode. Please refer to the Operating Condition Parameters
V_{SS}	7, 25, 41, 59	–	Digital Ground Connect decoupling capacitors to adjacent V_{DD}/V_{SS} pin pairs as close as possible to the pins. All V_{SS} pins must be connected to the ground-line or ground-plane.

can consist of up to 16 word wide (R0 to R15) and/or byte wide (RL0, RH0, …, RL7, RH7) so-called General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word wide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XC166 Family. Therefore, they should either not be accessed, or written with zeros, to ensure upward compatibility.

Table 3 XC164SM Memory Map

Address Area	Start Loc.	End Loc.	Area Size [1]	Notes
Flash register space	FF'F000$_H$	FF'FFFF$_H$	4 Kbytes	[2]
Reserved (Acc. trap)	F8'0000$_H$	FF'FFFF$_H$	508 Kbytes	–
Reserved for PSRAM	E0'0800$_H$	F7'FFFF$_H$	< 1.5 Mbytes	Minus PSRAM
Program SRAM	E0'0000$_H$	E0'07FF$_H$	2 Kbytes	–
Reserved for pr. mem.	C2'0000$_H$	DF'FFFF$_H$	< 2 Mbytes	Minus Flash
Program Flash	C0'0000$_H$	C1'FFFF$_H$	128 Kbytes	XC164SM-16F
	C0'0000$_H$	C0'FFFF$_H$	64 Kbytes	XC164SM-8F
	C0'0000$_H$	C0'7FFF$_H$	32 Kbytes	XC164SM-4F
Reserved	20'0000$_H$	BF'FFFF$_H$	< 10 Mbytes	
Reserved	01'0000$_H$	1F'FFFF$_H$	< 2 Mbytes	Minus segment 0
SFR area	00'FE00$_H$	00'FFFF$_H$	0.5 Kbyte	–
Dual-Port RAM	00'F600$_H$	00'FDFF$_H$	2 Kbytes	–
Reserved for DPRAM	00'F200$_H$	00'F5FF$_H$	1 Kbyte	–
ESFR area	00'F000$_H$	00'F1FF$_H$	0.5 Kbyte	–
XSFR area	00'E000$_H$	00'EFFF$_H$	4 Kbytes	–
Reserved	00'D000$_H$	00'DFFF$_H$	6 Kbytes	–
Data SRAM	00'C000$_H$	00'CFFF$_H$	4 Kbytes	[3]
Reserved for DSRAM	00'8000$_H$	00'BFFF$_H$	16 Kbytes	–
Reserved	00'0000$_H$	00'7FFF$_H$	32 Kbytes	–

1) The areas marked with "<" are slightly smaller than indicated, see column "Notes".

2) Not defined register locations return a trap code (1E9B$_H$).

3) Depends on the respective derivative. See Table 1 "XC164SM Derivative Synopsis" on Page 6 .

3.2 Central Processing Unit (CPU)

The main core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply and divide unit, a bit-mask generator, and a barrel shifter.

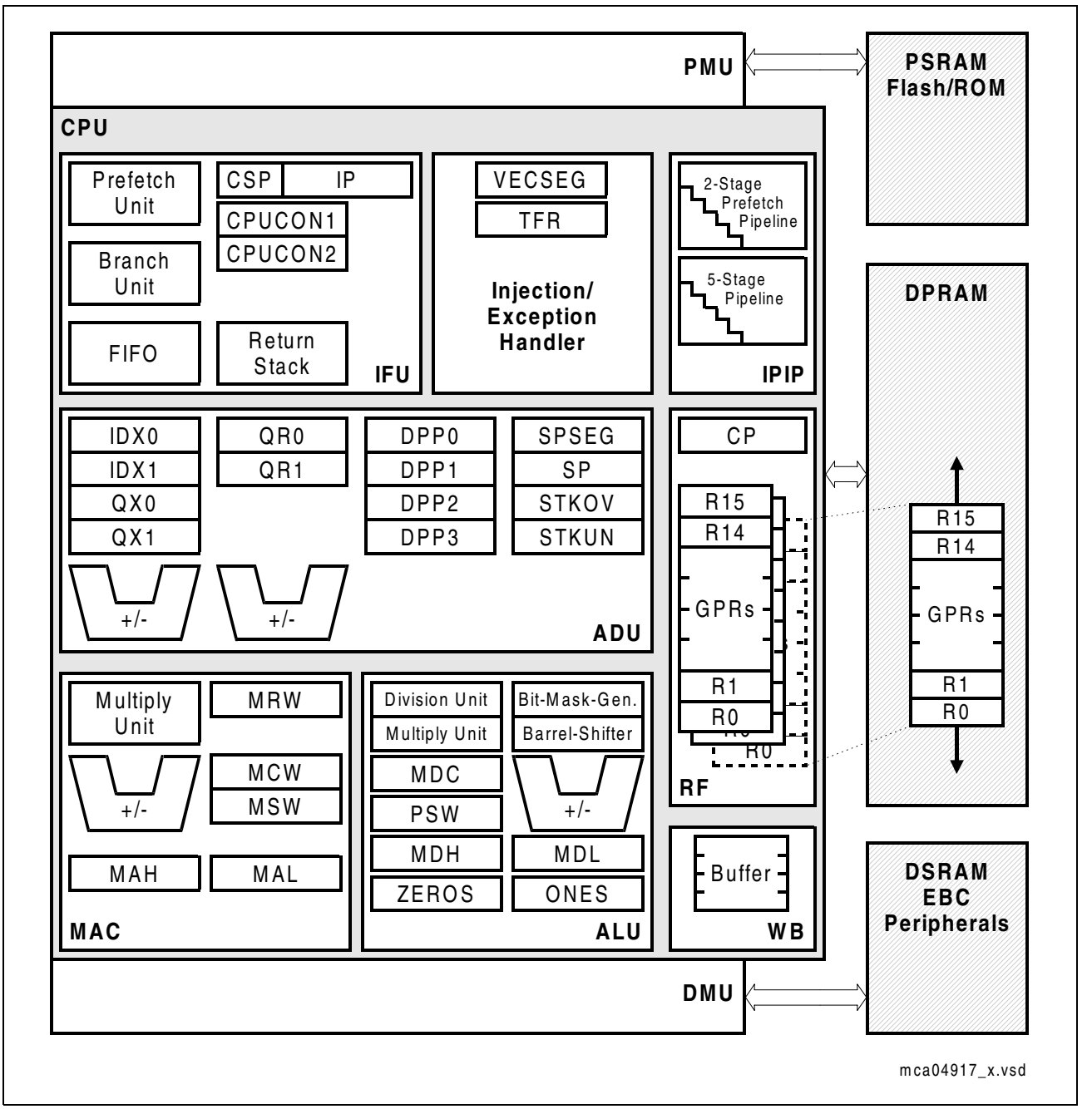

Figure 4 CPU Block Diagram

Based on these hardware provisions, most of the XC164SM's instructions can be executed in just one machine cycle which requires 25 ns at 40 MHz CPU clock. For

3.3 Interrupt System

With an interrupt response time of typically 8 CPU clocks (in case of internal program execution), the XC164SM is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the XC164SM supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source, or the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The XC164SM has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bit field exists for each of the possible interrupt nodes. Via its related register, each node can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt nodes has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge, or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

Table 4 shows all of the possible XC164SM interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not assigned to peripherals (unassigned nodes), may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

Table 4 XC164SM Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location [1]	Trap Number
Unassigned node	–	xx'0050$_H$	14$_H$ / 20$_D$
Unassigned node	–	xx'0054$_H$	15$_H$ / 21$_D$
Unassigned node	–	xx'0058$_H$	16$_H$ / 22$_D$
Unassigned node	–	xx'005C$_H$	17$_H$ / 23$_D$
Unassigned node	–	xx'0078$_H$	1E$_H$ / 30$_D$
Unassigned node	–	xx'007C$_H$	1F$_H$ / 31$_D$
Unassigned node	–	xx'0080$_H$	20$_H$ / 32$_D$
Unassigned node	–	xx'0084$_H$	21$_H$ / 33$_D$
Unassigned node	–	xx'00FC$_H$	3F$_H$ / 63$_D$
Unassigned node	–	xx'0100$_H$	40$_H$ / 64$_D$
Unassigned node	–	xx'0104$_H$	41$_H$ / 65$_D$
Unassigned node	–	xx'012C$_H$	4B$_H$ / 75$_D$
Unassigned node	–	xx'0150$_H$	54$_H$ / 84$_D$
Unassigned node	–	xx'0154$_H$	55$_H$ / 85$_D$
Unassigned node	–	xx'0158$_H$	56$_H$ / 86$_D$
Unassigned node	–	xx'015C$_H$	57$_H$ / 87$_D$
Unassigned node	–	xx'0160$_H$	58$_H$ / 88$_D$
Unassigned node	–	xx'0164$_H$	59$_H$ / 89$_D$
Unassigned node	–	xx'0168$_H$	5A$_H$ / 90$_D$
Unassigned node	–	xx'016C$_H$	5B$_H$ / 91$_D$
Unassigned node	–	xx'0170$_H$	5C$_H$ / 92$_D$

1) Register VECSEG defines the segment where the vector table is located to.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.