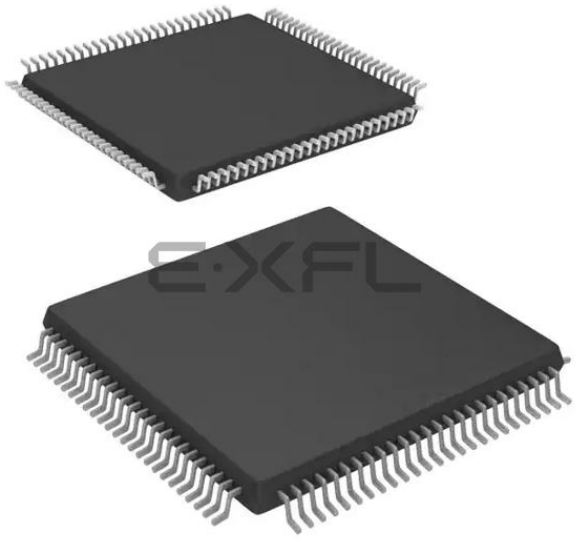

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300
Core Size	8-Bit
Speed	16MHz
Connectivity	Host Interface, I²C, SCI
Peripherals	POR, PWM, WDT
Number of I/O	74
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f3437stf16v

General Precautions on Handling of Product

1. Treatment of NC Pins

Note: Do not connect anything to the NC pins.
The NC (not connected) pins are either not connected to any of the internal circuitry or are they are used as test pins or to reduce noise. If something is connected to the NC pins, the operation of the LSI is not guaranteed.

2. Treatment of Unused Input Pins

Note: Fix all unused input pins to high or low level.
Generally, the input pins of CMOS products are high-impedance input pins. If unused pins are in their open states, intermediate levels are induced by noise in the vicinity, a pass-through current flows internally, and a malfunction may occur.

3. Processing before Initialization

Note: When power is first supplied, the product's state is undefined.
The states of internal circuits are undefined until full power is supplied throughout the chip and a low level is input on the reset pin. During the period where the states are undefined, the register settings and the output state of each pin are also undefined. Design your system so that it does not malfunction because of processing while it is in this undefined state. For those products which have a reset function, reset the LSI immediately after the power supply has been turned on.

4. Prohibition of Access to Undefined or Reserved Addresses

Note: Access to undefined or reserved addresses is prohibited.
The undefined or reserved addresses may be used to expand functions, or test registers may have been be allocated to these addresses. Do not access these registers; the system's operation is not guaranteed if they are accessed.

4.3.2 Interrupt-Related Registers

The interrupt-related registers are the system control register (SYSCR), IRQ sense control register (ISCR), IRQ enable register (IER), and keyboard matrix interrupt mask registers (KMIMR and KMIMRA).

Table 4.3 Registers Read by Interrupt Controller

Name	Abbreviation	Read/Write	Address
System control register	SYSCR	R/W	H'FFC4
IRQ sense control register	ISCR	R/W	H'FFC6
IRQ enable register	IER	R/W	H'FFC7
Keyboard matrix interrupt mask register	KMIMR	R/W	H'FFF1
Keyboard matrix interrupt mask register A	KMIMRA	R/W	H'FFF3

System Control Register (SYSCR)

Bit	7	6	5	4	3	2	1	0
	SSBY	STS2	STS1	STS0	XRST	NMIEG	HIE	RAME
Initial value	0	0	0	0	1	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

The valid edge on the $\overline{\text{NMI}}$ line is controlled by bit 2 (NMIEG) in the system control register.

Bit 2—NMI Edge (NMIEG): Determines whether a nonmaskable interrupt is generated on the falling or rising edge of the $\overline{\text{NMI}}$ input signal.

Bit 2: NMIEG	Description
0	An interrupt is generated on the falling edge of $\overline{\text{NMI}}$. (Initial state)
1	An interrupt is generated on the rising edge of $\overline{\text{NMI}}$.

See section 3.2, System Control Register, for information on the other SYSCR bits.

IRQ Sense Control Register (ISCR)

Bit	7	6	5	4	3	2	1	0
	IRQ7SC	IRQ6SC	IRQ5SC	IRQ4SC	IRQ3SC	IRQ2SC	IRQ1SC	IRQ0SC
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7.3.4 Input Pull-Up Transistors

Port 2 has built-in programmable input pull-up transistors that are available in modes 2 and 3. The pull-up for each bit can be turned on and off individually. To turn on an input pull-up in mode 2 or 3, set the corresponding P2PCR bit to 1 and clear the corresponding P2DDR bit to 0. P2PCR is cleared to H'00 by a reset and in hardware standby mode, turning all input pull-ups off. In software standby mode, the previous state is maintained.

Table 7.5 indicates the states of the input pull-up transistors in each operating mode.

Table 7.5 States of Input Pull-Up Transistors (Port 2)

Mode	Reset	Hardware Standby	Software Standby	Other Operating Modes
1	Off	Off	Off	Off
2	Off	Off	On/off	On/off
3	Off	Off	On/off	On/off

Notes: Off: The input pull-up transistor is always off.
On/off: The input pull-up transistor is on if P2PCR = 1 and P2DDR = 0, but off otherwise.

Bit 2—Buffer Enable B (BUFEB): This bit selects whether to use ICRD as a buffer register for ICRB.

Bit 2: BUFEB	Description	
0	ICRD is used for input capture D.	(Initial value)
1	ICRD is used as a buffer register for input capture B.	

Bits 1 and 0—Clock Select (CKS1 and CKS0): These bits select external clock input or one of three internal clock sources for FRC. External clock pulses are counted on the rising edge of signals input to pin FTCI.

Bit 1: CKS1	Bit 0: CKS0	Description	
0	0	$ø_P$/2 internal clock source	(Initial value)
	1	$ø_P$/8 internal clock source	
1	0	$ø_P$/32 internal clock source	
	1	External clock source (rising edge)	

8.2.7 Timer Output Compare Control Register (TOCR)

Bit	7	6	5	4	3	2	1	0
	—	—	—	OCRS	OEA	OEB	OLVLA	OLVLB
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

TOCR is an 8-bit readable/writable register that enables output from the output compare pins, selects the output levels, and switches access between output compare registers A and B.

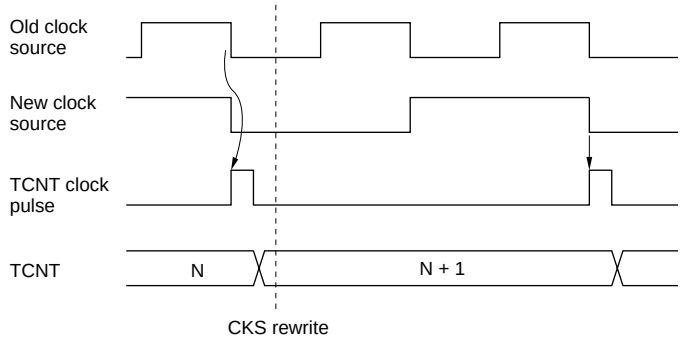
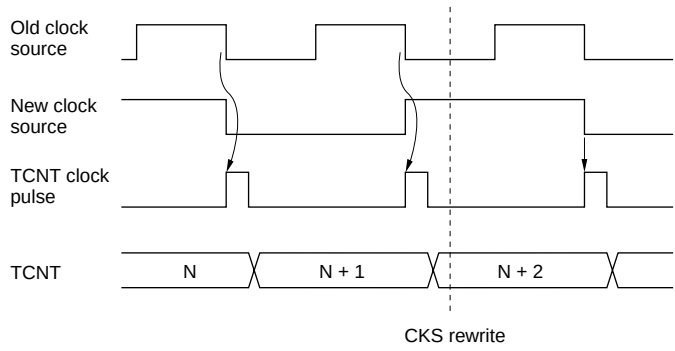
TOCR is initialized to H'E0 by a reset and in the standby modes.

Bits 7 to 5—Reserved: These bits cannot be modified and are always read as 1.

Bit 4—Output Compare Register Select (OCRS): OCRA and OCRB share the same address. When this address is accessed, the OCRS bit selects which register is accessed. This bit does not affect the operation of OCRA or OCRB.

Bit 4: OCRS	Description	
0	OCRA is selected.	(Initial value)
1	OCRB is selected.	

Table 9.5 Effect of Changing Internal Clock Sources

No.	Description	Timing
1	Low → low[*1]	
2	Low → high[*2]	

10.2.2 Duty Register (DTR)

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DTR is an 8-bit readable/writable register that specifies the duty cycle of the output pulse. Any duty cycle from 0% to 100% can be output by setting the corresponding value in DTR. The resolution is 1/250. Writing 0 (H'00) in DTR gives a 0% duty cycle. Writing 125 (H'7D) gives a 50% duty cycle. Writing 250 (H'FA) gives a 100% duty cycle.

The DTR and TCNT values are always compared. When the values match, the PWM output is placed in the 0 state.

DTR is double-buffered. A new value written in DTR does not become valid until after the timer count changes from H'F9 to H'00. While the OE bit is cleared to 0 in TCR, however, new values written in DTR become valid immediately. When DTR is read, the value read is the currently valid value.

DTR is initialized to H'FF by a reset and in the standby modes.

12.1.4 Register Configuration

Table 12.2 lists the SCI registers. These registers specify the operating mode (synchronous or asynchronous), data format and bit rate, and control the transmit and receive sections.

Table 12.2 SCI Registers

Channel	Name	Abbreviation	R/W	Initial Value	Address
0	Receive shift register	RSR	—*1	—*1	—*1
	Receive data register	RDR	R	H'00	H'FFDD
	Transmit shift register	TSR	—*1	—*1	—*1
	Transmit data register	TDR	R/W	H'FF	H'FFDB
	Serial mode register	SMR*3	R/W	H'00	H'FFD8
	Serial control register	SCR	R/W	H'00	H'FFDA
	Serial status register	SSR	R/(W)*2	H'84	H'FFDC
	Bit rate register	BRR*3	R/W	H'FF	H'FFD9
1	Receive shift register	RSR	—*1	—*1	—*1
	Receive data register	RDR	R	H'00	H'FF8D
	Transmit shift register	TSR	—*1	—*1	—*1
	Transmit data register	TDR	R/W	H'FF	H'FF8B
	Serial mode register	SMR	R/W	H'00	H'FF88
	Serial control register	SCR	R/W	H'00	H'FF8A
	Serial status register	SSR	R/(W)*2	H'84	H'FF8C
	Bit rate register	BRR	R/W	H'FF	H'FF89
0 and 1	Serial/timer control register	STCR	R/W	H'00	H'FFC3

Notes: *1 Cannot be read or written to.

*2 Software can write a 0 to clear the flags in bits 7 to 3, but cannot write 1 in these bits.

*3 SMR and BRR have the same addresses as I^2C bus interface registers ICCR and ICSR. For the access switching method and other details, see section 13, I^2C Bus Interface.

Bit 2—Transmit End (TEND): This bit indicates that the serial communication interface has stopped transmitting because there was no valid data in TDR when the last bit of the current character was transmitted. The TEND bit is also set to 1 when the TE bit in the serial control register (SCR) is cleared to 0.

The TEND bit is a read-only bit and cannot be modified directly. To use the TEI interrupt, first start transmitting data, which clears TEND to 0, then set TEIE to 1.

Bit 2: TEND	Description	
0	To clear TEND, the CPU must read TDRE after TDRE has been set to 1, then write a 0 in TDRE	
1	This bit is set to 1 when: 1. TE = 0 2. TDRE = 1 at the end of transmission of a character	(Initial value)

Bit 1—Multiprocessor Bit (MPB): Stores the value of the multiprocessor bit in data received in a multiprocessor format in asynchronous communication mode. This bit retains its previous value in synchronous mode, when a multiprocessor format is not used, or when the RE bit is cleared to 0 even if a multiprocessor format is used.

MPB can be read but not written.

Bit 1: MPB	Description	
0	Multiprocessor bit = 0 in receive data.	(Initial value)
1	Multiprocessor bit = 1 in receive data.	

Bit 0—Multiprocessor Bit Transfer (MPBT): Stores the value of the multiprocessor bit inserted in transmit data when a multiprocessor format is used in asynchronous communication mode. The MPBT bit is double-buffered in the same way as TSR and TDR. The MPBT bit has no effect in synchronous mode, or when a multiprocessor format is not used.

Bit 0: MPBT	Description	
0	Multiprocessor bit = 0 in transmit data.	(Initial value)
	Multiprocessor bit = 1 in transmit data.	

In receiving, the SCI operates as follows.

1. The SCI monitors the receive data line and synchronizes internally when it detects a start bit.

2. Receive data is shifted into RSR in order from LSB to MSB.

3. The parity bit and stop bit are received.

   After receiving these bits, the SCI makes the following checks:

   a. Parity check: The number of 1s in the receive data must match the even or odd parity setting of the O/E bit in SMR.

   b. Stop bit check: The stop bit value must be 1. If there are two stop bits, only the first stop bit is checked.

   c. Status check: RDRF must be 0 so that receive data can be loaded from RSR into RDR.

   If these checks all pass, the SCI sets RDRF to 1 and stores the received data in RDR. If one of the checks fails (receive error), the SCI operates as indicated in table 12.10.

Note: When a receive error flag is set, further receiving is disabled. The RDRF bit is not set to 1. Be sure to clear the error flags.

4. After setting RDRF to 1, if the RIE bit (receive-end interrupt enable) is set to 1 in SCR, the SCI requests an RXI (receive-end) interrupt. If one of the error flags (ORER, PER, or FER) is set to 1 and the RIE bit in SCR is also set to 1, the SCI requests an ERI (receive-error) interrupt.

Table 12.10 Receive Error Conditions and SCI Operation

Receive Error	Abbreviation	Condition	Data Transfer
Overrun error	ORER	Receiving of next data ends while RDRF is still set to 1 in SSR	Receive data not loaded from RSR into RDR
Framing error	FER	Stop bit is 0	Receive data loaded from RSR into RDR
Parity error	PER	Parity of receive data differs from even/odd parity setting in SMR	Receive data loaded from RSR into RDR

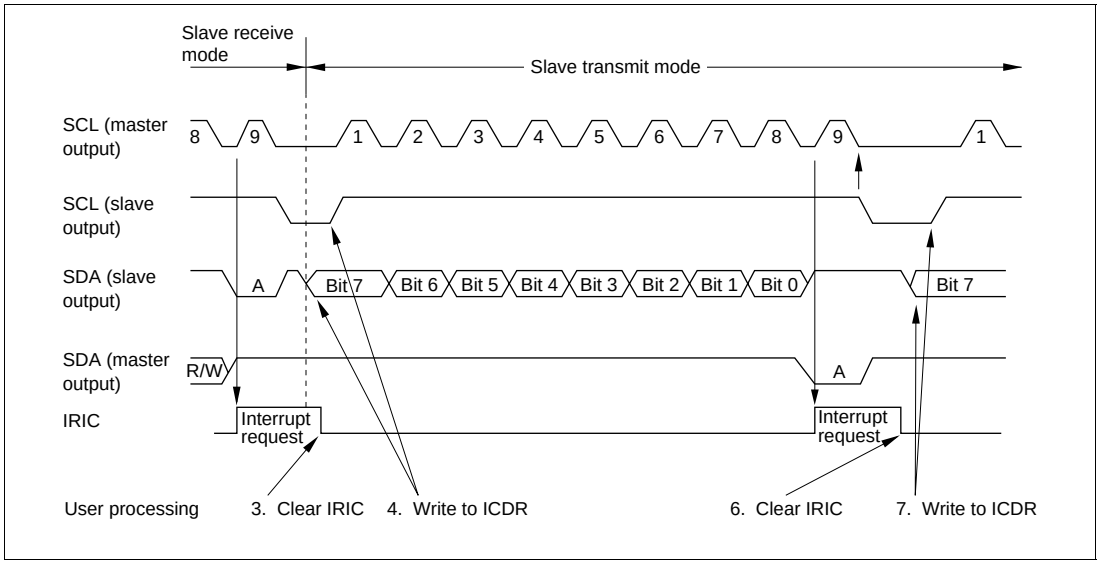


Figure 13.8 Timing in Slave Transmit Mode (MLS = WAIT = ACK = 0)

13.3.5 Slave Receive Operation

In slave receive mode, the master device outputs the transmit clock and transmit data, and the slave device returns an acknowledge signal. The receive procedure and operations in slave receive mode are described below. See also figure 13.9.

1. Set bits MLS and WAIT in ICMR and bits MST, TRS, and ACK in ICCR according to the operating mode. Set bit ICE in ICCR to 1, establishing slave receive mode.

2. A start condition output by the master device sets BBSY to 1 in ICSR.

3. After the slave device detects the start condition, if the first byte matches its slave address, at the ninth clock pulse the slave device drives SDA low to acknowledge the transfer. At the same time, IRIC is set to 1 in ICSR. If IEIC is 1 in ICCR, a CPU interrupt is requested. The slave device holds SCL low from the fall of the receive clock until it has read the data in ICDR.

4. Software clears IRIC to 0 in ICSR.

5. When ICDR is read, receiving of the next data starts.

Steps 4 and 5 can be repeated to receive data continuously. When a stop condition is detected (a low-to-high transition of SDA while SCL is high), BBSY is cleared to 0 in ICSR.

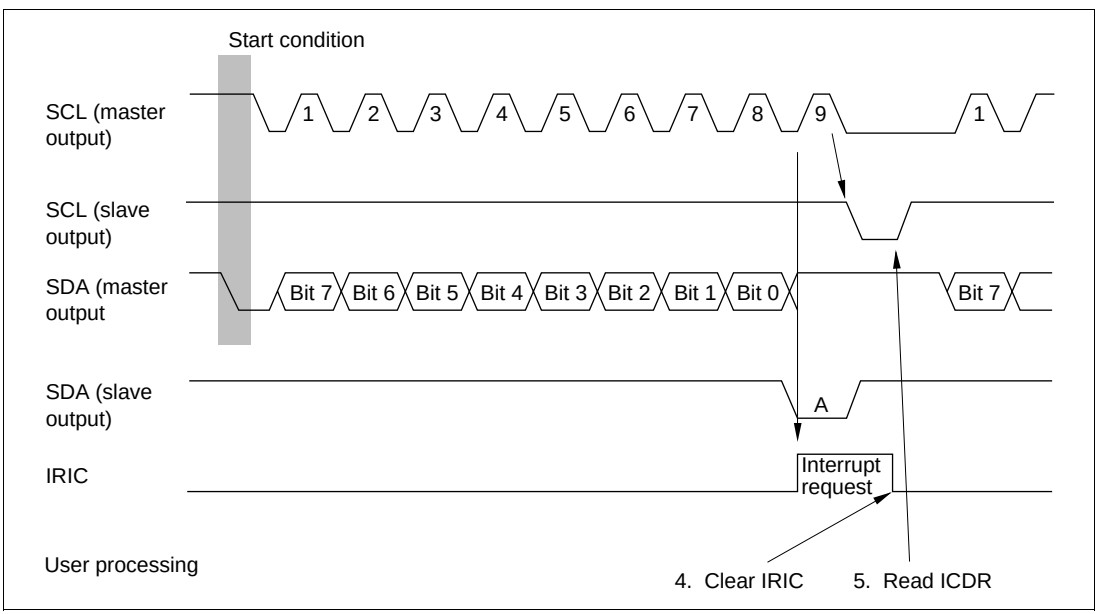


Figure 13.9 Timing in Slave Receive Mode (MLS = WAIT = ACK = ACKB = 0)

- Note on Issuance of Stop Condition

  If the rise of SCL is weakened by external pull-up resistance R and bus load capacitance C in master mode, or if SCL is pulled to the low level by a slave device, the timing at which SCL is lowered by the internal bit synchronization circuit may be delayed by 1t SCL. If, in this case, SCL is identified as being low at the bit synchronization circuit sampling timing, and a stop condition issuing instruction is executed before the reference SCL clock next falls, as in figure 13.18, SDA will change from high to low to high while SCL remains high. As a result, a stop condition will be issued before the end of the 9th clock.

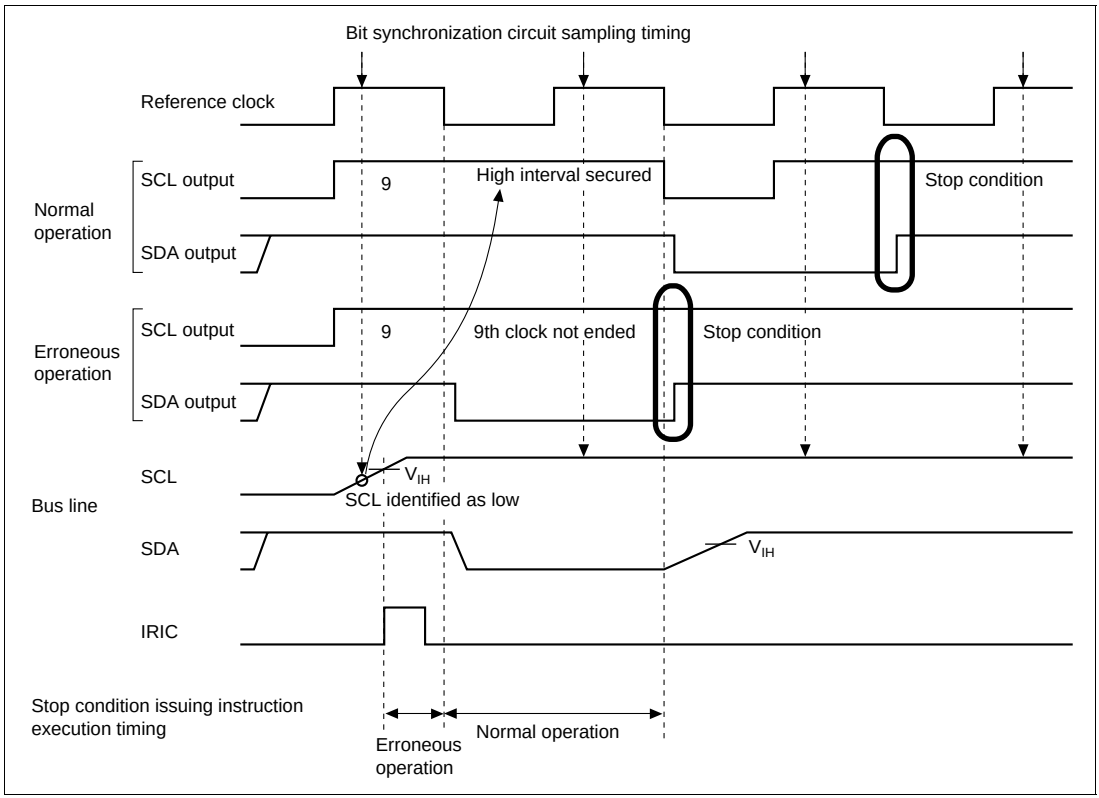
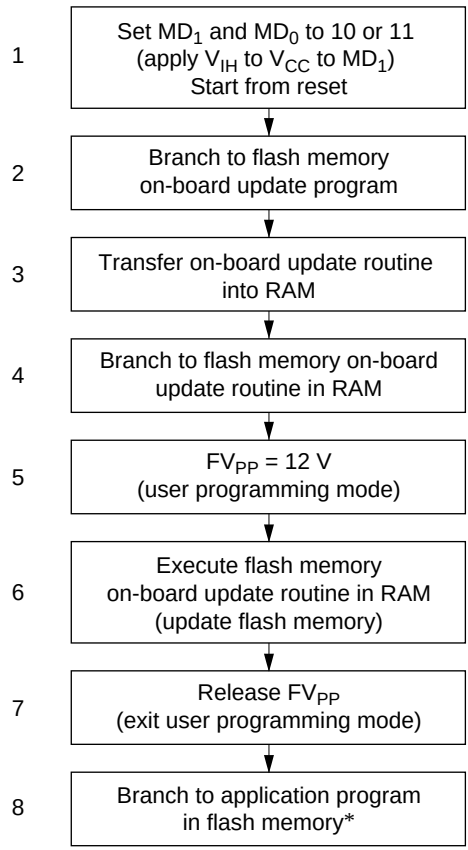


Figure 13.18 Stop Condition Erroneous Operation Timing

User Programming Mode Execution Procedure (Example)*: Figure 19.7 shows the execution procedure for user programming mode when the on-board update routine is executed in RAM.

Note: * Do not apply 12 V to the FV_{PP} pin during normal operation. To prevent flash memory from being accidentally programmed or erased due to program runaway etc., apply 12 V to FV_{PP} only when programming or erasing flash memory. Overprogramming or overerasing due to program runaway can cause memory cells to malfunction. While 12 V is applied, the watchdog timer should be running and enabled to halt runaway program execution, so that program runaway will not lead to overprogramming or overerasing. For details on applying, releasing, and shutting off V_{PP}, see section 19.7, Flash Memory Programming and Erasing Precautions (5).



Procedure

The flash memory on-board update program is written in flash memory ahead of time by the user.

1. Set MD1 and MD0 of the H8/3434F to 10 or 11, and start from a reset.
2. Branch to the flash memory on-board update program in flash memory.
3. Transfer the on-board update routine into RAM.
4. Branch to the on-board update routine that was transferred into RAM.
5. Apply 12 V to the FV_{PP} pin, to enter user programming mode.
6. Execute the flash memory on-board update routine in RAM, to perform an on-board update of the flash memory.
7. Change the voltage at the FV_{PP} pin from 12 V to V_{CC}, to exit user programming mode.
8. After the on-board update of flash memory ends, execution branches to an application program in flash memory.

Note: * After the update is finished, when input of 12 V to the FV_{PP} pin is released, the flash memory read setup time (t_{FRS}) must elapse before any program in flash memory is executed. This is the required setup time from when the FV_{PP} pin reaches the (V_{CC} + 2 V) level after 12 V is released until flash memory can be read.

Figure 19.7 User Programming Mode Operation (Example)

20.3.2 User Programming Mode

When set to user programming mode, the H8/3437F can erase and program its flash memory by executing a user program. On-board updates of the on-chip flash memory can be carried out by providing on-board circuits for supplying V_{PP} and data, and storing an update program in part of the program area.

To select user programming mode, select a mode that enables the on-chip ROM (mode 2 or 3) and apply 12 V to the FV_{PP} pin, either during a reset, or after the reset has ended (been released) but while flash memory is not being accessed. In user programming mode, the on-chip supporting modules operate as they normally would in mode 2 or 3, except for the flash memory. However, hardware standby mode cannot be set while 12 V is applied to the FV_{PP} pin.

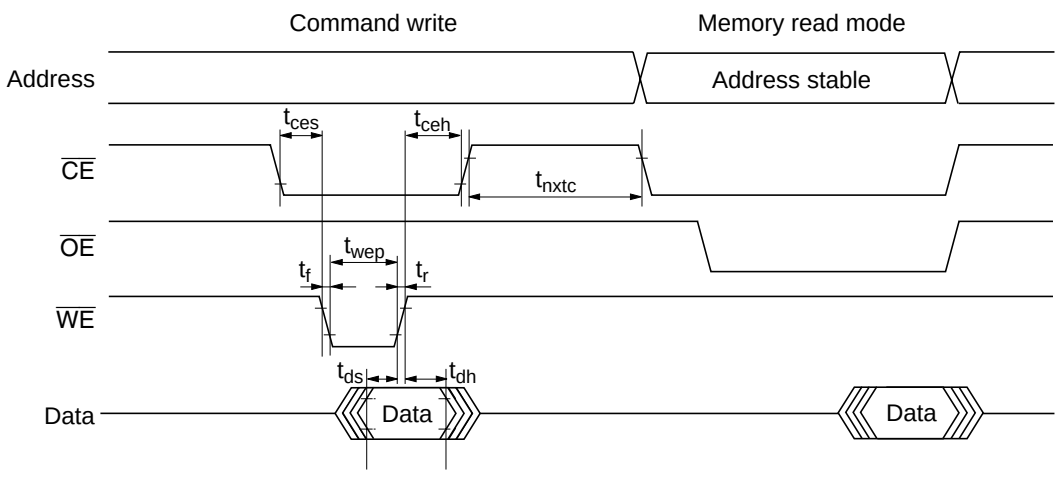
The flash memory cannot be read while it is being programmed or erased, so the update program must either be stored in external memory, or transferred temporarily to the RAM area and executed in RAM.

Memory Read Mode

1. After completion of auto-program/auto-erase/status read operations, a transition is made to the command wait state. When reading memory contents, a transition to memory read mode must first be made with a command write, after which the memory contents are read.
2. In memory read mode, command writes can be performed in the same way as in the command wait state.
3. Once memory read mode has been entered, consecutive reads can be performed.
4. After powering up, memory read mode is entered.

Table 21.13 AC Characteristics in Memory Read Mode
(Conditions: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, T_a = 25°C ±5°C)

Item	Symbol	Min	Max	Unit	Notes
Command write cycle	t_{nxtc}	20		µs	
$\overline{CE}$ hold time	t_{ceh}	0		ns	
$\overline{CE}$ setup time	t_{ces}	0		ns	
Data hold time	t_{dh}	50		ns	
Data setup time	t_{ds}	50		ns	
Programming pulse width	t_{wep}	70		ns	
$\overline{WE}$ rise time	t_r		30	ns	
$\overline{WE}$ fall time	t_f		30	ns	



Note: Data is latched at the rising edge of $\overline{WE}$.

Figure 21.16 Timing Waveforms for Memory Read after Command Write

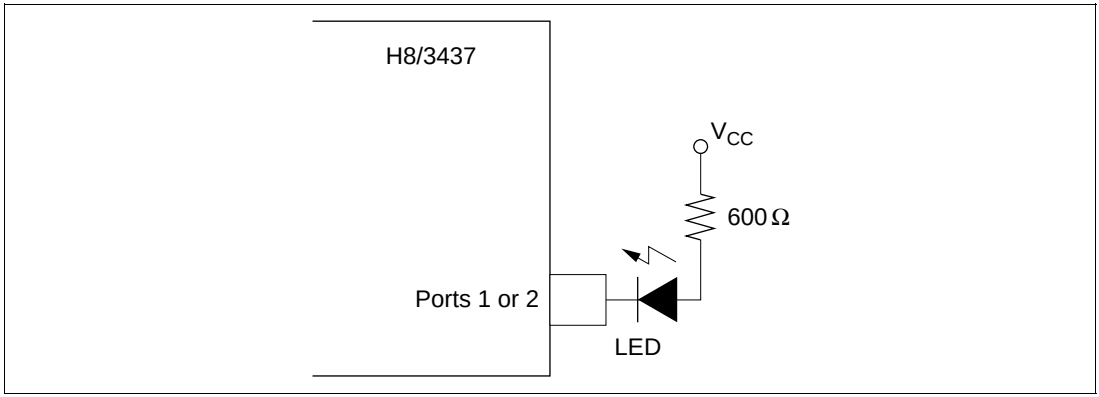


Figure 23.2 Example of Circuit for Driving an LED (5-V Version)

Table 23.7 Bus Drive Characteristics

Conditions: V_{CC} = 2.7 V to 5.5 V*, V_{SS} = 0 V, Ta = –20˚C to +75°C

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Output low level voltage	SCL, SDA PA_4 to PA_7 (bus drive selection)	V_{OL}	—	—	0.5	V	$V_{CC}B$ = 5 V ±10% I_{OL} = 16 mA
			—	—	0.5		$V_{CC}B$ = 2.7 V to 5.5 V* I_{OL} = 8 mA
			—	—	0.4		$V_{CC}B$ = 2.7 V to 5.5 V* I_{OL} = 3 mA

Note: * In the F-ZTAT LH version, V_{CC} = 3.0 V to 5.5 V, $V_{CC}B$ = 3.0 V to 5.5 V.

23.2.2 AC Characteristics

The AC characteristics are listed in four tables. Bus timing parameters are given in table 23.8, control signal timing parameters in table 23.9, timing parameters of the on-chip supporting modules in table 23.10, I^2C bus timing parameters in table 23.11, and external clock output stabilization delay time in table 23.12.

Table 23.9 Control Signal Timing

Condition A: V_{CC} = 5.0 V ±10%, $V_{CC}B$ = 5.0 V ±10%, V_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20˚C to +75˚C (regular specifications), Ta = –40˚C to +85˚C (wide-range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, $V_{CC}B$ = 4.0 V to 5.5V, V_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20˚C to +75˚C (regular specifications), Ta = –40˚C to +85˚C (wide-range specifications)

Condition C: V_{CC} = 2.7 V to 5.5 V*, $V_{CC}B$ = 2.7 V to 5.5 V*, V_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20˚C to +75˚C

		Condition C		Condition B		Condition A			
		10 MHz		12 MHz		16 MHz			Test
Item	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
$\overline{RES}$ setup time	t_{RESS}	300	—	200	—	200	—	ns	Fig. 23.9
$\overline{RES}$ pulse width	t_{RESW}	10	—	10	—	10	—	t_{cyc}	
$\overline{RESO}$ output delay time	t_{RESD}	—	200	—	120	—	100	ns	Fig. 23.25
$\overline{RESO}$ output pulse width	t_{RESOW}	132	—	132	—	132	—	t_{cyc}	
$\overline{NMI}$ setup time ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_7}$)	t_{NMIS}	300	—	150	—	150	—	ns	Fig. 23.10
$\overline{NMI}$ hold time ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_7}$)	t_{NMIH}	10	—	10	—	10	—	ns	
Interrupt pulse width for recovery from software standby mode ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_2}$, $\overline{IRQ_6}$)	t_{NMIW}	300	—	200	—	200	—	ns	
Crystal oscillator settling time (reset)	t_{OSC1}	20	—	20	—	20	—	ms	Fig. 23.11
Crystal oscillator settling time (software standby)	t_{OSC2}	8	—	8	—	8	—	ms	Fig. 23.12

Note: * In the F-ZTAT LH version, V_{CC} = 3.0 V to 5.5 V, $V_{CC}B$ = 3.0 V to 5.5 V.

23.2.4 D/A Converter Characteristics

Table 23.14 lists the characteristics of the on-chip D/A converter.

Table 23.14 D/A Converter Characteristics

Condition A: V_{CC} = 5.0 V ±10%, $V_{CC}B$ = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20 to +75˚C (regular specifications), Ta = –40 to +85˚C (wide-range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, $V_{CC}B$ = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, AV_{ref} = 4.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20 to +75˚C (regular specifications), Ta = –40 to +85˚C (wide-range specifications)

Condition C: V_{CC} = 2.7 V to 5.5 V*, $V_{CC}B$ = 2.7 V to 5.5 V*, AV_{CC} = 2.7 V to 5.5 V*, AV_{ref} = 2.7 V to AV_{CC}*, V_{SS} = AV_{SS} = 0 V, ø = 2.0 MHz to maximum operating frequency, Ta = –20 to +75˚C

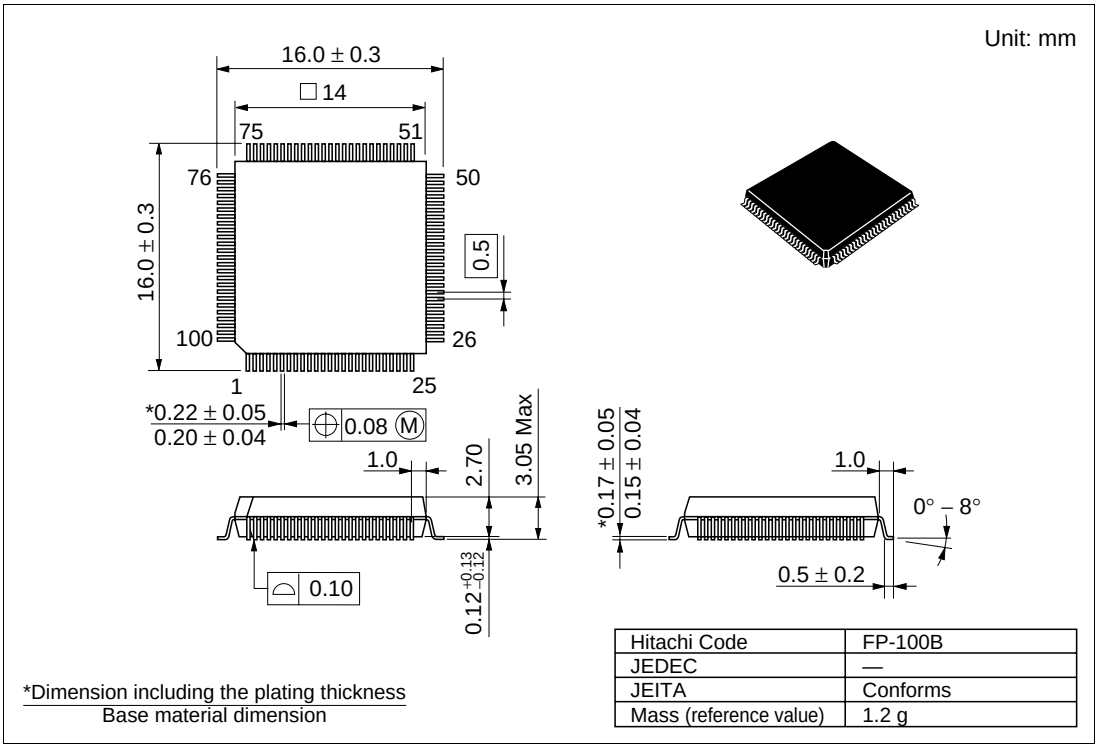
	Condition C			Condition B			Condition A				
	10 MHz			12 MHz			16 MHz				Test
Item	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Conditions
Resolution	8	8	8	8	8	8	8	8	8	Bits	
Conversion time (settling time)	—	—	10.0	—	—	10.0	—	—	10.0	µs	30 pF load capacitance
Absolute accuracy	—	±2.0	±3.0	—	±1.0	±1.5	—	±1.0	±1.5	LSB	2 MΩ load resistance
	—	—	±2.0	—	—	±1.0	—	—	±1.0	LSB	4 MΩ load resistance

Note: * In the F-ZTAT LH version, V_{CC} = 3.0 V to 5.5 V, $V_{CC}B$ = 3.0 V to 5.5 V, AV_{CC} = 3.0 V to 5.5 V, AV_{ref} = 3.0 V to AV_{CC}.

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
MOV	MOV.B #xx:8, Rd	1					
	MOV.B Rs, Rd	1					
	MOV.B @Rs, Rd	1			1		
	MOV.B @(d:16,Rs), Rd	2			1		
	MOV.B @Rs+, Rd	1			1		2
	MOV.B @aa:8, Rd	1			1		
	MOV.B @aa:16, Rd	2			1		
	MOV.B Rs, @Rd	1			1		
	MOV.B Rs, @(d:16, Rd)	2			1		
	MOV.B Rs, @–Rd	1			1		2
	MOV.B Rs, @aa:8	1			1		
	MOV.B Rs, @aa:16	2			1		
	MOV.W #xx:16, Rd	2					
	MOV.W Rs, Rd	1					
	MOV.W @Rs, Rd	1				1	
	MOV.W @(d:16, Rs), Rd	2				1	
	MOV.W @Rs+, Rd	1				1	2
	MOV.W @aa:16, Rd	2				1	
	MOV.W Rs, @Rd	1				1	
	MOV.W Rs, @(d:16, Rd)	2				1	
	MOV.W Rs, @–Rd	1				1	2
	MOV.W Rs, @aa:16	2				1	
MOVFPE	MOVFPE @aa:16, Rd	Not supported					
MOVTPE	MOVTPE.Rs, @aa:16	Not supported					
MULXU	MULXU.Rs, Rd	1					12
NEG	NEG.B Rd	1					
NOP	NOP	1					
NOT	NOT.B Rd	1					

Appendix H Package Dimensions

Figure H.1 shows the dimensions of the FP-100B package. Figure H.2 shows the dimensions of the TFP-100B package.



Hitachi Code	FP-100B
JEDEC	—
JEITA	Conforms
Mass (reference value)	1.2 g

Figure H.1 Package Dimensions (FP-100B)