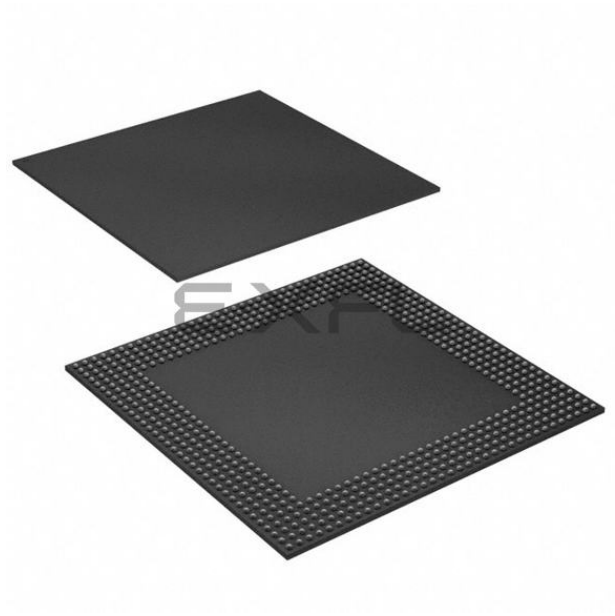


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

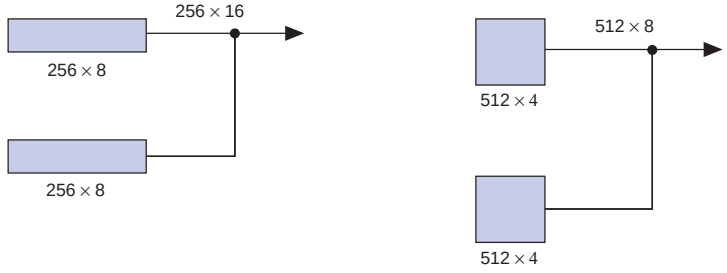
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	624
Number of Logic Elements/Cells	4992
Total RAM Bits	24576
Number of I/O	406
Number of Gates	158000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	600-BGA
Supplier Device Package	600-BGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k100abc600-1

Larger blocks of RAM are created by combining multiple EABs. For example, two 256 × 8 RAM blocks can be combined to form a 256 × 16 RAM block; two 512 × 4 blocks of RAM can be combined to form a 512 × 8 RAM block. See Figure 3.

Figure 3. Examples of Combining EABs



If necessary, all EABs in a device can be cascaded to form a single RAM block. EABs can be cascaded to form RAM blocks of up to 2,048 words without impacting timing. Altera's software automatically combines EABs to meet a designer's RAM specifications.

EABs provide flexible options for driving and controlling clock signals. Different clocks can be used for the EAB inputs and outputs. Registers can be independently inserted on the data input, EAB output, or the address and `WE` inputs. The global signals and the EAB local interconnect can drive the `WE` signal. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control the `WE` signal or the EAB clock signals.

Each EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs. See Figure 4.

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks; the other two can be used for clear/preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I/O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I/O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

Logic Element

The LE, the smallest unit of logic in the FLEX 10K architecture, has a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect. See Figure 6.

Figure 6. FLEX 10K Logic Element

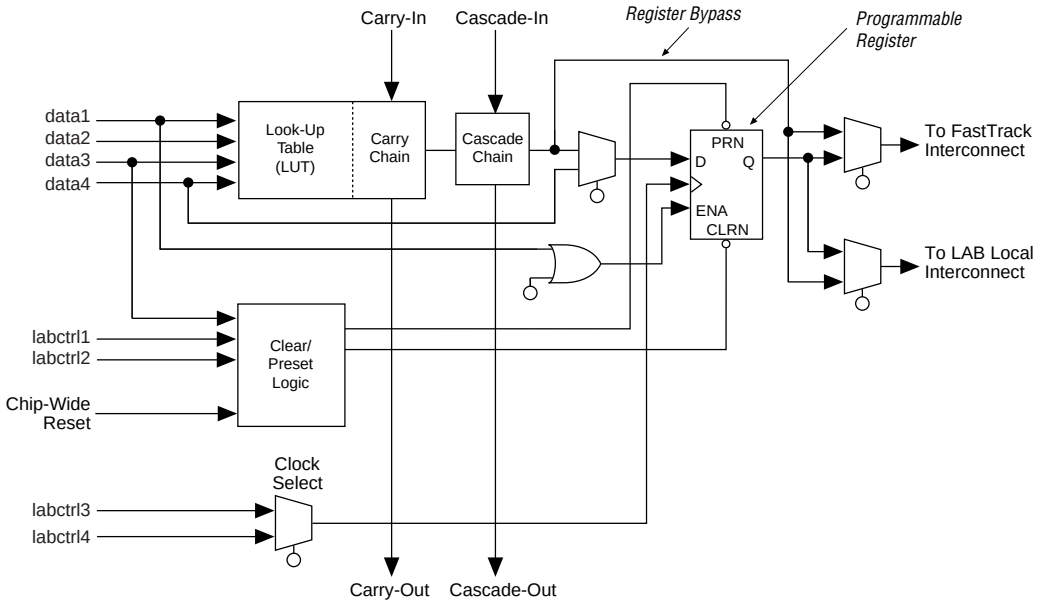
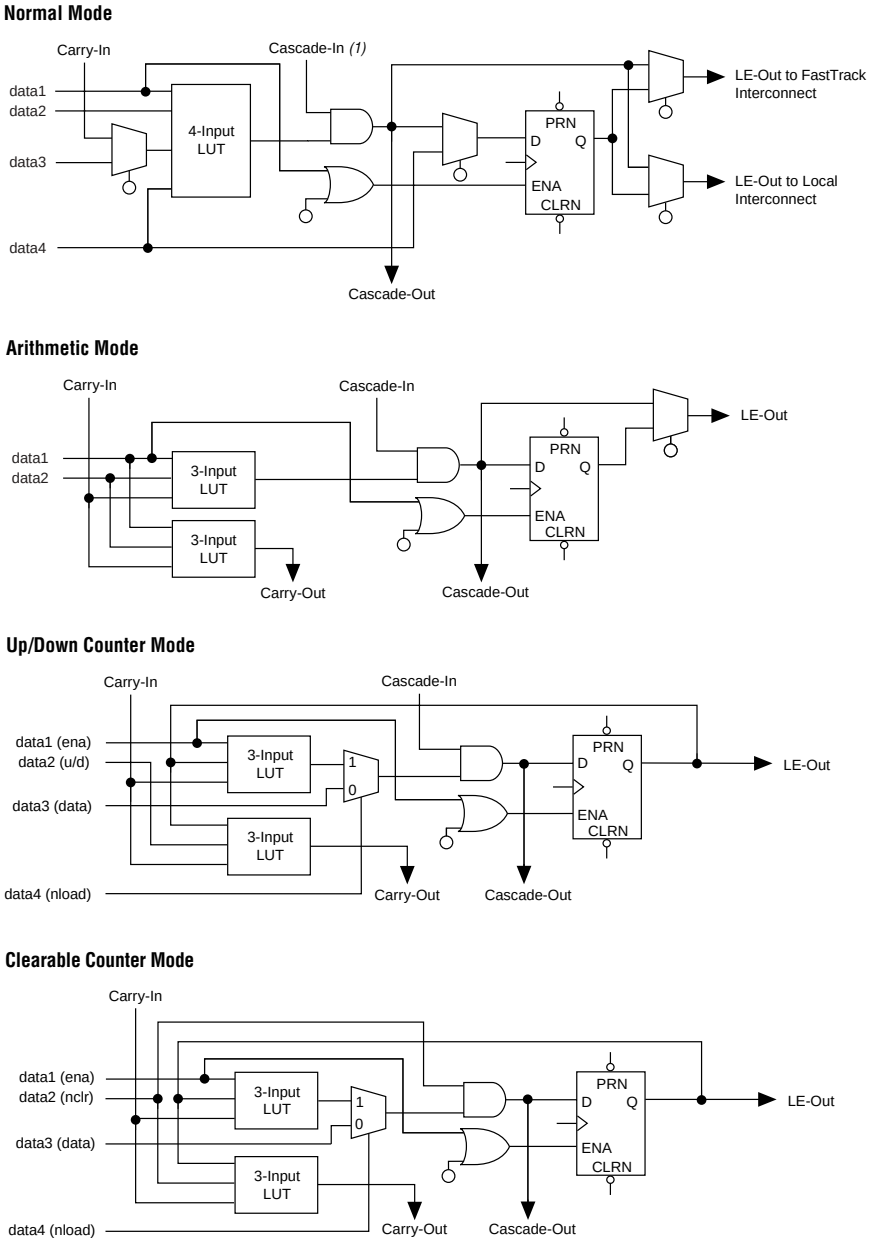


Figure 9. FLEX 10K LE Operating Modes



Note:
(1) Packed registers cannot be used with the cascade chain.

Figure 11. LAB Connections to Row & Column Interconnect

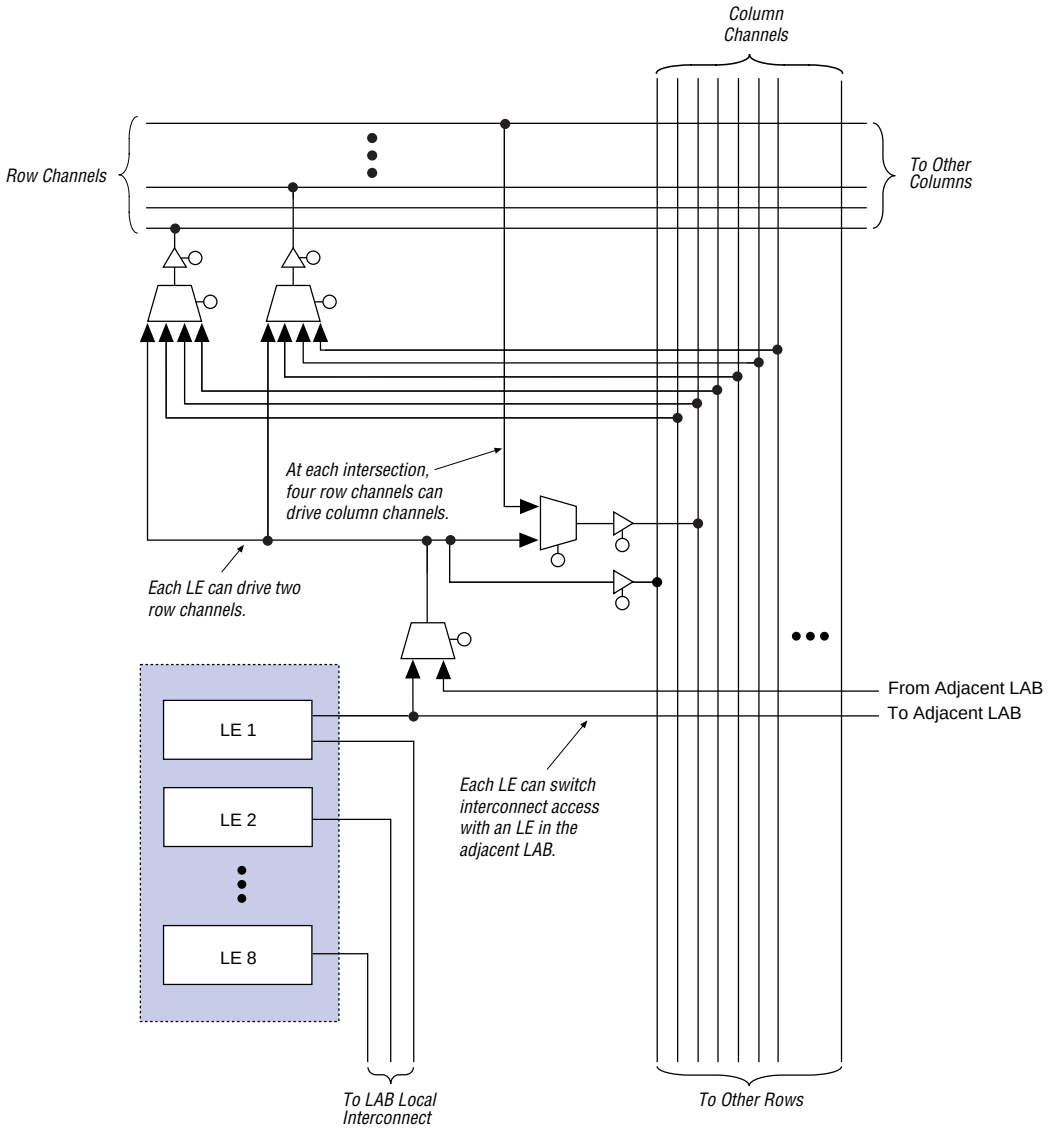


Table 8. EPF10K10, EPF10K20, EPF10K30, EPF10K40 & EPF10K50 Peripheral Bus Sources

Peripheral Control Signal	EPF10K10 EPF10K10A	EPF10K20	EPF10K30 EPF10K30A	EPF10K40	EPF10K50 EPF10K50V
OE0	Row A	Row A	Row A	Row A	Row A
OE1	Row A	Row B	Row B	Row C	Row B
OE2	Row B	Row C	Row C	Row D	Row D
OE3	Row B	Row D	Row D	Row E	Row F
OE4	Row C	Row E	Row E	Row F	Row H
OE5	Row C	Row F	Row F	Row G	Row J
CLKENA0/CLK0/GLOBAL0	Row A	Row A	Row A	Row B	Row A
CLKENA1/OE6/GLOBAL1	Row A	Row B	Row B	Row C	Row C
CLKENA2/CLR0	Row B	Row C	Row C	Row D	Row E
CLKENA3/OE7/GLOBAL2	Row B	Row D	Row D	Row E	Row G
CLKENA4/CLR1	Row C	Row E	Row E	Row F	Row I
CLKENA5/CLK1/GLOBAL3	Row C	Row F	Row F	Row H	Row J

Table 9. EPF10K70, EPF10K100, EPF10K130V & EPF10K250A Peripheral Bus Sources

Peripheral Control Signal	EPF10K70	EPF10K100 EPF10K100A	EPF10K130V	EPF10K250A
OE0	Row A	Row A	Row C	Row E
OE1	Row B	Row C	Row E	Row G
OE2	Row D	Row E	Row G	Row I
OE3	Row I	Row L	Row N	Row P
OE4	Row G	Row I	Row K	Row M
OE5	Row H	Row K	Row M	Row O
CLKENA0/CLK0/GLOBAL0	Row E	Row F	Row H	Row J
CLKENA1/OE6/GLOBAL1	Row C	Row D	Row F	Row H
CLKENA2/CLR0	Row B	Row B	Row D	Row F
CLKENA3/OE7/GLOBAL2	Row F	Row H	Row J	Row L
CLKENA4/CLR1	Row H	Row J	Row L	Row N
CLKENA5/CLK1/GLOBAL3	Row E	Row G	Row I	Row K

Figure 15. FLEX 10K Column-to-IOE Connections

The values for m and n are provided in Table 11.

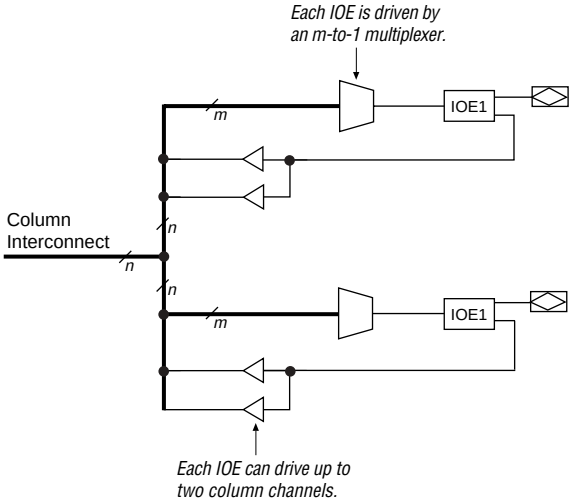


Table 11 lists the FLEX 10K column-to-IOE interconnect resources.

Table 11. FLEX 10K Column-to-IOE Interconnect Resources

Device	Channels per Column (*n*)	Column Channel per Pin (*m*)
EPF10K10 EPF10K10A	24	16
EPF10K20	24	16
EPF10K30 EPF10K30A	24	16
EPF10K40	24	16
EPF10K50 EPF10K50V	24	16
EPF10K70	24	16
EPF10K100 EPF10K100A	24	16
EPF10K130V	32	24
EPF10K250A	40	32

Table 12 describes the FLEX 10K device supply voltages and MultiVolt I/O support levels.

Table 12. Supply Voltages & MultiVolt I/O Support Levels

Devices	Supply Voltage (V)		MultiVolt I/O Support Levels (V)	
	V_{CCINT}	V_{CCIO}	Input	Output
FLEX 10K *(1)*	5.0	5.0	3.3 or 5.0	5.0
	5.0	3.3	3.3 or 5.0	3.3 or 5.0
EPF10K50V *(1)*	3.3	3.3	3.3 or 5.0	3.3 or 5.0
EPF10K130V	3.3	3.3	3.3 or 5.0	3.3 or 5.0
FLEX 10KA *(1)*	3.3	3.3	2.5, 3.3, or 5.0	3.3 or 5.0
	3.3	2.5	2.5, 3.3, or 5.0	2.5

Note
(1) 240-pin QFP packages do not support the MultiVolt I/O features, so they do not have separate V_{CCIO} pins.

Power Sequencing & Hot-Socketing

Because FLEX 10K devices can be used in a multi-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power supplies can be powered in any order.

Signals can be driven into FLEX 10KA devices before and during power up without damaging the device. Additionally, FLEX 10KA devices do not drive out during power up. Once operating conditions are reached, FLEX 10KA devices operate as specified by the user.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All FLEX 10K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. All FLEX 10K devices can also be configured using the JTAG pins through the BitBlaster serial download cable, or ByteBlasterMV parallel port download cable, or via hardware that uses the Jam™ programming and test language. JTAG BST can be performed before or after configuration, but not during configuration. FLEX 10K devices support the JTAG instructions shown in Table 13.

Tables 22 through 25 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for EPF10K50V and EPF10K130V devices.

Table 22. EPF10K50V & EPF10K130V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground *(2)*	–0.5	4.6	V
V_I	DC input voltage		–2.0	5.75	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		RQFP and BGA packages, under bias		135	° C

Table 23. EPF10K50V & EPF10K130V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
V_{CCIO}	Supply voltage for output buffers	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
V_I	Input voltage	*(5)*	-0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 28. FLEX 10KA 3.3-V Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		1.7 or $0.5 \times V_{CCINT}$, whichever is lower		5.75	V
V_{IL}	Low-level input voltage		–0.5		$0.3 \times V_{CCINT}$	V
V_{OH}	3.3-V high-level TTL output voltage	I_{OH} = –11 mA DC, V_{CCIO} = 3.00 V *(8)*	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(8)*	V_{CCIO} – 0.2			V
	3.3-V high-level PCI output voltage	I_{OH} = –0.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(8)*	$0.9 \times V_{CCIO}$			V
	2.5-V high-level output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 2.30 V *(8)*	2.1			V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V *(8)*	2.0			V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V *(8)*	1.7			V
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 9 mA DC, V_{CCIO} = 3.00 V *(9)*			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(9)*			0.2	V
	3.3-V low-level PCI output voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(9)*			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V *(9)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(9)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(9)*			0.7	V
I_I	Input pin leakage current	V_I = 5.3 V to –0.3 V *(10)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 5.3 V to –0.3 V *(10)*	–10		10	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load		0.3	10	mA
		V_I = ground, no load *(11)*		10		mA

Table 36. Interconnect Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
$t_{DIN2IOE}$	Delay from dedicated input pin to IOE control input	*(7)*
$t_{DCLK2LE}$	Delay from dedicated clock pin to LE or EAB clock	*(7)*
$t_{DIN2DATA}$	Delay from dedicated input or clock to LE or EAB data	*(7)*
$t_{DCLK2IOE}$	Delay from dedicated clock pin to IOE clock	*(7)*
t_{DIN2LE}	Delay from dedicated input pin to LE or EAB control input	*(7)*
$t_{SAMELAB}$	Routing delay for an LE driving another LE in the same LAB	
$t_{SAMEROW}$	Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row	*(7)*
$t_{SAMECOLUMN}$	Routing delay for an LE driving an IOE in the same column	*(7)*
$t_{DIFFROW}$	Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row	*(7)*
$t_{TWOROWS}$	Routing delay for a row IOE or EAB driving an LE or EAB in a different row	*(7)*
$t_{LEPERIPH}$	Routing delay for an LE driving a control signal of an IOE via the peripheral control bus	*(7)*
$t_{LABCARRY}$	Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	

Table 37. External Timing Parameters *Notes (8), (10)*

Symbol	Parameter	Conditions
t_{DRR}	Register-to-register delay via four LEs, three row interconnects, and four local interconnects	*(9)*
t_{INSU}	Setup time with global clock at IOE register	
t_{INH}	Hold time with global clock at IOE register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE register	

Table 38. External Bidirectional Timing Parameters *Note (10)*

Symbol	Parameter	Condition
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at adjacent LE register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at adjacent LE register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	
$t_{XZBIDIR}$	Synchronous IOE output buffer disable delay	
$t_{ZXBIDIR}$	Synchronous IOE output buffer enable delay, slow slew rate = off	

Notes to tables:

(1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.

(2) Operating conditions: V_{CCIO} = 5.0 V ± 5% for commercial use in FLEX 10K devices.
V_{CCIO} = 5.0 V ± 10% for industrial use in FLEX 10K devices.
V_{CCIO} = 3.3 V ± 10% for commercial or industrial use in FLEX 10KA devices.

(3) Operating conditions: V_{CCIO} = 3.3 V ± 10% for commercial or industrial use in FLEX 10K devices.
V_{CCIO} = 2.5 V ± 0.2 V for commercial or industrial use in FLEX 10KA devices.

(4) Operating conditions: V_{CCIO} = 2.5 V, 3.3 V, or 5.0 V.

(5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the WE signal is registered.

(6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.

(7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.

(8) External reference timing parameters are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.

(9) Contact Altera Applications for test circuit specifications and test conditions.

(10) These timing parameters are sample-tested only.

Figures 29 and 30 show the asynchronous and synchronous timing waveforms, respectively, for the EAB macroparameters in Table 34.

Figure 29. EAB Asynchronous Timing Waveforms

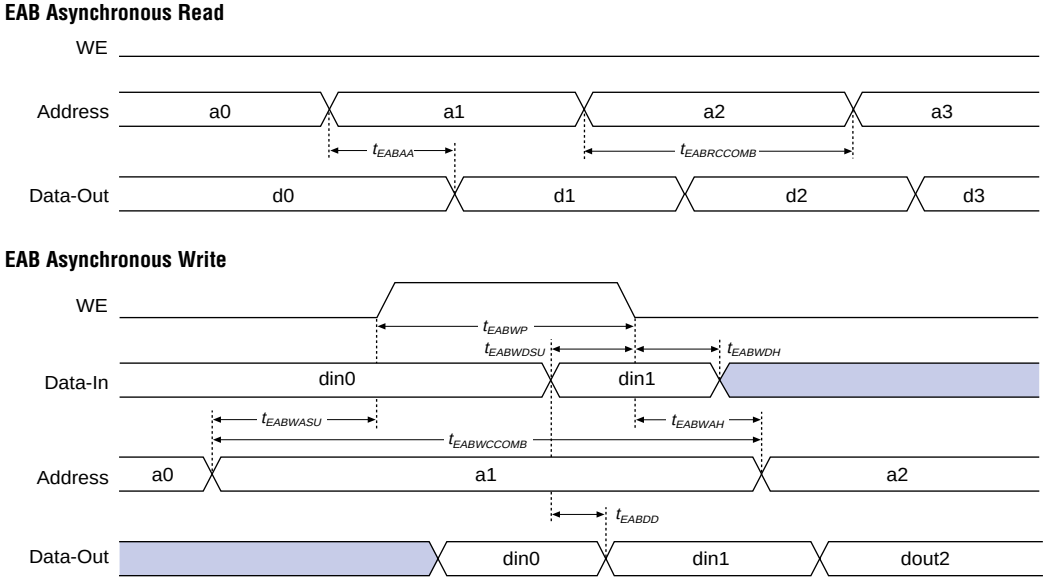


Table 54. EPF10K50 Device Interconnect Timing Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{DIN2IOE}$		8.4		10.2	ns
t_{DIN2LE}		3.6		4.8	ns
$t_{DIN2DATA}$		5.5		7.2	ns
$t_{DCLK2IOE}$		4.6		6.2	ns
$t_{DCLK2LE}$		3.6		4.8	ns
$t_{SAMELAB}$		0.3		0.3	ns
$t_{SAMEROW}$		3.3		3.7	ns
$t_{SAMECOLUMN}$		3.9		4.1	ns
$t_{DIFFROW}$		7.2		7.8	ns
$t_{TWOROWS}$		10.5		11.5	ns
$t_{LEPERIPH}$		7.5		8.2	ns
$t_{LABCARRY}$		0.4		0.6	ns
$t_{LABCASC}$		2.4		3.0	ns

Table 55. EPF10K30, EPF10K40 & EPF10K50 Device External Timing Parameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{DRR}		17.2		21.1	ns
t_{INSU} *(2)*, *(3)*	5.7		6.4		ns
t_{INH} *(3)*	0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	8.8	2.0	11.2	ns

Table 56. EPF10K30, EPF10K40 & EPF10K50 Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{INSUBIDIR}$	4.1		4.6		ns
$t_{INHBIDIR}$	0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	8.8	2.0	11.2	ns
$t_{XZBIDIR}$		12.3		15.0	ns
$t_{ZXBIDIR}$		12.3		15.0	ns

Table 59. EPF10K70 Device EAB Internal Microparameters *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.3		1.5		1.9	ns
$t_{EABDATA2}$		4.3		4.8		6.0	ns
t_{EABWE1}		0.9		1.0		1.2	ns
t_{EABWE2}		4.5		5.0		6.2	ns
t_{EABCLK}		0.9		1.0		2.2	ns
t_{EABCO}		0.4		0.5		0.6	ns
$t_{EABBYPASS}$		1.3		1.5		1.9	ns
t_{EABSU}	1.3		1.5		1.8		ns
t_{EABH}	1.8		2.0		2.5		ns
t_{AA}		7.8		8.7		10.7	ns
t_{WP}	5.2		5.8		7.2		ns
t_{WDSU}	1.4		1.6		2.0		ns
t_{WDH}	0.3		0.3		0.4		ns
t_{WASU}	0.4		0.5		0.6		ns
t_{WAH}	0.9		1.0		1.2		ns
t_{WO}		4.5		5.0		6.2	ns
t_{DD}		4.5		5.0		6.2	ns
t_{EABOUT}		0.4		0.5		0.6	ns
t_{EABCH}	4.0		4.0		4.0		ns
t_{EABCL}	5.2		5.8		7.2		ns

Notes to tables:
(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Tables 64 through 70 show EPF10K100 device internal and external timing parameters.

Table 64. EPF10K100 Device LE Timing Microparameters *Note (1)*

Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		1.5		1.5		2.0	ns
t_{CLUT}		0.4		0.4		0.5	ns
t_{RLUT}		1.6		1.6		2.0	ns
t_{PACKED}		0.9		0.9		1.3	ns
t_{EN}		0.9		0.9		1.2	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		1.1		1.1		1.4	ns
t_{CGENR}		1.2		1.2		1.5	ns
t_{CASC}		1.1		1.1		1.3	ns
t_{C}		0.8		0.8		1.0	ns
t_{CO}		1.0		1.0		1.4	ns
t_{COMB}		0.5		0.5		0.7	ns
t_{SU}	2.1		2.1		2.6		ns
t_{H}	2.3		2.3		3.1		ns
t_{PRE}		1.0		1.0		1.4	ns
t_{CLR}		1.0		1.0		1.4	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns

Table 68. EPF10K100 Device Interconnect Timing Microparameters *Note (1)*

Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		10.3		10.3		12.2	ns
t_{DIN2LE}		4.8		4.8		6.0	ns
$t_{DIN2DATA}$		7.3		7.3		11.0	ns
$t_{DCLK2IOE}$ without ClockLock or ClockBoost circuitry		6.2		6.2		7.7	ns
$t_{DCLK2IOE}$ with ClockLock or ClockBoost circuitry		2.3		–		–	ns
$t_{DCLK2LE}$ without ClockLock or ClockBoost circuitry		4.8		4.8		6.0	ns
$t_{DCLK2LE}$ with ClockLock or ClockBoost circuitry		2.3		–		–	ns
$t_{SAMELAB}$		0.4		0.4		0.5	ns
$t_{SAMEROW}$		4.9		4.9		5.5	ns
$t_{SAMECOLUMN}$		5.1		5.1		5.4	ns
$t_{DIFFROW}$		10.0		10.0		10.9	ns
$t_{TWOROWS}$		14.9		14.9		16.4	ns
$t_{LEPERIPH}$		6.9		6.9		8.1	ns
$t_{LABCARRY}$		0.9		0.9		1.1	ns
$t_{LABCASC}$		3.0		3.0		3.2	ns

Table 80. EPF10K130V Device EAB Internal Microparameters *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.9		2.4		2.4	ns
$t_{EABDATA2}$		3.7		4.7		4.7	ns
t_{EABWE1}		1.9		2.4		2.4	ns
t_{EABWE2}		3.7		4.7		4.7	ns
t_{EABCLK}		0.7		0.9		0.9	ns
t_{EABCO}		0.5		0.6		0.6	ns
$t_{EABBYPASS}$		0.6		0.8		0.8	ns
t_{EABSU}	1.4		1.8		1.8		ns
t_{EABH}	0.0		0.0		0.0		ns
t_{AA}		5.6		7.1		7.1	ns
t_{WP}	3.7		4.7		4.7		ns
t_{WDSU}	4.6		5.9		5.9		ns
t_{WDH}	0.0		0.0		0.0		ns
t_{WASU}	3.9		5.0		5.0		ns
t_{WAH}	0.0		0.0		0.0		ns
t_{WO}		5.6		7.1		7.1	ns
t_{DD}		5.6		7.1		7.1	ns
t_{EABOUT}		2.4		3.1		3.1	ns
t_{EABCH}	4.0		4.0		4.0		ns
t_{EABCL}	4.0		4.7		4.7		ns

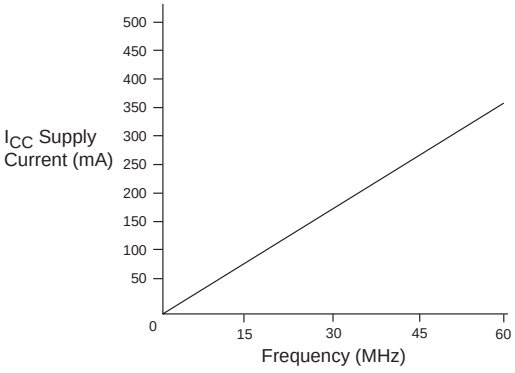
Table 88. EPF10K10A Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		8.1		9.8		13.1	ns
$t_{EABRCCOMB}$	8.1		9.8		13.1		ns
$t_{EABRCREG}$	5.8		6.9		9.3		ns
t_{EABWP}	2.0		2.4		3.2		ns
$t_{EABWCCOMB}$	3.5		4.2		5.6		ns
$t_{EABWCREG}$	9.4		11.2		14.8		ns
t_{EABDD}		6.9		8.3		11.0	ns
$t_{EABDATACO}$		1.3		1.5		2.0	ns
$t_{EABDATASU}$	2.4		3.0		3.9		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	4.1		4.9		6.5		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.4		1.6		2.2		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	2.5		3.0		4.1		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		6.2		7.5		9.9	ns

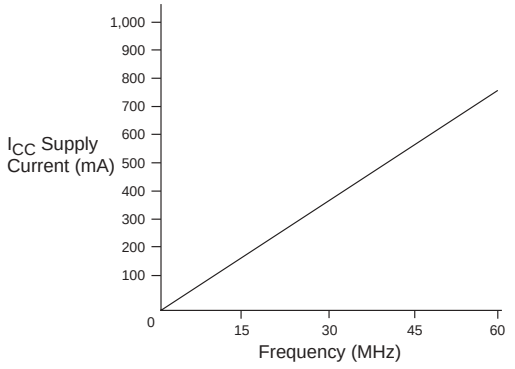
Table 95. EPF10K30A Device EAB Internal Timing Macroparameters *Note (1)*							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		9.7		11.6		16.2	ns
$t_{EABRCCOMB}$	9.7		11.6		16.2		ns
$t_{EABRCREG}$	5.9		7.1		9.7		ns
t_{EABWP}	3.8		4.5		5.9		ns
$t_{EABWCCOMB}$	4.0		4.7		6.3		ns
$t_{EABWCREG}$	9.8		11.6		16.6		ns
t_{EABDD}		9.2		11.0		16.1	ns
$t_{EABDATACO}$		1.7		2.1		3.4	ns
$t_{EABDATASU}$	2.3		2.7		3.5		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	3.3		3.9		4.9		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	3.2		3.8		5.0		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.7		4.4		5.1		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		6.1		7.3		11.3	ns

Figure 32. $I_{CCACTIVE}$ vs. Operating Frequency (Part 1 of 3)

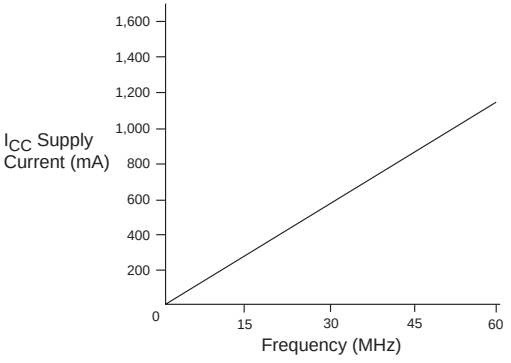
EPF10K10



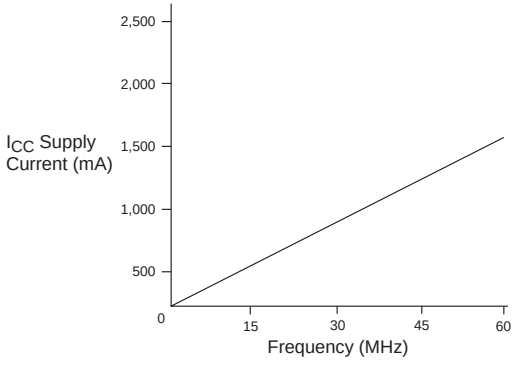
EPF10K20



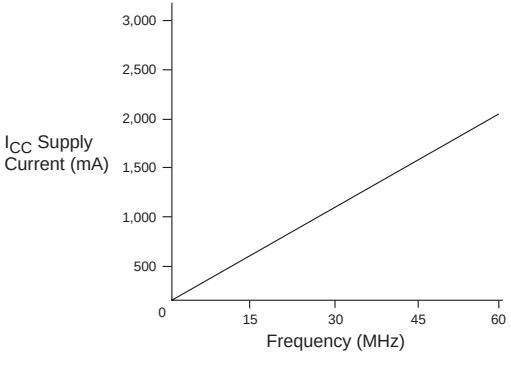
EPF10K30



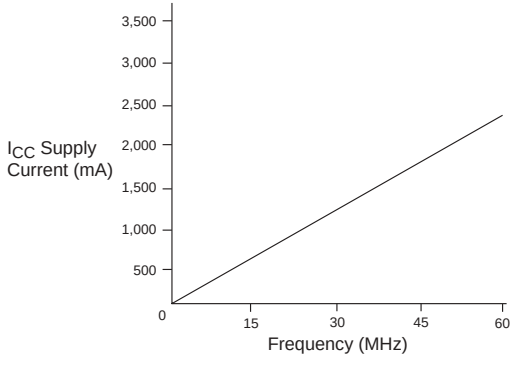
EPF10K40



EPF10K50



EPF10K70



Multiple FLEX 10K devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 116. Data Sources for Configuration

Configuration Scheme	Data Source
Configuration device	EPC1, EPC2, EPC16, or EPC1441 configuration device
Passive serial (PS)	BitBlaster, MasterBlaster, or ByteBlasterMV download cable, or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	BitBlaster, MasterBlaster, or ByteBlasterMV download cable, or microprocessor with Jam STAPL file or Jam Byte-Code file

Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the Altera Digital Library for pin-out information.

Revision History

The information contained in the *FLEX 10K Embedded Programmable Logic Device Family Data Sheet* version 4.2 supersedes information published in previous versions.

Version 4.2 Changes

The following change was made to version 4.2 of the *FLEX 10K Embedded Programmable Logic Device Family Data Sheet*: updated Figure 13.

Version 4.1 Changes

The following changes were made to version 4.1 of the *FLEX 10K Embedded Programmable Logic Device Family Data Sheet*.

- Updated General Description section
- Updated I/O Element section
- Updated SameFrame Pin-Outs section
- Updated Figure 16
- Updated Tables 13 and 116
- Added Note 9 to Table 19
- Added Note 10 to Table 24
- Added Note 10 to Table 28