

Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	624
Number of Logic Elements/Cells	4992
Total RAM Bits	24576
Number of I/O	406
Number of Gates	158000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	600-BGA
Supplier Device Package	600-BGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k100abc600-3

The FLEX 10K architecture is similar to that of embedded gate arrays, the fastest-growing segment of the gate array market. As with standard gate arrays, embedded gate arrays implement general logic in a conventional “sea-of-gates” architecture. In addition, embedded gate arrays have dedicated die areas for implementing large, specialized functions. By embedding functions in silicon, embedded gate arrays provide reduced die area and increased speed compared to standard gate arrays. However, embedded megafunctions typically cannot be customized, limiting the designer’s options. In contrast, FLEX 10K devices are programmable, providing the designer with full control over embedded megafunctions and general logic while facilitating iterative design changes during debugging.

Each FLEX 10K device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), microcontroller, wide-data-path manipulation, and data-transformation functions. The logic array performs the same function as the sea-of-gates in the gate array: it is used to implement general logic, such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

FLEX 10K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers the EPC1, EPC2, EPC16, and EPC1441 configuration devices, which configure FLEX 10K devices via a serial data stream. Configuration data can also be downloaded from system RAM or from Altera’s BitBlaster™ serial download cable or ByteBlasterMV™ parallel port download cable. After a FLEX 10K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 320 ms, real-time changes can be made during system operation.

FLEX 10K devices contain an optimized interface that permits microprocessors to configure FLEX 10K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat a FLEX 10K device as memory and configure the device by writing to a virtual memory location, making it very easy for the designer to reconfigure the device.

Logic functions are implemented by programming the EAB with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of EABs. The large capacity of EABs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or field-programmable gate array (FPGA) RAM blocks. For example, a single EAB can implement a 4×4 multiplier with eight inputs and eight outputs. Parameterized functions such as LPM functions can automatically take advantage of the EAB.

The EAB provides advantages over FPGAs, which implement on-board RAM as arrays of small, distributed RAM blocks. These FPGA RAM blocks contain delays that are less predictable as the size of the RAM increases. In addition, FPGA RAM blocks are prone to routing problems because small blocks of RAM must be connected together to make larger blocks. In contrast, EABs can be used to implement large, dedicated blocks of RAM that eliminate these timing and routing concerns.

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (\overline{WE}) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the \overline{WE} signal. In contrast, the EAB's synchronous RAM generates its own \overline{WE} signal and is self-timed with respect to the global clock. A circuit using the EAB's self-timed RAM need only meet the setup and hold time specifications of the global clock.

When used as RAM, each EAB can be configured in any of the following sizes: 256×8 , 512×4 , $1,024 \times 2$, or $2,048 \times 1$. See [Figure 2](#).

Figure 2. EAB Memory Configurations

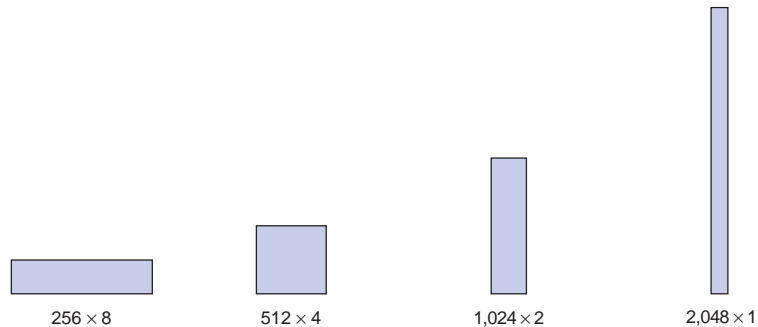
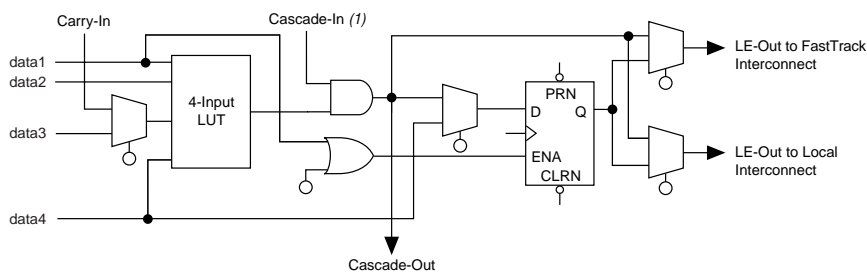
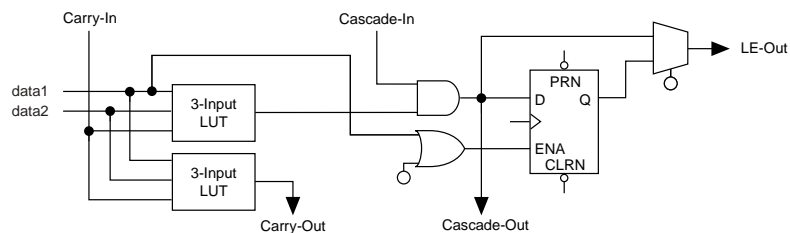


Figure 9. FLEX 10K LE Operating Modes

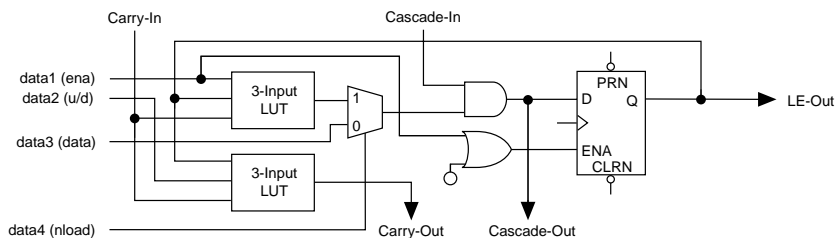
Normal Mode



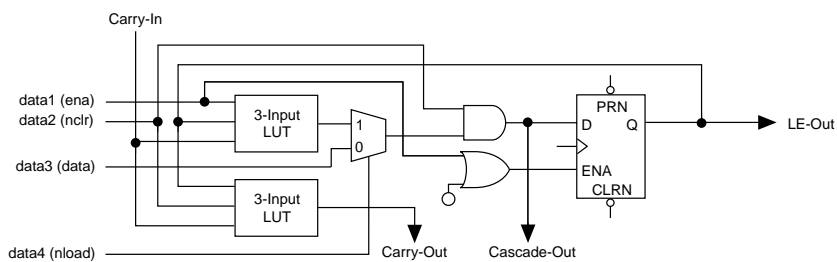
Arithmetic Mode



Up/Down Counter Mode



Clearable Counter Mode



Note:

(1) Packed registers cannot be used with the cascade chain.

Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. Either the register or the LUT can be used to drive both the local interconnect and the FastTrack Interconnect at the same time.

The LUT and the register in the LE can be used independently; this feature is known as register packing. To support register packing, the LE has two outputs; one drives the local interconnect and the other drives the FastTrack Interconnect. The DATA4 signal can drive the register directly, allowing the LUT to compute a function that is independent of the registered signal; a three-input function can be computed in the LUT, and a fourth independent signal can be registered. Alternatively, a four-input function can be generated, and one of the inputs to this function can be used to drive the register. The register in a packed LE can still use the clock enable, clear, and preset signals in the LE. In a packed LE, the register can drive the FastTrack Interconnect while the LUT drives the local interconnect, or vice versa.

Arithmetic Mode

The arithmetic mode offers 2 three-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT computes a three-input function, and the other generates a carry output. As shown in [Figure 9](#) on page 19, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three signals: a, b, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

FastTrack Interconnect

In the FLEX 10K architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, which is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect. The row interconnect can drive I/O pins and feed other LABs in the device. The column interconnect routes signals between rows and can drive I/O pins.

A row channel can be driven by an LE or by one of three column channels. These four signals feed dual 4-to-1 multiplexers that connect to two specific row channels. These multiplexers, which are connected to each LE, allow column channels to drive row channels even when all eight LEs in an LAB drive the row interconnect.

Each column of LABs is served by a dedicated column interconnect. The column interconnect can then drive I/O pins or another row's interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must be routed to the row interconnect before it can enter an LAB or EAB. Each row channel that is driven by an IOE or EAB can drive one specific column channel.

Access to row and column channels can be switched between LEs in adjacent pairs of LABs. For example, an LE in one LAB can drive the row and column channels normally driven by a particular LE in the adjacent LAB in the same row, and vice versa. This routing flexibility enables routing resources to be used more efficiently. See [Figure 11](#).

Signals on the peripheral control bus can also drive the four global signals, referred to as GLOBAL0 through GLOBAL3 in [Tables 8 and 9](#). The internally generated signal can drive the global signal, providing the same low-skew, low-delay characteristics for an internally generated signal as for a signal driven by an input. This feature is ideal for internally generated clear or clock signals with high fan-out. When a global signal is driven by internal logic, the dedicated input pin that drives that global signal cannot be used. The dedicated input pin should be driven to a known logic state (such as ground) and not be allowed to float.

When the chip-wide output enable pin is held low, it will tri-state all pins on the device. This option can be set in the Global Project Device Options menu. Additionally, the registers in the IOE can be reset by holding the chip-wide reset pin low.

Row-to-IOE Connections

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Up to eight IOEs connect to each side of each row channel. See [Figure 14](#).

Figure 14. FLEX 10K Row-to-IOE Connections

The values for m and n are provided in Table 10.

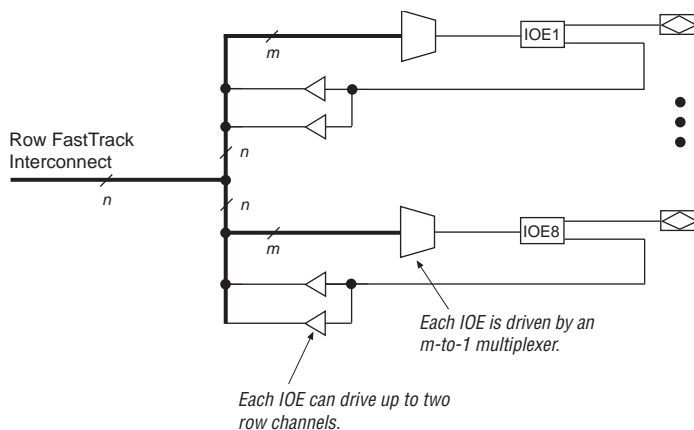


Figure 15. FLEX 10K Column-to-IOE Connections

The values for m and n are provided in Table 11.

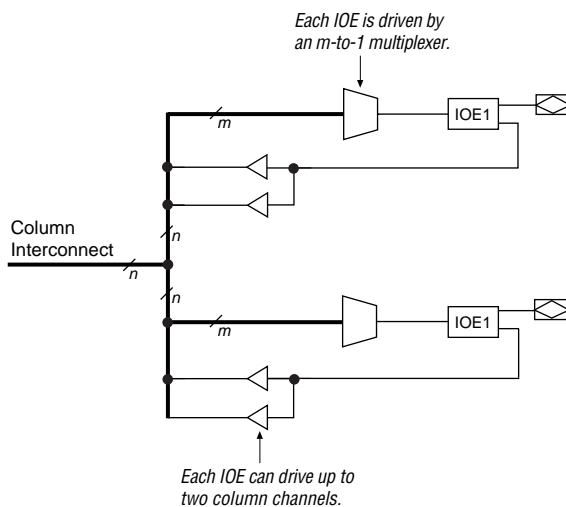


Table 11 lists the FLEX 10K column-to-IOE interconnect resources.

Table 11. FLEX 10K Column-to-IOE Interconnect Resources

Device	Channels per Column (n)	Column Channel per Pin (m)
EPF10K10 EPF10K10A	24	16
EPF10K20	24	16
EPF10K30 EPF10K30A	24	16
EPF10K40	24	16
EPF10K50 EPF10K50V	24	16
EPF10K70	24	16
EPF10K100 EPF10K100A	24	16
EPF10K130V	32	24
EPF10K250A	40	32

Table 12 describes the FLEX 10K device supply voltages and MultiVolt I/O support levels.

Table 12. Supply Voltages & MultiVolt I/O Support Levels

Devices	Supply Voltage (V)		MultiVolt I/O Support Levels (V)	
	V _{CCINT}	V _{CCIO}	Input	Output
FLEX 10K (1)	5.0	5.0	3.3 or 5.0	5.0
	5.0	3.3	3.3 or 5.0	3.3 or 5.0
EPF10K50V (1)	3.3	3.3	3.3 or 5.0	3.3 or 5.0
EPF10K130V	3.3	3.3	3.3 or 5.0	3.3 or 5.0
FLEX 10KA (1)	3.3	3.3	2.5, 3.3, or 5.0	3.3 or 5.0
	3.3	2.5	2.5, 3.3, or 5.0	2.5

Note

(1) 240-pin QFP packages do not support the MultiVolt I/O features, so they do not have separate V_{CCIO} pins.

Power Sequencing & Hot-Socketing

Because FLEX 10K devices can be used in a multi-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power supplies can be powered in any order.

Signals can be driven into FLEX 10KA devices before and during power up without damaging the device. Additionally, FLEX 10KA devices do not drive out during power up. Once operating conditions are reached, FLEX 10KA devices operate as specified by the user.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All FLEX 10K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. All FLEX 10K devices can also be configured using the JTAG pins through the BitBlaster serial download cable, or ByteBlasterMV parallel port download cable, or via hardware that uses the Jam™ programming and test language. JTAG BST can be performed before or after configuration, but not during configuration. FLEX 10K devices support the JTAG instructions shown in Table 13.

Table 27. FLEX 10KA 3.3-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.30 (2.30)	2.70 (2.70)	V
V_I	Input voltage	(5)	−0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	−40	85	° C
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 28. FLEX 10KA 3.3-V Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		1.7 or $0.5 \times V_{CCINT}$, whichever is lower		5.75	V
V_{IL}	Low-level input voltage		-0.5		$0.3 \times V_{CCINT}$	V
V_{OH}	3.3-V high-level TTL output voltage	$I_{OH} = -11$ mA DC, $V_{CCIO} = 3.00$ V (8)	2.4			V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (8)	$V_{CCIO} - 0.2$			V
	3.3-V high-level PCI output voltage	$I_{OH} = -0.5$ mA DC, $V_{CCIO} = 3.00$ to 3.60 V (8)	$0.9 \times V_{CCIO}$			V
	2.5-V high-level output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 2.30$ V (8)	2.1			V
		$I_{OH} = -1$ mA DC, $V_{CCIO} = 2.30$ V (8)	2.0			V
		$I_{OH} = -2$ mA DC, $V_{CCIO} = 2.30$ V (8)	1.7			V
V_{OL}	3.3-V low-level TTL output voltage	$I_{OL} = 9$ mA DC, $V_{CCIO} = 3.00$ V (9)			0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.00$ V (9)			0.2	V
	3.3-V low-level PCI output voltage	$I_{OL} = 1.5$ mA DC, $V_{CCIO} = 3.00$ to 3.60 V (9)			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 2.30$ V (9)			0.2	V
		$I_{OL} = 1$ mA DC, $V_{CCIO} = 2.30$ V (9)			0.4	V
		$I_{OL} = 2$ mA DC, $V_{CCIO} = 2.30$ V (9)			0.7	V
I_I	Input pin leakage current	$V_I = 5.3$ V to -0.3 V (10)	-10		10	μ A
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = 5.3$ V to -0.3 V (10)	-10		10	μ A
I_{CC0}	V_{CC} supply current (standby)	$V_I =$ ground, no load		0.3	10	mA
		$V_I =$ ground, no load (11)		10		mA

Figure 26. FLEX 10K Device IOE Timing Model

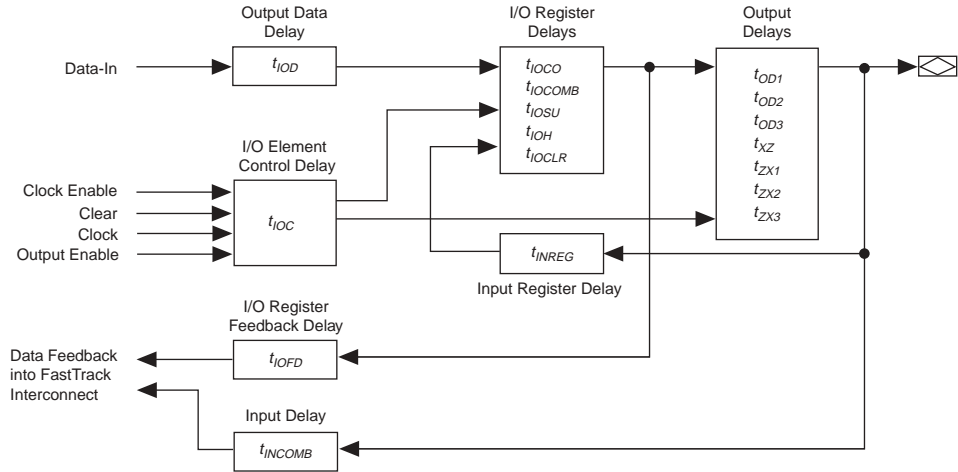


Figure 27. FLEX 10K Device EAB Timing Model

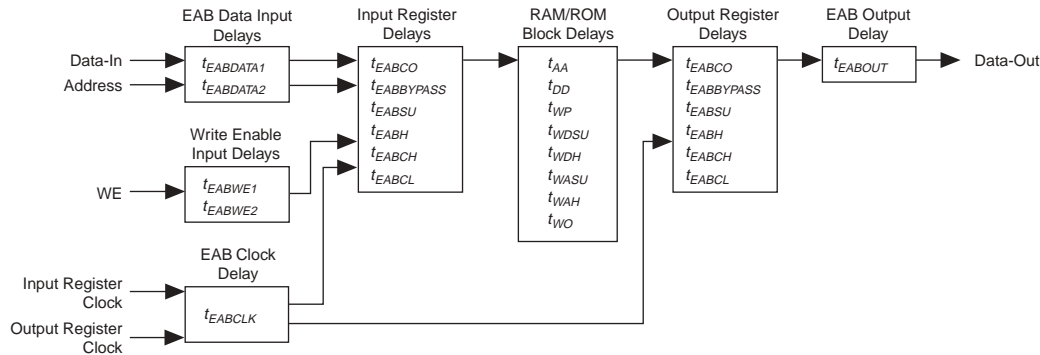


Figure 28 shows the timing model for bidirectional I/O pin timing.

Table 32. LE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions
t_{SU}	LE register setup time for data and enable signals before clock; LE register recovery time after asynchronous clear, preset, or load	
t_H	LE register hold time for data and enable signals after clock	
t_{PRE}	LE register preset delay	
t_{CLR}	LE register clear delay	
t_{CH}	Minimum clock high time from clock pin	
t_{CL}	Minimum clock low time from clock pin	

Table 33. IOE Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
t_{IOD}	IOE data delay	
t_{IOC}	IOE register control signal delay	
t_{IOCO}	IOE register clock-to-output delay	
t_{IOCOMB}	IOE combinatorial delay	
t_{IOSU}	IOE register setup time for data and enable signals before clock; IOE register recovery time after asynchronous clear	
t_{IOH}	IOE register hold time for data and enable signals after clock	
t_{IOCLR}	IOE register clear time	
t_{OD1}	Output buffer and pad delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$	C1 = 35 pF (2)
t_{OD2}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = low voltage	C1 = 35 pF (3)
t_{OD3}	Output buffer and pad delay, slow slew rate = on	C1 = 35 pF (4)
t_{XZ}	IOE output buffer disable delay	
t_{ZX1}	IOE output buffer enable delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$	C1 = 35 pF (2)
t_{ZX2}	IOE output buffer enable delay, slow slew rate = off, V_{CCIO} = low voltage	C1 = 35 pF (3)
t_{ZX3}	IOE output buffer enable delay, slow slew rate = on	C1 = 35 pF (4)
t_{INREG}	IOE input pad and buffer to IOE register delay	
t_{OFD}	IOE register feedback delay	
t_{INCOMB}	IOE input pad and buffer to FastTrack Interconnect delay	

Table 40. EPF10K10 & EPF10K20 Device IOE Timing Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{IOD}		1.3		1.6	ns
t_{IOC}		0.5		0.7	ns
t_{IOCO}		0.2		0.2	ns
t_{IOCOMB}		0.0		0.0	ns
t_{IOSU}	2.8		3.2		ns
t_{IOH}	1.0		1.2		ns
t_{IOCLR}		1.0		1.2	ns
t_{OD1}		2.6		3.5	ns
t_{OD2}		4.9		6.4	ns
t_{OD3}		6.3		8.2	ns
t_{XZ}		4.5		5.4	ns
t_{ZX1}		4.5		5.4	ns
t_{ZX2}		6.8		8.3	ns
t_{ZX3}		8.2		10.1	ns
t_{INREG}		6.0		7.5	ns
t_{IOFD}		3.1		3.5	ns
t_{INCOMB}		3.1		3.5	ns

Table 49. EPF10K30, EPF10K40 & EPF10K50 Device IOE Timing Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{IOD}		0.4		0.6	ns
t_{IOC}		0.5		0.9	ns
t_{IOCO}		0.4		0.5	ns
t_{IOCOMB}		0.0		0.0	ns
t_{IOSU}	3.1		3.5		ns
t_{IOH}	1.0		1.9		ns
t_{IOCLR}		1.0		1.2	ns
t_{OD1}		3.3		3.6	ns
t_{OD2}		5.6		6.5	ns
t_{OD3}		7.0		8.3	ns
t_{XZ}		5.2		5.5	ns
t_{ZX1}		5.2		5.5	ns
t_{ZX2}		7.5		8.4	ns
t_{ZX3}		8.9		10.2	ns
t_{INREG}		7.7		10.0	ns
t_{IOFD}		3.3		4.0	ns
t_{INCOMB}		3.3		4.0	ns

Table 59. EPF10K70 Device EAB Internal Microparameters *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.3		1.5		1.9	ns
$t_{EABDATA2}$		4.3		4.8		6.0	ns
t_{EABWE1}		0.9		1.0		1.2	ns
t_{EABWE2}		4.5		5.0		6.2	ns
t_{EABCLK}		0.9		1.0		2.2	ns
t_{EABCO}		0.4		0.5		0.6	ns
$t_{EABYPASS}$		1.3		1.5		1.9	ns
t_{EABSU}	1.3		1.5		1.8		ns
t_{EABH}	1.8		2.0		2.5		ns
t_{AA}		7.8		8.7		10.7	ns
t_{WP}	5.2		5.8		7.2		ns
t_{WDSU}	1.4		1.6		2.0		ns
t_{WDH}	0.3		0.3		0.4		ns
t_{WASU}	0.4		0.5		0.6		ns
t_{WAH}	0.9		1.0		1.2		ns
t_{WO}		4.5		5.0		6.2	ns
t_{DD}		4.5		5.0		6.2	ns
t_{EABOUT}		0.4		0.5		0.6	ns
t_{EABCH}	4.0		4.0		4.0		ns
t_{EABCL}	5.2		5.8		7.2		ns

Notes to tables:

- (1) All timing parameters are described in Tables 32 through 38 in this data sheet.
- (2) Using an LE to register the signal may provide a lower setup time.
- (3) This parameter is specified by characterization.

Tables 85 through 91 show EPF10K10A device internal and external timing parameters.

Table 85. EPF10K10A Device LE Timing Microparameters <i>Note (1)</i>							
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.9		1.2		1.6	ns
t_{CLUT}		1.2		1.4		1.9	ns
t_{RLUT}		1.9		2.3		3.0	ns
t_{PACKED}		0.6		0.7		0.9	ns
t_{EN}		0.5		0.6		0.8	ns
t_{CICO}		0.2		0.3		0.4	ns
t_{CGEN}		0.7		0.9		1.1	ns
t_{CGENR}		0.7		0.9		1.1	ns
t_{CASC}		1.0		1.2		1.7	ns
t_C		1.2		1.4		1.9	ns
t_{CO}		0.5		0.6		0.8	ns
t_{COMB}		0.5		0.6		0.8	ns
t_{SU}	1.1		1.3		1.7		ns
t_H	0.6		0.7		0.9		ns
t_{PRE}		0.5		0.6		0.9	ns
t_{CLR}		0.5		0.6		0.9	ns
t_{CH}	3.0		3.5		4.0		ns
t_{CL}	3.0		3.5		4.0		ns

Table 86. EPF10K10A Device IOE Timing Microparameters <i>Note (1) (Part 1 of 2)</i>							
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
		1.3		1.5		2.0	ns
t_{IOC}		0.2		0.3		0.3	ns
t_{IOCO}		0.2		0.3		0.4	ns
t_{IOCOMB}		0.6		0.7		0.9	ns
t_{IOSU}	0.8		1.0		1.3		ns

Table 87. EPF10K10A Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		3.3		3.9		5.2	ns
$t_{EABDATA2}$		1.0		1.3		1.7	ns
t_{EABWE1}		2.6		3.1		4.1	ns
t_{EABWE2}		2.7		3.2		4.3	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		1.2		1.4		1.8	ns
$t_{EABYPASS}$		0.1		0.2		0.2	ns
t_{EABSU}	1.4		1.7		2.2		ns
t_{EABH}	0.1		0.1		0.1		ns
t_{AA}		4.5		5.4		7.3	ns
t_{WP}	2.0		2.4		3.2		ns
t_{WDSU}	0.7		0.8		1.1		ns
t_{WDH}	0.5		0.6		0.7		ns
t_{WASU}	0.6		0.7		0.9		ns
t_{WAH}	0.9		1.1		1.5		ns
t_{WO}		3.3		3.9		5.2	ns
t_{DD}		3.3		3.9		5.2	ns
t_{EABOUT}		0.1		0.1		0.2	ns
t_{EABCH}	3.0		3.5		4.0		ns
t_{EABCL}	3.03		3.5		4.0		ns

Notes to tables:

- (1) All timing parameters are described in Tables 32 through 38 in this data sheet.
- (2) Using an LE to register the signal may provide a lower setup time.
- (3) This parameter is specified by characterization.

Tables 92 through 98 show EPF10K30A device internal and external timing parameters.

Table 92. EPF10K30A Device LE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.8		1.1		1.5	ns
t_{CLUT}		0.6		0.7		1.0	ns
t_{RLUT}		1.2		1.5		2.0	ns
t_{PACKED}		0.6		0.6		1.0	ns
t_{EN}		1.3		1.5		2.0	ns
t_{CICO}		0.2		0.3		0.4	ns
t_{CGEN}		0.8		1.0		1.3	ns
t_{CGENR}		0.6		0.8		1.0	ns
t_{CASC}		0.9		1.1		1.4	ns
t_C		1.1		1.3		1.7	ns
t_{CO}		0.4		0.6		0.7	ns
t_{COMB}		0.6		0.7		0.9	ns
t_{SU}	0.9		0.9		1.4		ns
t_H	1.1		1.3		1.7		ns
t_{PRE}		0.5		0.6		0.8	ns
t_{CLR}		0.5		0.6		0.8	ns
t_{CH}	3.0		3.5		4.0		ns
t_{CL}	3.0		3.5		4.0		ns

Table 93. EPF10K30A Device IOE Timing Microparameters *Note (1) (Part 1 of 2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{IOD}		2.2		2.6		3.4	ns
t_{IOC}		0.3		0.3		0.5	ns
t_{IOCO}		0.2		0.2		0.3	ns
t_{IOCOMB}		0.5		0.6		0.8	ns
t_{IOSU}	1.4		1.7		2.2		ns

Table 113. ClockLock & ClockBoost Parameters (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
$f_{CLKDEV1}$	Input deviation from user specification in MAX+PLUS II (ClockBoost clock multiplication factor equals 1) (1)			± 1	MHz
$f_{CLKDEV2}$	Input deviation from user specification in MAX+PLUS II (ClockBoost clock multiplication factor equals 2) (1)			± 0.5	MHz
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)			100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock (2)			10	μ s
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock (3)			1	ns
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock	40	50	60	%

Notes:

- (1) To implement the ClockLock and ClockBoost circuitry with the MAX+PLUS II software, designers must specify the input frequency. The MAX+PLUS II software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The f_{CLKDEV} parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.
- (2) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the t_{LOCK} value is less than the time required for configuration.
- (3) The t_{JITTER} specification is measured under long-term observation.

Power Consumption

The supply power (P) for FLEX 10K devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

Typical $I_{CCSTANDBY}$ values are shown as I_{CC0} in the FLEX 10K device DC operating conditions tables on pages 46, 49, and 52 of this data sheet. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value is calculated based on the amount of current that each LE typically consumes. The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.



Compared to the rest of the device, the embedded array consumes a negligible amount of power. Therefore, the embedded array can be ignored when calculating supply current.

The $I_{CCACTIVE}$ value is calculated with the following equation:

$$I_{CCACTIVE} = K \times f_{MAX} \times N \times \text{tog}_{LC} \times \frac{\mu A}{\text{MHz} \times LE}$$

The parameters in this equation are shown below:

Figure 32. *I_{CCACTIVE}* vs. Operating Frequency (Part 1 of 3)

