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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	624
Number of Logic Elements/Cells	4992
Total RAM Bits	24576
Number of I/O	406
Number of Gates	158000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	600-BGA
Supplier Device Package	600-BGA (45x45)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epf10k100abi600-2">https://www.e-xfl.com/product-detail/intel/epf10k100abi600-2</a>

The FLEX 10K architecture is similar to that of embedded gate arrays, the fastest-growing segment of the gate array market. As with standard gate arrays, embedded gate arrays implement general logic in a conventional “sea-of-gates” architecture. In addition, embedded gate arrays have dedicated die areas for implementing large, specialized functions. By embedding functions in silicon, embedded gate arrays provide reduced die area and increased speed compared to standard gate arrays. However, embedded megafunctions typically cannot be customized, limiting the designer’s options. In contrast, FLEX 10K devices are programmable, providing the designer with full control over embedded megafunctions and general logic while facilitating iterative design changes during debugging.

Each FLEX 10K device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), microcontroller, wide-data-path manipulation, and data-transformation functions. The logic array performs the same function as the sea-of-gates in the gate array: it is used to implement general logic, such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

FLEX 10K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers the EPC1, EPC2, EPC16, and EPC1441 configuration devices, which configure FLEX 10K devices via a serial data stream. Configuration data can also be downloaded from system RAM or from Altera’s BitBlaster™ serial download cable or ByteBlasterMV™ parallel port download cable. After a FLEX 10K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 320 ms, real-time changes can be made during system operation.

FLEX 10K devices contain an optimized interface that permits microprocessors to configure FLEX 10K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat a FLEX 10K device as memory and configure the device by writing to a virtual memory location, making it very easy for the designer to reconfigure the device.



For more information, see the following documents:

- *Configuration Devices for APEX & FLEX Devices Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Application Note 116 (Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices)*

FLEX 10K devices are supported by Altera development systems; single, integrated packages that offer schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The Altera software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Altera software works easily with common gate array EDA tools for synthesis and simulation. For example, the Altera software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Altera software contains EDA libraries that use device-specific features such as carry chains which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Altera development systems include DesignWare functions that are optimized for the FLEX 10K architecture.

The Altera development systems run on Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations.



See the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* for more information.

## Functional Description

Each FLEX 10K device contains an embedded array to implement memory and specialized logic functions, and a logic array to implement general logic.

The embedded array consists of a series of EABs. When implementing memory functions, each EAB provides 2,048 bits, which can be used to create RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. When implementing logic, each EAB can contribute 100 to 600 gates towards complex logic functions, such as multipliers, microcontrollers, state machines, and DSP functions. EABs can be used independently, or multiple EABs can be combined to implement larger functions.

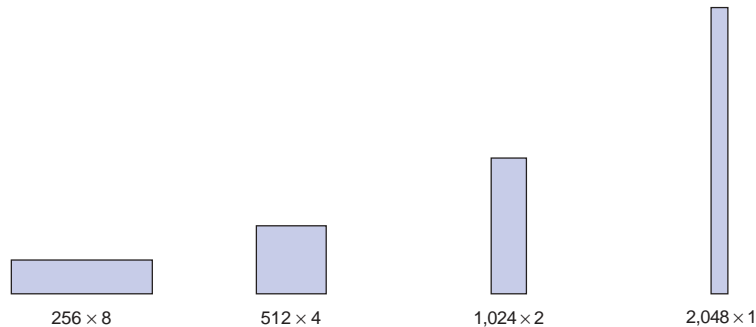
Logic functions are implemented by programming the EAB with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of EABs. The large capacity of EABs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or field-programmable gate array (FPGA) RAM blocks. For example, a single EAB can implement a  $4 \times 4$  multiplier with eight inputs and eight outputs. Parameterized functions such as LPM functions can automatically take advantage of the EAB.

The EAB provides advantages over FPGAs, which implement on-board RAM as arrays of small, distributed RAM blocks. These FPGA RAM blocks contain delays that are less predictable as the size of the RAM increases. In addition, FPGA RAM blocks are prone to routing problems because small blocks of RAM must be connected together to make larger blocks. In contrast, EABs can be used to implement large, dedicated blocks of RAM that eliminate these timing and routing concerns.

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the EAB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. A circuit using the EAB's self-timed RAM need only meet the setup and hold time specifications of the global clock.

When used as RAM, each EAB can be configured in any of the following sizes:  $256 \times 8$ ,  $512 \times 4$ ,  $1,024 \times 2$ , or  $2,048 \times 1$ . See [Figure 2](#).

**Figure 2. EAB Memory Configurations**



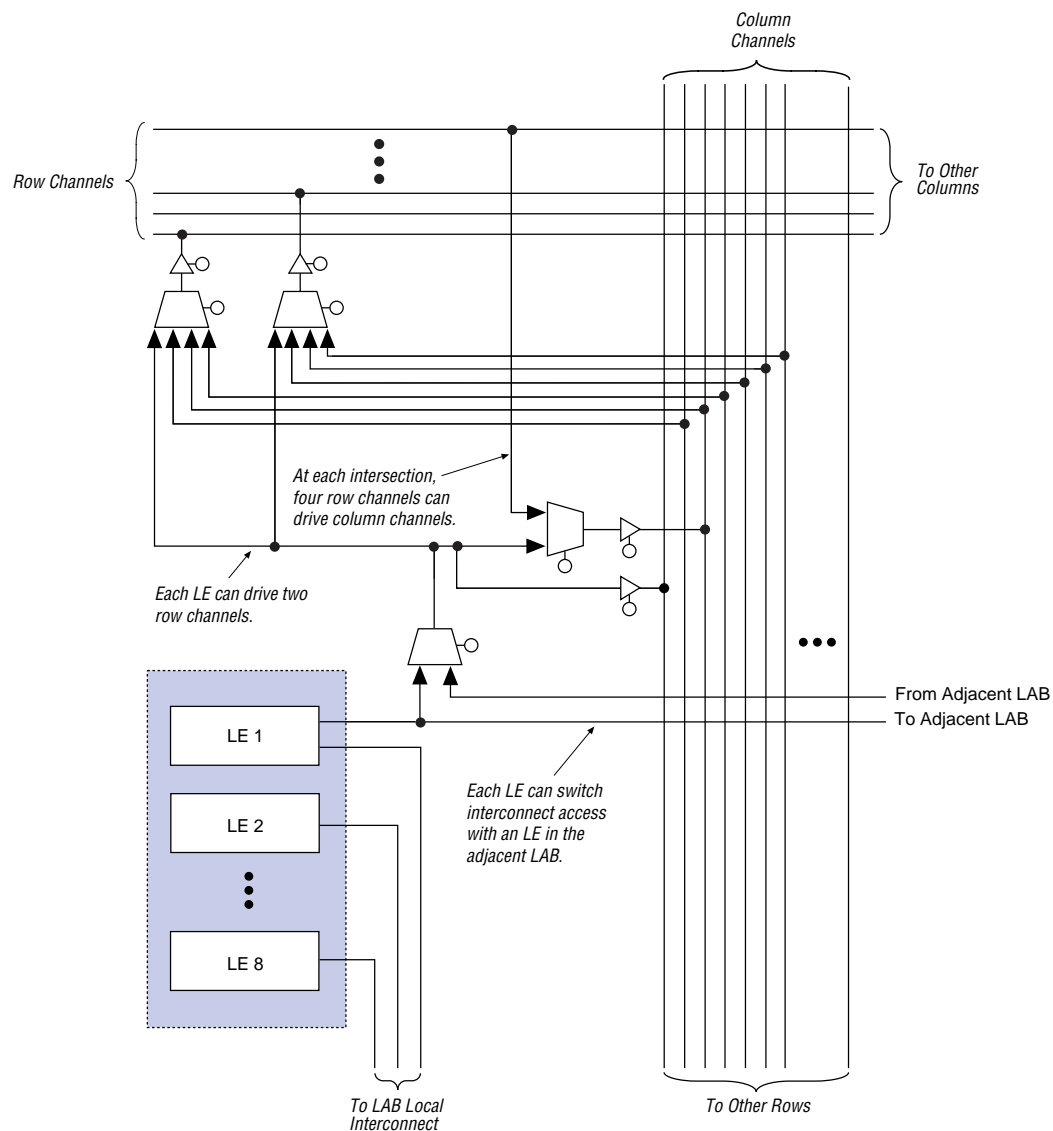
During compilation, the Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six modes chosen during design entry:

- Asynchronous clear
- Asynchronous preset
- Asynchronous clear and preset
- Asynchronous load with clear
- Asynchronous load with preset
- Asynchronous load without clear or preset

In addition to the six clear and preset modes, FLEX 10K devices provide a chip-wide reset pin that can reset all registers in the device. Use of this feature is set during design entry. In any of the clear and preset modes, the chip-wide reset overrides all other signals. Registers with asynchronous presets may be preset when the chip-wide reset is asserted. Inversion can be used to implement the asynchronous preset. [Figure 10](#) shows examples of how to enter a section of a design for the desired functionality.

**Figure 11. LAB Connections to Row & Column Interconnect**

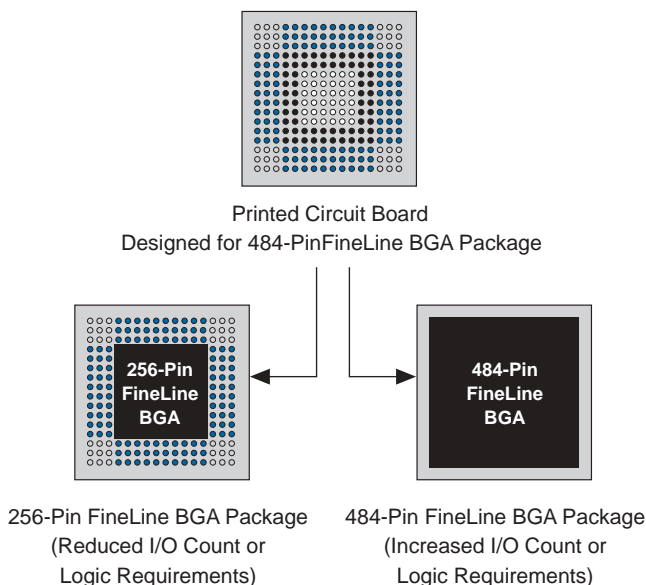


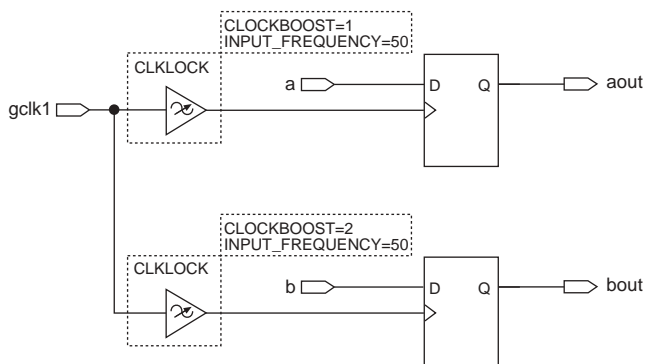
## SameFrame Pin-Outs

FLEX 10KE devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPF10K10A device in a 256-pin FineLine BGA package to an EPF10K100A device in a 484-pin FineLine BGA package.

The Altera software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software generates pin-outs describing how to lay out a board to take advantage of this migration (see [Figure 16](#)).

**Figure 16. SameFrame Pin-Out Example**



**Figure 17. Enabling ClockLock & ClockBoost in the Same Design**

To use both the ClockLock and ClockBoost circuits in the same design, designers must use Revision C EPF10K100GC503-3DX devices and MAX+PLUS II software versions 7.2 or higher. The die revision is indicated by the third digit of the nine-digit code on the top side of the device.

## Output Configuration

This section discusses the peripheral component interconnect (PCI) pull-up clamping diode option, slew-rate control, open-drain output option, MultiVolt I/O interface, and power sequencing for FLEX 10K devices. The PCI pull-up clamping diode, slew-rate control, and open-drain output options are controlled pin-by-pin via Altera logic options. The MultiVolt I/O interface is controlled by connecting  $V_{CCIO}$  to a different voltage than  $V_{CCINT}$ . Its effect can be simulated in the Altera software via the **Global Project Device Options** dialog box (Assign menu).

### PCI Clamping Diodes

The EPF10K10A and EPF10K30A devices have a pull-up clamping diode on every I/O, dedicated input, and dedicated clock pin. PCI clamping diodes clamp the transient overshoot caused by reflected waves to the  $V_{CCIO}$  value and are required for 3.3-V PCI compliance. Clamping diodes can also be used to limit overshoot in other systems.

Clamping diodes are controlled on a pin-by-pin basis via a logic option in the Altera software. When  $V_{CCIO}$  is 3.3 V, a pin that has the clamping diode turned on can be driven by a 2.5-V or 3.3-V signal, but not a 5.0-V signal. When  $V_{CCIO}$  is 2.5 V, a pin that has the clamping diode turned on can be driven by a 2.5-V signal, but not a 3.3-V or 5.0-V signal. However, a clamping diode can be turned on for a subset of pins, which allows devices to bridge between a 3.3-V PCI bus and a 5.0-V device.



**Table 19. FLEX 10K 5.0-V Device DC Operating Conditions** Notes (5), (6)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IH}$	High-level input voltage		2.0		$V_{CCINT} + 0.5$	V
$V_{IL}$	Low-level input voltage		-0.5		0.8	V
$V_{OH}$	5.0-V high-level TTL output voltage	$I_{OH} = -4$ mA DC, $V_{CCIO} = 4.75$ V (7)	2.4			V
	3.3-V high-level TTL output voltage	$I_{OH} = -4$ mA DC, $V_{CCIO} = 3.00$ V (7)	2.4			V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (7)	$V_{CCIO} - 0.2$			V
$V_{OL}$	5.0-V low-level TTL output voltage	$I_{OL} = 12$ mA DC, $V_{CCIO} = 4.75$ V (8)			0.45	V
	3.3-V low-level TTL output voltage	$I_{OL} = 12$ mA DC, $V_{CCIO} = 3.00$ V (8)			0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.00$ V (8)			0.2	V
$I_I$	Input pin leakage current	$V_I = V_{CC}$ or ground (9)	-10		10	$\mu$ A
$I_{OZ}$	Tri-stated I/O pin leakage current	$V_O = V_{CC}$ or ground (9)	-40		40	$\mu$ A
$I_{CC0}$	$V_{CC}$ supply current (standby)	$V_I =$ ground, no load		0.5	10	mA

**Table 20. 5.0-V Device Capacitance of EPF10K10, EPF10K20 & EPF10K30 Devices** Note (10)

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		8	pF
$C_{INCLK}$	Input capacitance on dedicated clock pin	$V_{IN} = 0$ V, $f = 1.0$ MHz		12	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		8	pF

**Table 21. 5.0-V Device Capacitance of EPF10K40, EPF10K50, EPF10K70 & EPF10K100 Devices** Note (10)

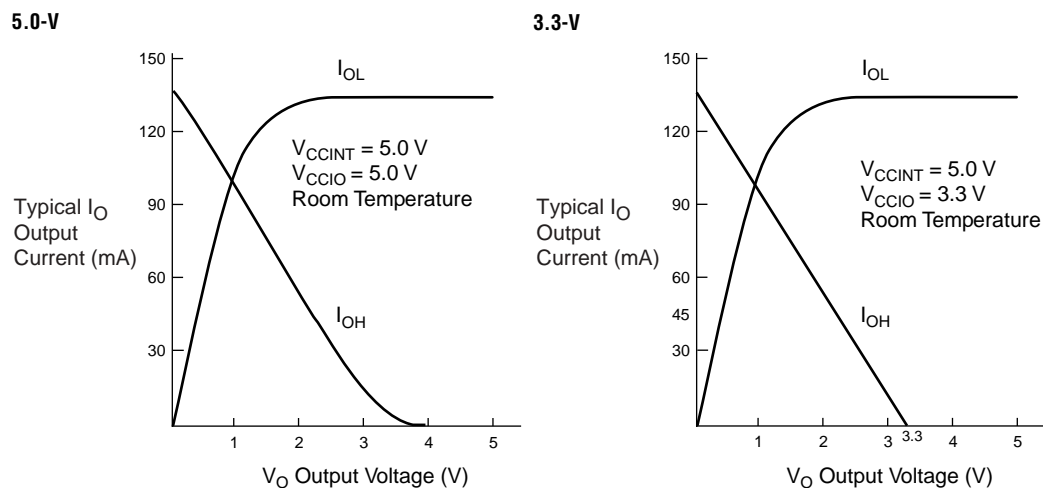
Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		10	pF
$C_{INCLK}$	Input capacitance on dedicated clock pin	$V_{IN} = 0$ V, $f = 1.0$ MHz		15	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		10	pF

**Notes to tables:**

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input voltage is  $-0.5$  V. During transitions, the inputs may undershoot to  $-2.0$  V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum  $V_{CC}$  rise time is 100 ms.  $V_{CC}$  must rise monotonically.
- (5) Typical values are for  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5.0$  V.
- (6) These values are specified under the Recommended Operation Condition shown in Table 18 on page 45.
- (7) The  $I_{OH}$  parameter refers to high-level TTL or CMOS output current.
- (8) The  $I_{OL}$  parameter refers to low-level TTL or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (9) This value is specified for normal device operation. The value may vary during power-up.
- (10) Capacitance is sample-tested only.

Figure 20 shows the typical output drive characteristics of FLEX 10K devices with 5.0-V and 3.3-V  $V_{CCIO}$ . The output driver is compliant with the 5.0-V *PCI Local Bus Specification, Revision 2.2* (for 5.0-V  $V_{CCIO}$ ).

**Figure 20. Output Drive Characteristics of FLEX 10K Devices**



**Table 24. EPF10K50V & EPF10K130V Device DC Operating Conditions** Notes (6), (7)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IH}$	High-level input voltage		2.0		5.75	V
$V_{IL}$	Low-level input voltage		-0.5		0.8	V
$V_{OH}$	3.3-V high-level TTL output voltage	$I_{OH} = -8$ mA DC (8)	2.4			V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC (8)	$V_{CCIO} - 0.2$			V
$V_{OL}$	3.3-V low-level TTL output voltage	$I_{OL} = 8$ mA DC (9)			0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC (9)			0.2	V
$I_I$	Input pin leakage current	$V_I = 5.3$ V to $-0.3$ V (10)	-10		10	$\mu$ A
$I_{OZ}$	Tri-stated I/O pin leakage current	$V_O = 5.3$ V to $-0.3$ V (10)	-10		10	$\mu$ A
$I_{CC0}$	$V_{CC}$ supply current (standby)	$V_I =$ ground, no load		0.3	10	mA
		$V_I =$ ground, no load (11)		10		mA

**Table 25. EPF10K50V & EPF10K130V Device Capacitance** (12)

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		10	pF
$C_{INCLK}$	Input capacitance on dedicated clock pin	$V_{IN} = 0$ V, $f = 1.0$ MHz		15	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		10	pF

**Notes to tables:**

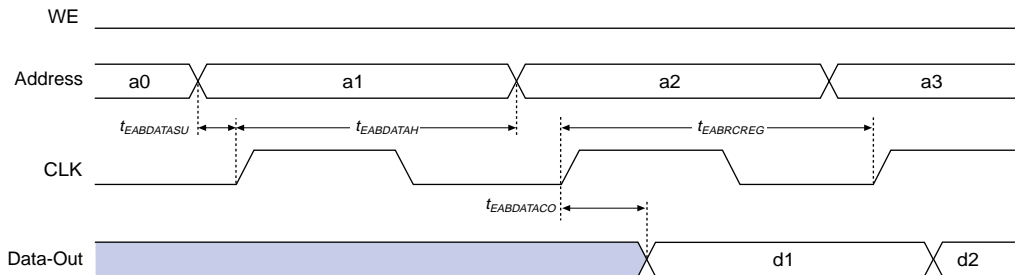
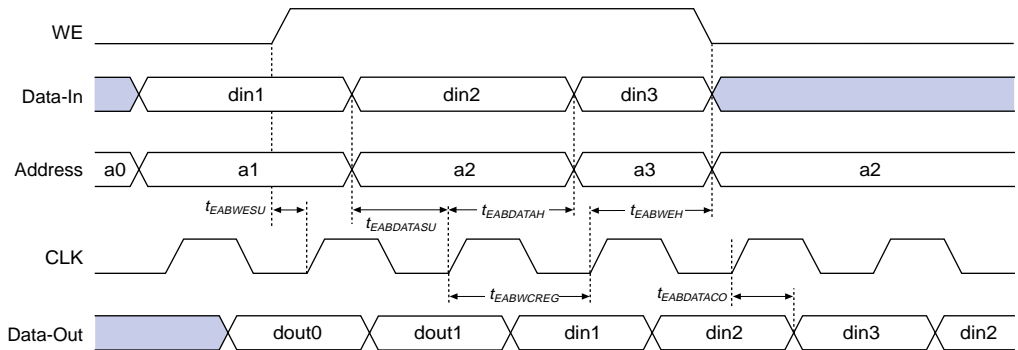
- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input voltage is  $-0.5$  V. During transitions, the inputs may undershoot to  $-2.0$  V or overshoot to  $5.75$  V for input currents less than  $100$  mA and periods shorter than  $20$  ns.
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum  $V_{CC}$  rise time is  $100$  ms.  $V_{CC}$  must rise monotonically.
- (5) EPF10K50V and EPF10K130V device inputs may be driven before  $V_{CCINT}$  and  $V_{CCIO}$  are powered.
- (6) Typical values are for  $T_A = 25^\circ$  C and  $V_{CC} = 3.3$  V.
- (7) These values are specified under the EPF10K50V and EPF10K130V device Recommended Operating Conditions in Table 23 on page 48.
- (8) The  $I_{OH}$  parameter refers to high-level TTL or CMOS output current.
- (9) The  $I_{OL}$  parameter refers to low-level TTL or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (10) This value is specified for normal device operation. The value may vary during power-up.
- (11) This parameter applies to -1 speed grade EPF10K50V devices, -2 speed grade EPF10K50V industrial temperature devices, and -2 speed grade EPF10K130V devices.
- (12) Capacitance is sample-tested only.

**Table 27. FLEX 10KA 3.3-V Device Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage for internal logic and input buffers	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
$V_{CCIO}$	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.30 (2.30)	2.70 (2.70)	V
$V_I$	Input voltage	(5)	−0.5	5.75	V
$V_O$	Output voltage		0	$V_{CCIO}$	V
$T_A$	Ambient temperature	For commercial use	0	70	° C
		For industrial use	−40	85	° C
$T_J$	Operating temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
$t_R$	Input rise time			40	ns
$t_F$	Input fall time			40	ns

**Table 34. EAB Timing Microparameters** *Note (1)*

Symbol	Parameter	Conditions
$t_{EABDATA1}$	Data or address delay to EAB for combinatorial input	
$t_{EABDATA2}$	Data or address delay to EAB for registered input	
$t_{EABWE1}$	Write enable delay to EAB for combinatorial input	
$t_{EABWE2}$	Write enable delay to EAB for registered input	
$t_{EABCLK}$	EAB register clock delay	
$t_{EABCO}$	EAB register clock-to-output delay	
$t_{EABYPASS}$	Bypass register delay	
$t_{EABSU}$	EAB register setup time before clock	
$t_{EABH}$	EAB register hold time after clock	
$t_{AA}$	Address access delay	
$t_{WP}$	Write pulse width	
$t_{WDSU}$	Data setup time before falling edge of write pulse	(5)
$t_{WDH}$	Data hold time after falling edge of write pulse	(5)
$t_{WASU}$	Address setup time before rising edge of write pulse	(5)
$t_{WAH}$	Address hold time after falling edge of write pulse	(5)
$t_{WO}$	Write enable to data output valid delay	
$t_{DD}$	Data-in to data-out valid delay	
$t_{EABOUT}$	Data-out delay	
$t_{EABCH}$	Clock high time	
$t_{EABCL}$	Clock low time	

**Figure 30. EAB Synchronous Timing Waveforms****EAB Synchronous Read****EAB Synchronous Write (EAB Output Registers Used)**

## Notes to tables:

- (1) All timing parameters are described in Tables 32 through 38 in this data sheet.
- (2) Using an LE to register the signal may provide a lower setup time.
- (3) This parameter is specified by characterization.

Tables 57 through 63 show EPF10K70 device internal and external timing parameters.

**Table 57. EPF10K70 Device LE Timing Microparameters** *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{LUT}$		1.3		1.5		2.0	ns
$t_{CLUT}$		0.4		0.4		0.5	ns
$t_{RLUT}$		1.5		1.6		2.0	ns
$t_{PACKED}$		0.8		0.9		1.3	ns
$t_{EN}$		0.8		0.9		1.2	ns
$t_{CICO}$		0.2		0.2		0.3	ns
$t_{CGEN}$		1.0		1.1		1.4	ns
$t_{CGENR}$		1.1		1.2		1.5	ns
$t_{CASC}$		1.0		1.1		1.3	ns
$t_C$		0.7		0.8		1.0	ns
$t_{CO}$		0.9		1.0		1.4	ns
$t_{COMB}$		0.4		0.5		0.7	ns
$t_{SU}$	1.9		2.1		2.6		ns
$t_H$	2.1		2.3		3.1		ns
$t_{PRE}$		0.9		1.0		1.4	ns
$t_{CLR}$		0.9		1.0		1.4	ns
$t_{CH}$	4.0		4.0		4.0		ns
$t_{CL}$	4.0		4.0		4.0		ns

**Table 61. EPF10K70 Device Interconnect Timing Microparameters** *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		6.6		7.3		8.8	ns
$t_{DIN2LE}$		4.2		4.8		6.0	ns
$t_{DIN2DATA}$		6.5		7.1		10.8	ns
$t_{DCLK2IOE}$		5.5		6.2		7.7	ns
$t_{DCLK2LE}$		4.2		4.8		6.0	ns
$t_{SAMELAB}$		0.4		0.4		0.5	ns
$t_{SAMEROW}$		4.8		4.9		5.5	ns
$t_{SAMECOLUMN}$		3.3		3.4		3.7	ns
$t_{DIFFROW}$		8.1		8.3		9.2	ns
$t_{TWOROWS}$		12.9		13.2		14.7	ns
$t_{LEPERIPH}$		5.5		5.7		6.5	ns
$t_{LABCARRY}$		0.8		0.9		1.1	ns
$t_{LABCASC}$		2.7		3.0		3.2	ns

**Table 62. EPF10K70 Device External Timing Parameters** *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DRR}$		17.2		19.1		24.2	ns
$t_{INSU}$ (2), (3)	6.6		7.3		8.0		ns
$t_{INH}$ (3)	0.0		0.0		0.0		ns
$t_{OUTCO}$ (3)	2.0	9.9	2.0	11.1	2.0	14.3	ns

**Table 63. EPF10K70 Device External Bidirectional Timing Parameters** *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	7.4		8.1		10.4		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	9.9	2.0	11.1	2.0	14.3	ns
$t_{XZBIDIR}$		13.7		15.4		18.5	ns
$t_{ZXBIDIR}$		13.7		15.4		18.5	ns



**Notes to tables:**

- (1) All timing parameters are described in Tables 32 through 38 in this data sheet.
- (2) Using an LE to register the signal may provide a lower setup time.
- (3) This parameter is specified by characterization.

Tables 85 through 91 show EPF10K10A device internal and external timing parameters.

<b>Table 85. EPF10K10A Device LE Timing Microparameters</b> <i>Note (1)</i>							
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{LUT}$		0.9		1.2		1.6	ns
$t_{CLUT}$		1.2		1.4		1.9	ns
$t_{RLUT}$		1.9		2.3		3.0	ns
$t_{PACKED}$		0.6		0.7		0.9	ns
$t_{EN}$		0.5		0.6		0.8	ns
$t_{CICO}$		0.2		0.3		0.4	ns
$t_{CGEN}$		0.7		0.9		1.1	ns
$t_{CGENR}$		0.7		0.9		1.1	ns
$t_{CASC}$		1.0		1.2		1.7	ns
$t_C$		1.2		1.4		1.9	ns
$t_{CO}$		0.5		0.6		0.8	ns
$t_{COMB}$		0.5		0.6		0.8	ns
$t_{SU}$	1.1		1.3		1.7		ns
$t_H$	0.6		0.7		0.9		ns
$t_{PRE}$		0.5		0.6		0.9	ns
$t_{CLR}$		0.5		0.6		0.9	ns
$t_{CH}$	3.0		3.5		4.0		ns
$t_{CL}$	3.0		3.5		4.0		ns

<b>Table 86. EPF10K10A Device IOE Timing Microparameters</b> <i>Note (1) (Part 1 of 2)</i>							
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
		1.3		1.5		2.0	ns
$t_{IOC}$		0.2		0.3		0.3	ns
$t_{IOCO}$		0.2		0.3		0.4	ns
$t_{IOCOMB}$		0.6		0.7		0.9	ns
$t_{IOSU}$	0.8		1.0		1.3		ns

**Table 103. EPF10K100A Device Interconnect Timing Microparameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		4.8		5.4		6.0	ns
$t_{DIN2LE}$		2.0		2.4		2.7	ns
$t_{DIN2DATA}$		2.4		2.7		2.9	ns
$t_{DCLK2IOE}$		2.6		3.0		3.5	ns
$t_{DCLK2LE}$		2.0		2.4		2.7	ns
$t_{SAMELAB}$		0.1		0.1		0.1	ns
$t_{SAMEROW}$		1.5		1.7		1.9	ns
$t_{SAMECOLUMN}$		5.5		6.5		7.4	ns
$t_{DIFFROW}$		7.0		8.2		9.3	ns
$t_{TWOROWS}$		8.5		9.9		11.2	ns
$t_{LEPERIPH}$		3.9		4.2		4.5	ns
$t_{LABCARRY}$		0.2		0.2		0.3	ns
$t_{LABCASC}$		0.4		0.5		0.6	ns

**Table 104. EPF10K100A Device External Timing Parameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DRR}$		12.5		14.5		17.0	ns
$t_{INSU}$ (2), (3)	3.7		4.5		5.1		ns
$t_{INH}$ (3)	0.0		0.0		0.0		ns
$t_{OUTCO}$ (3)	2.0	5.3	2.0	6.1	2.0	7.2	ns

**Table 105. EPF10K100A Device External Bidirectional Timing Parameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	4.9		5.8		6.8		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	5.3	2.0	6.1	2.0	7.2	ns
$t_{XZBIDIR}$		7.4		8.6		10.1	ns
$t_{ZXBIDIR}$		7.4		8.6		10.1	ns

- $f_{\text{MAX}}$  = Maximum operating frequency in MHz  
 $N$  = Total number of logic cells used in the device  
 $\text{tog}_{\text{LC}}$  = Average percent of logic cells toggling at each clock (typically 12.5%)  
 $K$  = Constant, shown in [Tables 114 and 115](#)

**Table 114. FLEX 10K K Constant Values**

Device	K Value
EPF10K10	82
EPF10K20	89
EPF10K30	88
EPF10K40	92
EPF10K50	95
EPF10K70	85
EPF10K100	88

**Table 115. FLEX 10KA K Constant Values**

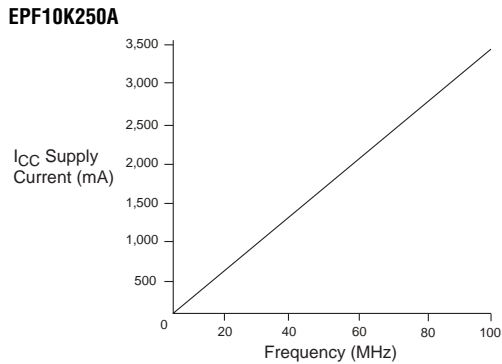
Device	K Value
EPF10K10A	17
EPF10K30A	17
EPF10K50V	19
EPF10K100A	19
EPF10K130V	22
EPF10K250A	23

This calculation provides an  $I_{\text{CC}}$  estimate based on typical conditions with no output load. The actual  $I_{\text{CC}}$  should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

To better reflect actual designs, the power model (and the constant  $K$  in the power calculation equations) for continuous interconnect FLEX devices assumes that logic cells drive FastTrack Interconnect channels. In contrast, the power model of segmented FPGAs assumes that all logic cells drive only one short interconnect segment. This assumption may lead to inaccurate results, compared to measured power consumption for an actual design in a segmented interconnect FPGA.

[Figure 32](#) shows the relationship between the current and operating frequency of FLEX 10K devices.

**Figure 32.  $I_{CCACTIVE}$  vs. Operating Frequency (Part 3 of 3)**



# Configuration & Operation



The FLEX 10K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

See *Application Note 116 (Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices)* for detailed descriptions of device configuration options, device configuration pins, and for information on configuring FLEX 10K devices, including sample schematics, timing diagrams, and configuration parameters.

## Operating Modes

The FLEX 10K architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. The process of physically loading the SRAM data into the device is called *configuration*. Before configuration, as VCC rises, the device initiates a Power-On Reset (POR). This POR event clears the device and prepares it for configuration. The FLEX 10K POR time does not exceed 50  $\mu$ s.

During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.



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