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Understanding Embedded - FPGAs (Field Programmable Gate Array)

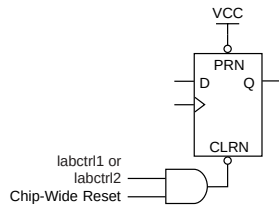
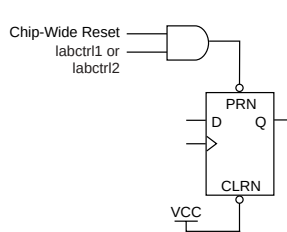
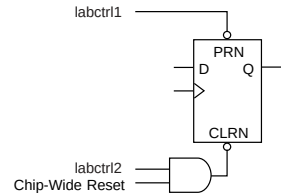
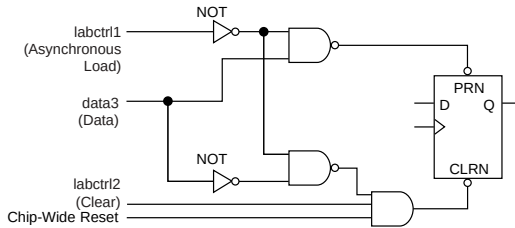
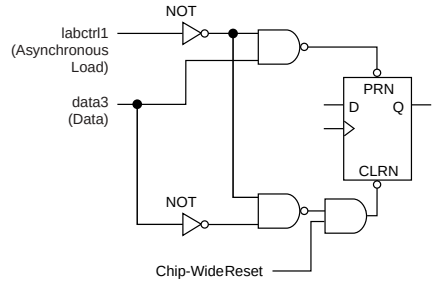
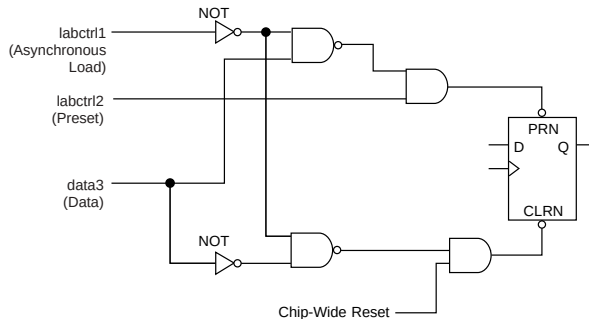
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	144
Number of Logic Elements/Cells	1152
Total RAM Bits	12288
Number of I/O	147
Number of Gates	63000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP Exposed Pad
Supplier Device Package	208-RQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k20rc208-3n

Figure 10. LE Clear & Preset Modes**Asynchronous Clear****Asynchronous Preset****Asynchronous Clear & Preset****Asynchronous Load with Clear****Asynchronous Load without Clear or Preset****Asynchronous Load with Preset****Asynchronous Clear**

The flipflop can be cleared by either LABCTRL1 or LABCTRL2. In this mode, the preset signal is tied to V_{CC} to deactivate it.

Figure 12 shows the interconnection of adjacent LABs and EABs with row, column, and local interconnects, as well as the associated cascade and carry chains. Each LAB is labeled according to its location: a letter represents the row and a number represents the column. For example, LAB B3 is in row B, column 3.

Figure 12. Interconnect Resources

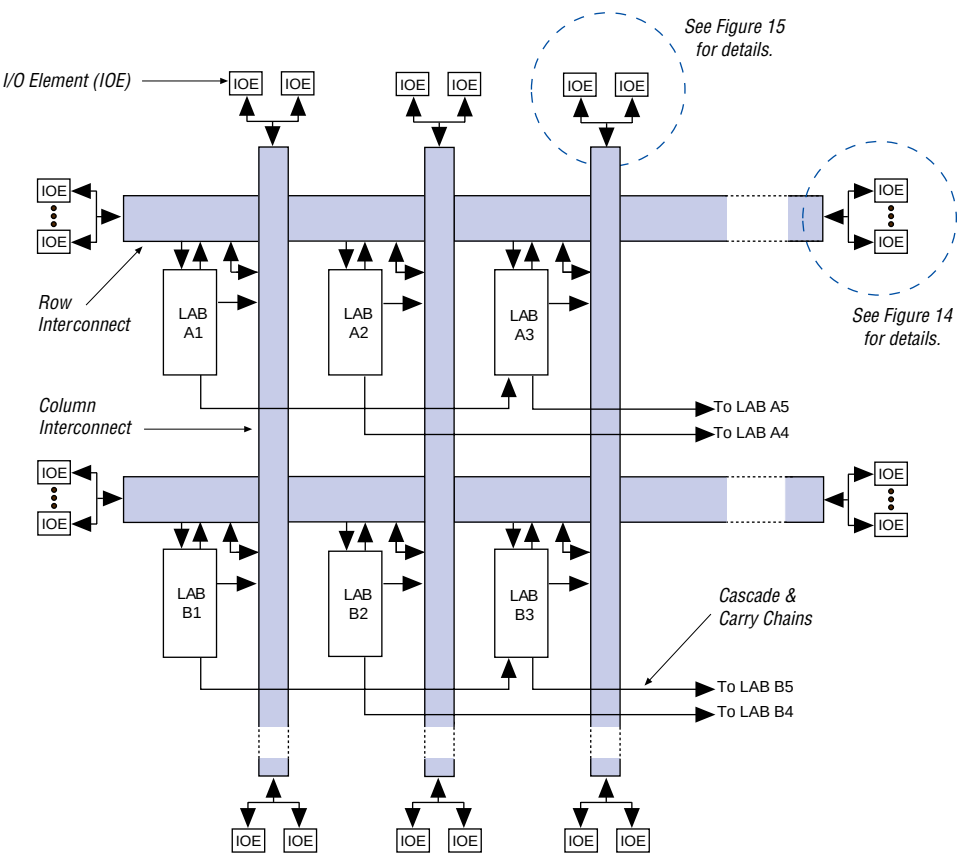


Figure 13. Bidirectional I/O Registers

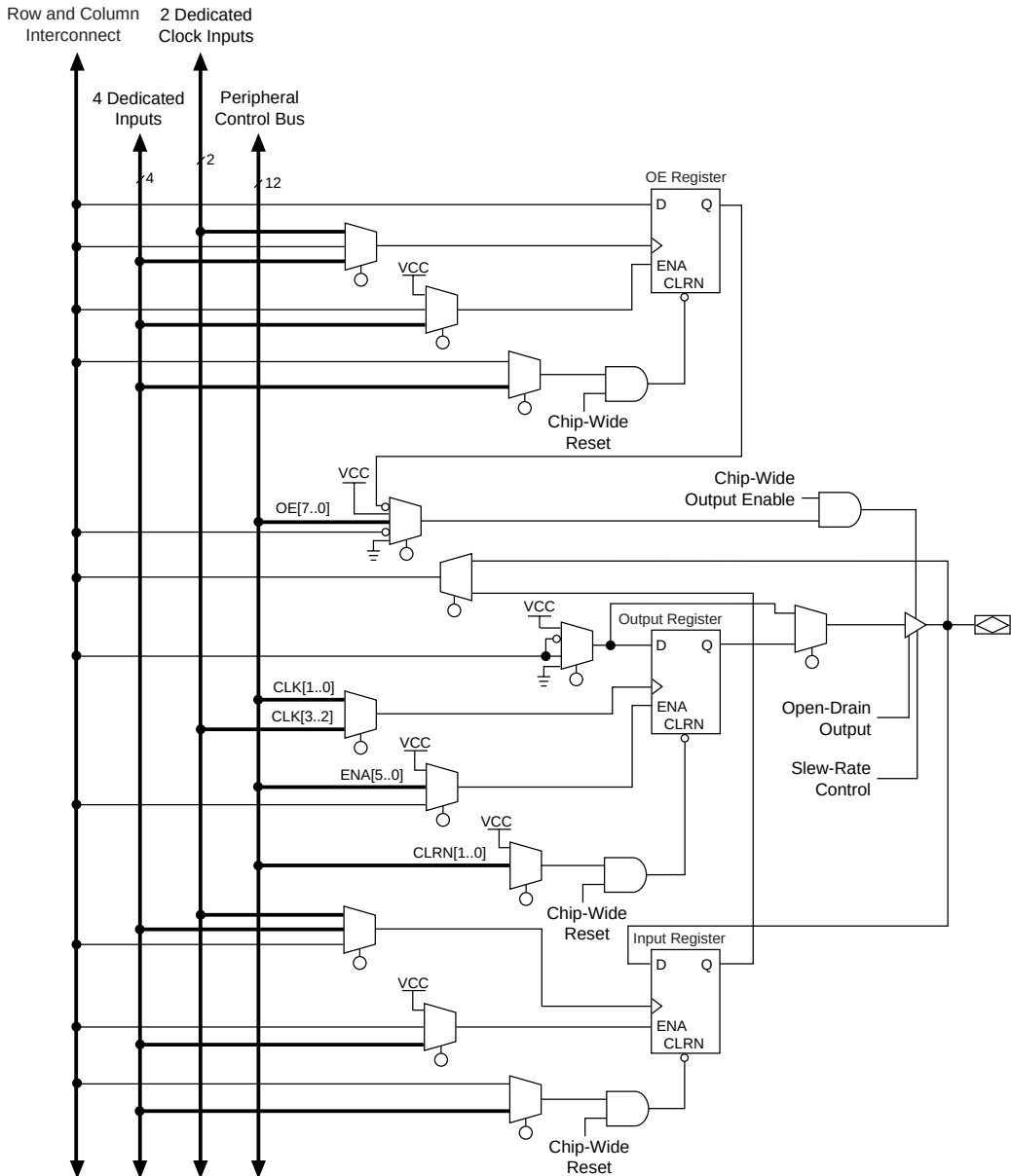


Table 8. EPF10K10, EPF10K20, EPF10K30, EPF10K40 & EPF10K50 Peripheral Bus Sources

Peripheral Control Signal	EPF10K10 EPF10K10A	EPF10K20	EPF10K30 EPF10K30A	EPF10K40	EPF10K50 EPF10K50V
OE0	Row A	Row A	Row A	Row A	Row A
OE1	Row A	Row B	Row B	Row C	Row B
OE2	Row B	Row C	Row C	Row D	Row D
OE3	Row B	Row D	Row D	Row E	Row F
OE4	Row C	Row E	Row E	Row F	Row H
OE5	Row C	Row F	Row F	Row G	Row J
CLKENA0/CLK0/GLOBAL0	Row A	Row A	Row A	Row B	Row A
CLKENA1/OE6/GLOBAL1	Row A	Row B	Row B	Row C	Row C
CLKENA2/CLR0	Row B	Row C	Row C	Row D	Row E
CLKENA3/OE7/GLOBAL2	Row B	Row D	Row D	Row E	Row G
CLKENA4/CLR1	Row C	Row E	Row E	Row F	Row I
CLKENA5/CLK1/GLOBAL3	Row C	Row F	Row F	Row H	Row J

Table 9. EPF10K70, EPF10K100, EPF10K130V & EPF10K250A Peripheral Bus Sources

Peripheral Control Signal	EPF10K70	EPF10K100 EPF10K100A	EPF10K130V	EPF10K250A
OE0	Row A	Row A	Row C	Row E
OE1	Row B	Row C	Row E	Row G
OE2	Row D	Row E	Row G	Row I
OE3	Row I	Row L	Row N	Row P
OE4	Row G	Row I	Row K	Row M
OE5	Row H	Row K	Row M	Row O
CLKENA0/CLK0/GLOBAL0	Row E	Row F	Row H	Row J
CLKENA1/OE6/GLOBAL1	Row C	Row D	Row F	Row H
CLKENA2/CLR0	Row B	Row B	Row D	Row F
CLKENA3/OE7/GLOBAL2	Row F	Row H	Row J	Row L
CLKENA4/CLR1	Row H	Row J	Row L	Row N
CLKENA5/CLK1/GLOBAL3	Row E	Row G	Row I	Row K

Table 15. 32-Bit FLEX 10K Device IDCODE *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)
EPF10K10, EPF10K10A	0000	0001 0000 0001 0000	00001101110	1
EPF10K20	0000	0001 0000 0010 0000	00001101110	1
EPF10K30, EPF10K30A	0000	0001 0000 0011 0000	00001101110	1
EPF10K40	0000	0001 0000 0100 0000	00001101110	1
EPF10K50, EPF10K50V	0000	0001 0000 0101 0000	00001101110	1
EPF10K70	0000	0001 0000 0111 0000	00001101110	1
EPF10K100, EPF10K100A	0000	0000 0001 0000 0000	00001101110	1
EPF10K130V	0000	0000 0001 0011 0000	00001101110	1
EPF10K250A	0000	0000 0010 0101 0000	00001101110	1

Notes:

- (1) The most significant bit (MSB) is on the left.
 (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

FLEX 10K devices include weak pull-ups on JTAG pins.



For more information, see the following documents:

- *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Jam Programming & Test Language Specification*

Tables 22 through 25 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for EPF10K50V and EPF10K130V devices.

Table 22. EPF10K50V & EPF10K130V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground (2)	−0.5	4.6	V
V_I	DC input voltage		−2.0	5.75	V
I_{OUT}	DC output current, per pin		−25	25	mA
T_{STG}	Storage temperature	No bias	−65	150	° C
T_{AMB}	Ambient temperature	Under bias	−65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		RQFP and BGA packages, under bias		135	° C

Table 23. EPF10K50V & EPF10K130V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
V_{CCIO}	Supply voltage for output buffers	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
V_I	Input voltage	(5)	−0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	−40	85	° C
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Figure 22 shows the typical output drive characteristics of EPF10K10A, EPF10K30A, EPF10K100A, and EPF10K250A devices with 3.3-V and 2.5-V V_{CCIO} . The output driver is compliant with the 3.3-V *PCI Local Bus Specification, Revision 2.2* (with 3.3-V V_{CCIO}). Moreover, device analysis shows that the EPF10K10A, EPF10K30A, and EPF 10K100A devices can drive a 5.0-V PCI bus with eight or fewer loads.

Figure 22. Output Drive Characteristics for EPF10K10A, EPF10K30A & EPF10K100A Devices

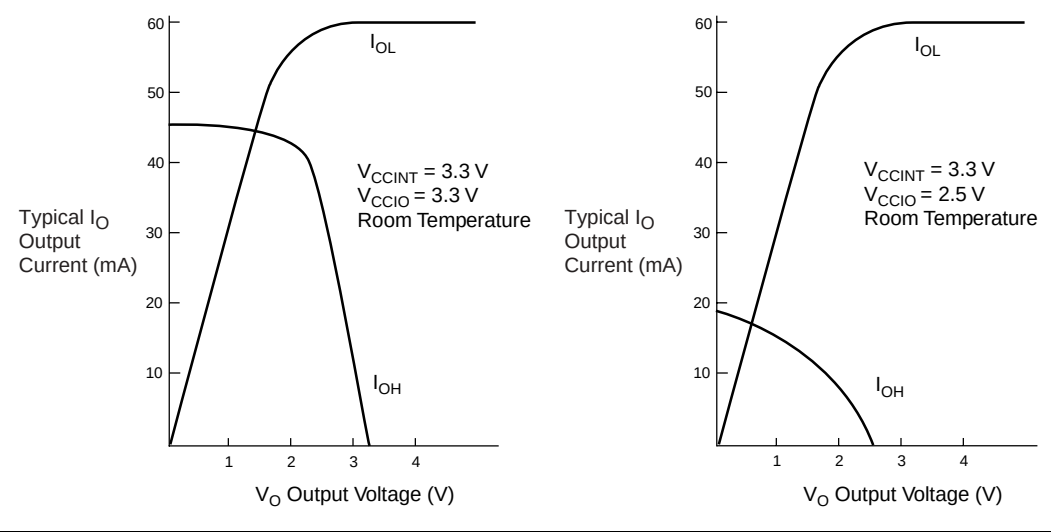


Figure 23 shows the typical output drive characteristics of the EPF10K250A device with 3.3-V and 2.5-V V_{CCIO} .

Table 35. EAB Timing Macroparameters *Notes (1), (6)*

Symbol	Parameter	Conditions
t_{EABAA}	EAB address access delay	
$t_{EABRCCOMB}$	EAB asynchronous read cycle time	
$t_{EABRCREG}$	EAB synchronous read cycle time	
t_{EABWP}	EAB write pulse width	
$t_{EABWCCOMB}$	EAB asynchronous write cycle time	
$t_{EABWCREG}$	EAB synchronous write cycle time	
t_{EABDD}	EAB data-in to data-out valid delay	
$t_{EABDATACO}$	EAB clock-to-output delay when using output registers	
$t_{EABDATASU}$	EAB data/address setup time before clock when using input register	
$t_{EABDATAH}$	EAB data/address hold time after clock when using input register	
$t_{EABWESU}$	EAB WE setup time before clock when using input register	
t_{EABWEH}	EAB WE hold time after clock when using input register	
$t_{EABWDSU}$	EAB data setup time before falling edge of write pulse when not using input registers	
t_{EABWDH}	EAB data hold time after falling edge of write pulse when not using input registers	
$t_{EABWASU}$	EAB address setup time before rising edge of write pulse when not using input registers	
t_{EABWAH}	EAB address hold time after falling edge of write pulse when not using input registers	
t_{EABWO}	EAB write enable to data output valid delay	

Tables 39 through 47 show EPF10K10 and EPF10K20 device internal and external timing parameters.

Table 39. EPF10K10 & EPF10K20 Device LE Timing Microparameters <i>Note (1)</i>					
Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{LUT}		1.4		1.7	ns
t_{CLUT}		0.6		0.7	ns
t_{RLUT}		1.5		1.9	ns
t_{PACKED}		0.6		0.9	ns
t_{EN}		1.0		1.2	ns
t_{CICO}		0.2		0.3	ns
t_{CGEN}		0.9		1.2	ns
t_{CGENR}		0.9		1.2	ns
t_{CASC}		0.8		0.9	ns
t_C		1.3		1.5	ns
t_{CO}		0.9		1.1	ns
t_{COMB}		0.5		0.6	ns
t_{SU}	1.3		2.5		ns
t_H	1.4		1.6		ns
t_{PRE}		1.0		1.2	ns
t_{CLR}		1.0		1.2	ns
t_{CH}	4.0		4.0		ns
t_{CL}	4.0		4.0		ns

Table 42. EPF10K10 & EPF10K20 Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{EABAA}		13.7		17.0	ns
$t_{EABRCCOMB}$	13.7		17.0		ns
$t_{EABRCREG}$	9.7		11.9		ns
t_{EABWP}	5.8		7.2		ns
$t_{EABWCCOMB}$	7.3		9.0		ns
$t_{EABWCREG}$	13.0		16.0		ns
t_{EABDD}		10.0		12.5	ns
$t_{EABDATA CO}$		2.0		3.4	ns
$t_{EABDATASU}$	5.3		5.6		ns
$t_{EABDATAH}$	0.0		0.0		ns
$t_{EABWESU}$	5.5		5.8		ns
t_{EABWEH}	0.0		0.0		ns
$t_{EABWDSU}$	5.5		5.8		ns
t_{EABWDH}	0.0		0.0		ns
$t_{EABWASU}$	2.1		2.7		ns
t_{EABWAH}	0.0		0.0		ns
t_{EABWO}		9.5		11.8	ns

Tables 48 through 56 show EPF10K30, EPF10K40, and EPF10K50 device internal and external timing parameters.

Table 48. EPF10K30, EPF10K40 & EPF10K50 Device LE Timing Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{LUT}		1.3		1.8	ns
t_{CLUT}		0.6		0.6	ns
t_{RLUT}		1.5		2.0	ns
t_{PACKED}		0.5		0.8	ns
t_{EN}		0.9		1.5	ns
t_{CICO}		0.2		0.4	ns
t_{CGEN}		0.9		1.4	ns
t_{CGENR}		0.9		1.4	ns
t_{CASC}		1.0		1.2	ns
t_C		1.3		1.6	ns
t_{CO}		0.9		1.2	ns
t_{COMB}		0.6		0.6	ns
t_{SU}	1.4		1.4		ns
t_H	0.9		1.3		ns
t_{PRE}		0.9		1.2	ns
t_{CLR}		0.9		1.2	ns
t_{CH}	4.0		4.0		ns
t_{CL}	4.0		4.0		ns

Tables 71 through 77 show EPF10K50V device internal and external timing parameters.

Table 71. EPF10K50V Device LE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.9		1.0		1.3		1.6	ns
t_{CLUT}		0.1		0.5		0.6		0.6	ns
t_{RLUT}		0.5		0.8		0.9		1.0	ns
t_{PACKED}		0.4		0.4		0.5		0.7	ns
t_{EN}		0.7		0.9		1.1		1.4	ns
t_{CICO}		0.2		0.2		0.2		0.3	ns
t_{CGEN}		0.8		0.7		0.8		1.2	ns
t_{CGENR}		0.4		0.3		0.3		0.4	ns
t_{CASC}		0.7		0.7		0.8		0.9	ns
t_C		0.3		1.0		1.3		1.5	ns
t_{CO}		0.5		0.7		0.9		1.0	ns
t_{COMB}		0.4		0.4		0.5		0.6	ns
t_{SU}	0.8		1.6		2.2		2.5		ns
t_H	0.5		0.8		1.0		1.4		ns
t_{PRE}		0.8		0.4		0.5		0.5	ns
t_{CLR}		0.8		0.4		0.5		0.5	ns
t_{CH}	2.0		4.0		4.0		4.0		ns
t_{CL}	2.0		4.0		4.0		4.0		ns

Table 81. EPF10K130V Device EAB Internal Timing Macroparameters*Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		11.2		14.2		14.2	ns
$t_{EABRCCOMB}$	11.1		14.2		14.2		ns
$t_{EABRCREG}$	8.5		10.8		10.8		ns
t_{EABWP}	3.7		4.7		4.7		ns
$t_{EABWCCOMB}$	7.6		9.7		9.7		ns
$t_{EABWCREG}$	14.0		17.8		17.8		ns
t_{EABDD}		11.1		14.2		14.2	ns
$t_{EABDATACO}$		3.6		4.6		4.6	ns
$t_{EABDATASU}$	4.4		5.6		5.6		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	4.4		5.6		5.6		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	4.6		5.9		5.9		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.9		5.0		5.0		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		11.1		14.2		14.2	ns

Table 87. EPF10K10A Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		3.3		3.9		5.2	ns
$t_{EABDATA2}$		1.0		1.3		1.7	ns
t_{EABWE1}		2.6		3.1		4.1	ns
t_{EABWE2}		2.7		3.2		4.3	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		1.2		1.4		1.8	ns
$t_{EABYPASS}$		0.1		0.2		0.2	ns
t_{EABSU}	1.4		1.7		2.2		ns
t_{EABH}	0.1		0.1		0.1		ns
t_{AA}		4.5		5.4		7.3	ns
t_{WP}	2.0		2.4		3.2		ns
t_{WDSU}	0.7		0.8		1.1		ns
t_{WDH}	0.5		0.6		0.7		ns
t_{WASU}	0.6		0.7		0.9		ns
t_{WAH}	0.9		1.1		1.5		ns
t_{WO}		3.3		3.9		5.2	ns
t_{DD}		3.3		3.9		5.2	ns
t_{EABOUT}		0.1		0.1		0.2	ns
t_{EABCH}	3.0		3.5		4.0		ns
t_{EABCL}	3.03		3.5		4.0		ns

Table 88. EPF10K10A Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		8.1		9.8		13.1	ns
$t_{EABRCCOMB}$	8.1		9.8		13.1		ns
$t_{EABRCREG}$	5.8		6.9		9.3		ns
t_{EABWP}	2.0		2.4		3.2		ns
$t_{EABWCCOMB}$	3.5		4.2		5.6		ns
$t_{EABWCREG}$	9.4		11.2		14.8		ns
t_{EABDD}		6.9		8.3		11.0	ns
$t_{EABDATA CO}$		1.3		1.5		2.0	ns
$t_{EABDATASU}$	2.4		3.0		3.9		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	4.1		4.9		6.5		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.4		1.6		2.2		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	2.5		3.0		4.1		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		6.2		7.5		9.9	ns

Table 95. EPF10K30A Device EAB Internal Timing Macroparameters*Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		9.7		11.6		16.2	ns
$t_{EABRCCOMB}$	9.7		11.6		16.2		ns
$t_{EABRCREG}$	5.9		7.1		9.7		ns
t_{EABWP}	3.8		4.5		5.9		ns
$t_{EABWCCOMB}$	4.0		4.7		6.3		ns
$t_{EABWCREG}$	9.8		11.6		16.6		ns
t_{EABDD}		9.2		11.0		16.1	ns
$t_{EABDATACO}$		1.7		2.1		3.4	ns
$t_{EABDATASU}$	2.3		2.7		3.5		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	3.3		3.9		4.9		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	3.2		3.8		5.0		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.7		4.4		5.1		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		6.1		7.3		11.3	ns

Notes to tables:

- (1) All timing parameters are described in Tables 32 through 38 in this data sheet.
- (2) Using an LE to register the signal may provide a lower setup time.
- (3) This parameter is specified by characterization.

Tables 99 through 105 show EPF10K100A device internal and external timing parameters.

Table 99. EPF10K100A Device LE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		1.0		1.2		1.4	ns
t_{CLUT}		0.8		0.9		1.1	ns
t_{RLUT}		1.4		1.6		1.9	ns
t_{PACKED}		0.4		0.5		0.5	ns
t_{EN}		0.6		0.7		0.8	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		0.4		0.4		0.6	ns
t_{CGENR}		0.6		0.7		0.8	ns
t_{CASC}		0.7		0.9		1.0	ns
t_C		0.9		1.0		1.2	ns
t_{CO}		0.2		0.3		0.3	ns
t_{COMB}		0.6		0.7		0.8	ns
t_{SU}	0.8		1.0		1.2		ns
t_H	0.3		0.5		0.5		ns
t_{PRE}		0.3		0.3		0.4	ns
t_{CLR}		0.3		0.3		0.4	ns
t_{CH}	2.5		3.5		4.0		ns
t_{CL}	2.5		3.5		4.0		ns

Table 101. EPF10K100A Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.8		2.1		2.4	ns
$t_{EABDATA2}$		3.2		3.7		4.4	ns
t_{EABWE1}		0.8		0.9		1.1	ns
t_{EABWE2}		2.3		2.7		3.1	ns
t_{EABCLK}		0.8		0.9		1.1	ns
t_{EABCO}		1.0		1.1		1.4	ns
$t_{EABYPASS}$		0.3		0.3		0.4	ns
t_{EABSU}	1.3		1.5		1.8		ns
t_{EABH}	0.4		0.5		0.5		ns
t_{AA}		4.1		4.8		5.6	ns
t_{WP}	3.2		3.7		4.4		ns
t_{WDSU}	2.4		2.8		3.3		ns
t_{WDH}	0.2		0.2		0.3		ns
t_{WASU}	0.2		0.2		0.3		ns
t_{WAH}	0.0		0.0		0.0		ns
t_{WO}		3.4		3.9		4.6	ns
t_{DD}		3.4		3.9		4.6	ns
t_{EABOUT}		0.3		0.3		0.4	ns
t_{EABCH}	2.5		3.5		4.0		ns
t_{EABCL}	3.2		3.7		4.4		ns

Notes to tables:

- (1) All timing parameters are described in Tables 32 through 37 in this data sheet.
- (2) Using an LE to register the signal may provide a lower setup time.
- (3) This parameter is specified by characterization.

ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. Figure 31 illustrates the incoming and generated clock specifications.

Figure 31. Specifications for the Incoming & Generated Clocks

The t_I parameter refers to the nominal input clock period; the t_O parameter refers to the nominal output clock period.

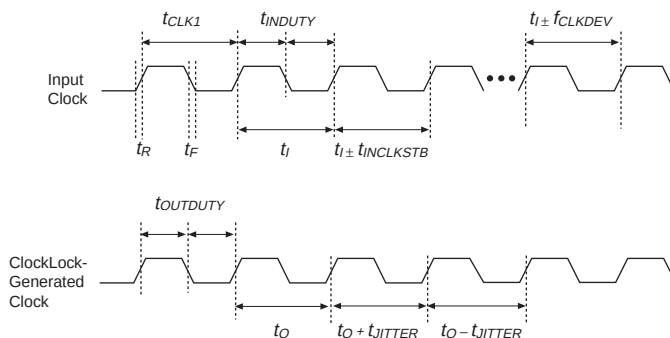


Table 113 summarizes the ClockLock and ClockBoost parameters.

Table 113. ClockLock & ClockBoost Parameters (Part 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
t_R	Input rise time			2	ns
t_F	Input fall time			2	ns
t_{INDUTY}	Input duty cycle	45		55	%
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)	30		80	MHz
t_{CLK1}	Input clock period (ClockBoost clock multiplication factor equals 1)	12.5		33.3	ns
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)	16		50	MHz
t_{CLK2}	Input clock period (ClockBoost clock multiplication factor equals 2)	20		62.5	ns



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