Intel - EPF10K20RC208-4N Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	144
Number of Logic Elements/Cells	1152
Total RAM Bits	12288
Number of I/O	147
Number of Gates	63000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP Exposed Pad
Supplier Device Package	208-RQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k20rc208-4n

Table 4. FLEX 10K Package Options & I/O Pin Count *Note (1)*

Device	84-Pin PLCC	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP RQFP	240-Pin PQFP RQFP
EPF10K10	59		102	134	
EPF10K10A		66	102	134	
EPF10K20			102	147	189
EPF10K30				147	189
EPF10K30A			102	147	189
EPF10K40				147	189
EPF10K50					189
EPF10K50V					189
EPF10K70					189
EPF10K100					
EPF10K100A					189
EPF10K130V					
EPF10K250A					

Table 5. FLEX 10K Package Options & I/O Pin Count (Continued) *Note (1)*

Device	503-Pin PGA	599-Pin PGA	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	600-Pin BGA	403-Pin PGA
EPF10K10							
EPF10K10A			150		150 *(2)*		
EPF10K20							
EPF10K30				246			
EPF10K30A			191	246	246		
EPF10K40							
EPF10K50				274			310
EPF10K50V				274			
EPF10K70	358						
EPF10K100	406						
EPF10K100A				274	369	406	
EPF10K130V		470				470	
EPF10K250A		470				470	

Notes to tables:

(1) FLEX 10K and FLEX 10KA device package types include plastic J-lead chip carrier (PLCC), thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), ball-grid array (BGA), pin-grid array (PGA), and FineLine BGA™ packages.

(2) This option is supported with a 256-pin FineLine BGA package. By using SameFrame pin migration, all FineLine BGA packages are pin compatible. For example, a board can be designed to support both 256-pin and 484-pin FineLine BGA packages. The Altera software automatically avoids conflicting pins when future migration is set.

General Description

Altera's FLEX 10K devices are the industry's first embedded PLDs. Based on reconfigurable CMOS SRAM elements, the Flexible Logic Element MatriX (FLEX) architecture incorporates all features necessary to implement common gate array megafunctions. With up to 250,000 gates, the FLEX 10K family provides the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device.

FLEX 10K devices are reconfigurable, which allows 100% testing prior to shipment. As a result, the designer is not required to generate test vectors for fault coverage purposes. Additionally, the designer does not need to manage inventories of different ASIC designs; FLEX 10K devices can be configured on the board for the specific functionality required.

Table 6 shows FLEX 10K performance for some common designs. All performance values were obtained with Synopsys DesignWare or LPM functions. No special design technique was required to implement the applications; the designer simply inferred or instantiated a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

Table 6. FLEX 10K & FLEX 10KA Performance

Application	Resources Used		Performance				Units
	LEs	EABs	-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	-4 Speed Grade	
16-bit loadable counter *(1)*	16	0	204	166	125	95	MHz
16-bit accumulator *(1)*	16	0	204	166	125	95	MHz
16-to-1 multiplexer *(2)*	10	0	4.2	5.8	6.0	7.0	ns
256 × 8 RAM read cycle speed *(3)*	0	1	172	145	108	84	MHz
256 × 8 RAM write cycle speed *(3)*	0	1	106	89	68	63	MHz

Notes:

(1) The speed grade of this application is limited because of clock high and low specifications.

(2) This application uses combinatorial inputs and outputs.

(3) This application uses registered inputs and outputs.

For more information, see the following documents:

- *Configuration Devices for APEX & FLEX Devices Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Application Note 116 (Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices)*

FLEX 10K devices are supported by Altera development systems; single, integrated packages that offer schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The Altera software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Altera software works easily with common gate array EDA tools for synthesis and simulation. For example, the Altera software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Altera software contains EDA libraries that use device-specific features such as carry chains which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Altera development systems include DesignWare functions that are optimized for the FLEX 10K architecture.

The Altera development systems run on Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations.

See the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* for more information.

Functional Description

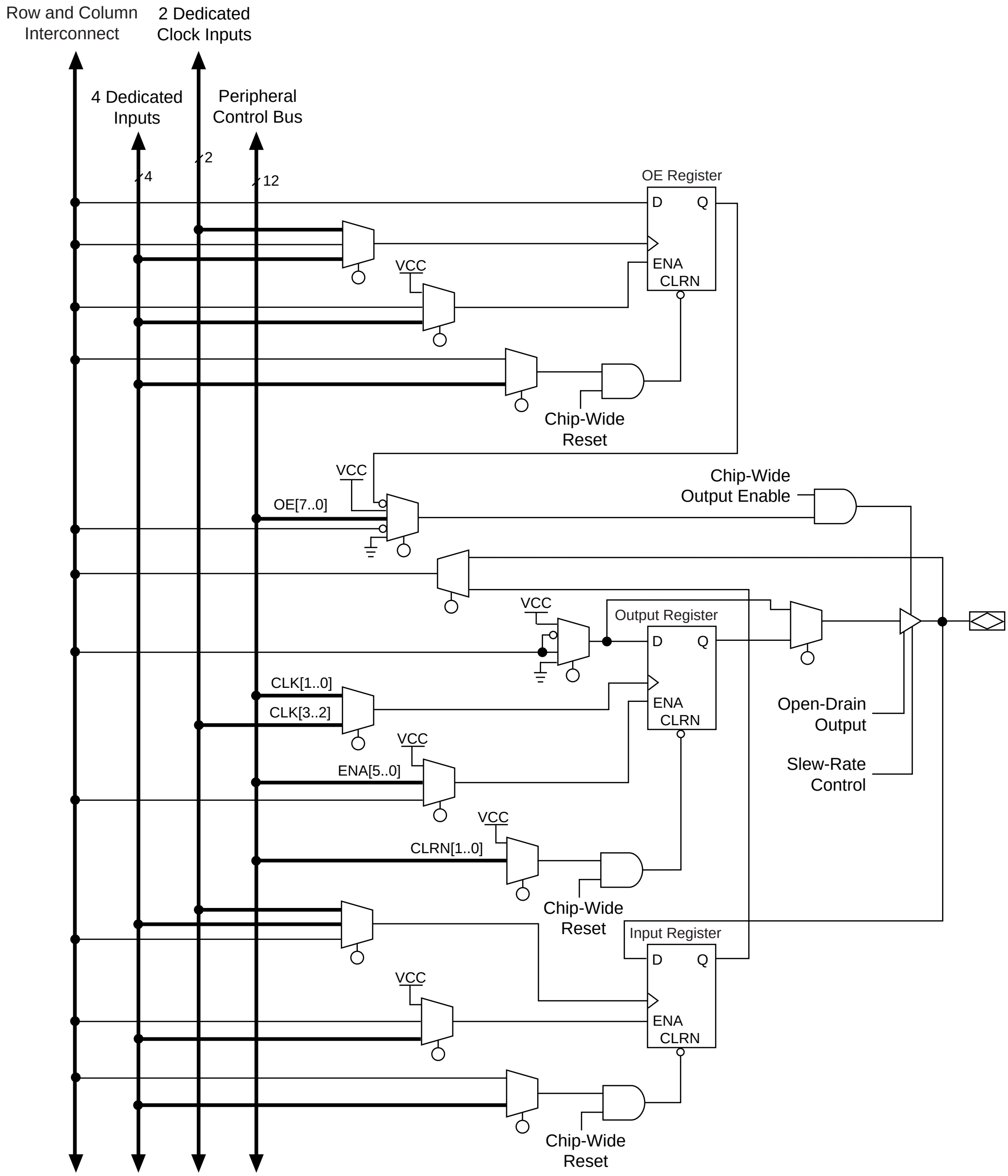
Each FLEX 10K device contains an embedded array to implement memory and specialized logic functions, and a logic array to implement general logic.

The embedded array consists of a series of EABs. When implementing memory functions, each EAB provides 2,048 bits, which can be used to create RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. When implementing logic, each EAB can contribute 100 to 600 gates towards complex logic functions, such as multipliers, microcontrollers, state machines, and DSP functions. EABs can be used independently, or multiple EABs can be combined to implement larger functions.

I/O Element

An I/O element (IOE) contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. In some cases, using an LE register for an input register will result in a faster setup time than using an IOE register. IOEs can be used as input, output, or bidirectional pins. For bidirectional registered I/O implementation, the output register should be in the IOE and, the data input and output enable register should be LE registers placed adjacent to the bidirectional pin. The Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Figure 13 shows the bidirectional I/O registers.

Figure 13. Bidirectional I/O Registers



Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across devices; it provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock enable or eight output enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by specific LEs. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, an LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal. The chip-wide reset signal will reset all IOE registers, overriding any other control signals.

Tables 8 and 9 list the sources for each peripheral control signal, and the rows that can drive global signals. These tables also show how the output enable, clock enable, clock, and clear signals share 12 peripheral control signals.

Signals on the peripheral control bus can also drive the four global signals, referred to as GLOBAL0 through GLOBAL3 in Tables 8 and 9. The internally generated signal can drive the global signal, providing the same low-skew, low-delay characteristics for an internally generated signal as for a signal driven by an input. This feature is ideal for internally generated clear or clock signals with high fan-out. When a global signal is driven by internal logic, the dedicated input pin that drives that global signal cannot be used. The dedicated input pin should be driven to a known logic state (such as ground) and not be allowed to float.

When the chip-wide output enable pin is held low, it will tri-state all pins on the device. This option can be set in the Global Project Device Options menu. Additionally, the registers in the IOE can be reset by holding the chip-wide reset pin low.

Row-to-IOE Connections

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Up to eight IOEs connect to each side of each row channel. See Figure 14.

Figure 14. FLEX 10K Row-to-IOE Connections

The values for m and n are provided in Table 10.

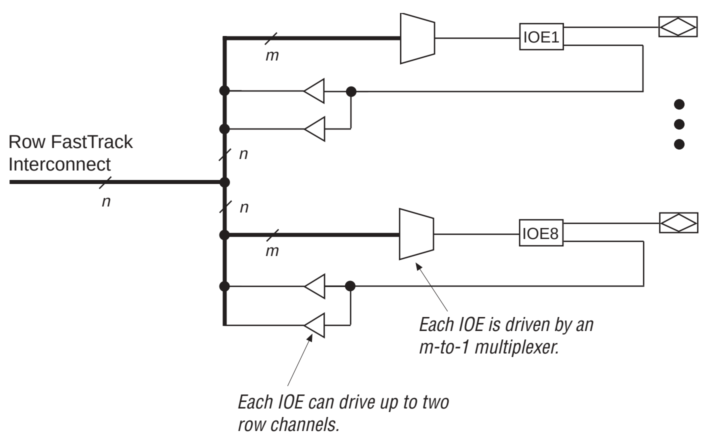


Table 15. 32-Bit FLEX 10K Device IDCODE *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) *(2)*
EPF10K10, EPF10K10A	0000	0001 0000 0001 0000	00001101110	1
EPF10K20	0000	0001 0000 0010 0000	00001101110	1
EPF10K30, EPF10K30A	0000	0001 0000 0011 0000	00001101110	1
EPF10K40	0000	0001 0000 0100 0000	00001101110	1
EPF10K50, EPF10K50V	0000	0001 0000 0101 0000	00001101110	1
EPF10K70	0000	0001 0000 0111 0000	00001101110	1
EPF10K100, EPF10K100A	0000	0000 0001 0000 0000	00001101110	1
EPF10K130V	0000	0000 0001 0011 0000	00001101110	1
EPF10K250A	0000	0000 0010 0101 0000	00001101110	1

Notes:

(1) The most significant bit (MSB) is on the left.

(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

FLEX 10K devices include weak pull-ups on JTAG pins.

For more information, see the following documents:

- *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Jam Programming & Test Language Specification*

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms. V_{CC} must rise monotonically.
(5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(6) These values are specified under the Recommended Operation Condition shown in Table 18 on page 45.
(7) The I_{OH} parameter refers to high-level TTL or CMOS output current.
(8) The I_{OL} parameter refers to low-level TTL or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(9) This value is specified for normal device operation. The value may vary during power-up.
(10) Capacitance is sample-tested only.

Figure 20 shows the typical output drive characteristics of FLEX 10K devices with 5.0-V and 3.3-V V_{CCIO}. The output driver is compliant with the 5.0-V ***PCI Local Bus Specification, Revision 2.2*** (for 5.0-V V_{CCIO}).

Figure 20. Output Drive Characteristics of FLEX 10K Devices

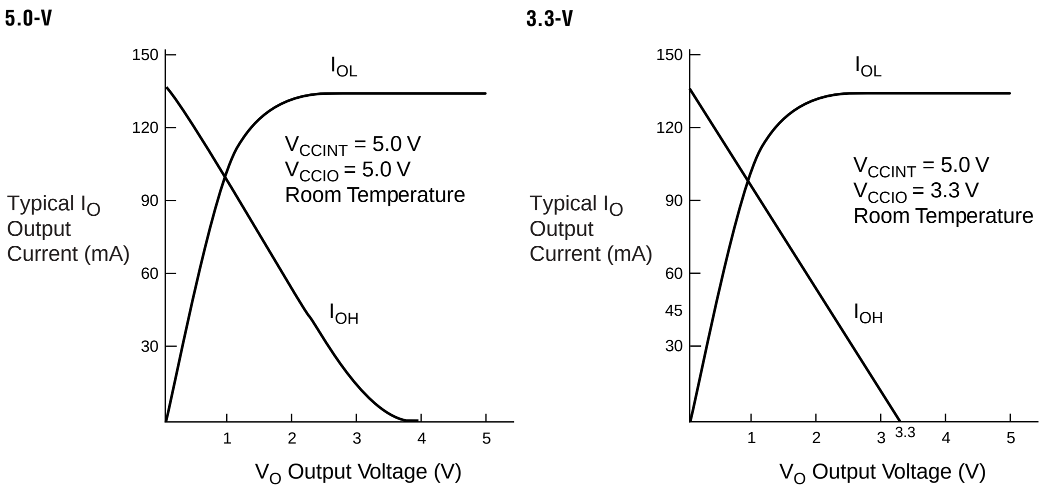


Table 28. FLEX 10KA 3.3-V Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		1.7 or $0.5 \times V_{CCINT}$, whichever is lower		5.75	V
V_{IL}	Low-level input voltage		–0.5		$0.3 \times V_{CCINT}$	V
V_{OH}	3.3-V high-level TTL output voltage	I_{OH} = –11 mA DC, V_{CCIO} = 3.00 V *(8)*	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(8)*	$V_{CCIO} - 0.2$			V
	3.3-V high-level PCI output voltage	I_{OH} = –0.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(8)*	$0.9 \times V_{CCIO}$			V
	2.5-V high-level output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 2.30 V *(8)*	2.1			V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V *(8)*	2.0			V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V *(8)*	1.7			V
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 9 mA DC, V_{CCIO} = 3.00 V *(9)*			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(9)*			0.2	V
	3.3-V low-level PCI output voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(9)*			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V *(9)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(9)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(9)*			0.7	V
I_I	Input pin leakage current	V_I = 5.3 V to –0.3 V *(10)*	–10		10	μA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 5.3 V to –0.3 V *(10)*	–10		10	μA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load		0.3	10	mA
		V_I = ground, no load *(11)*		10		mA

Table 29. 3.3-V Device Capacitance of EPF10K10A & EPF10K30A Devices *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Table 30. 3.3-V Device Capacitance of EPF10K100A Devices *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

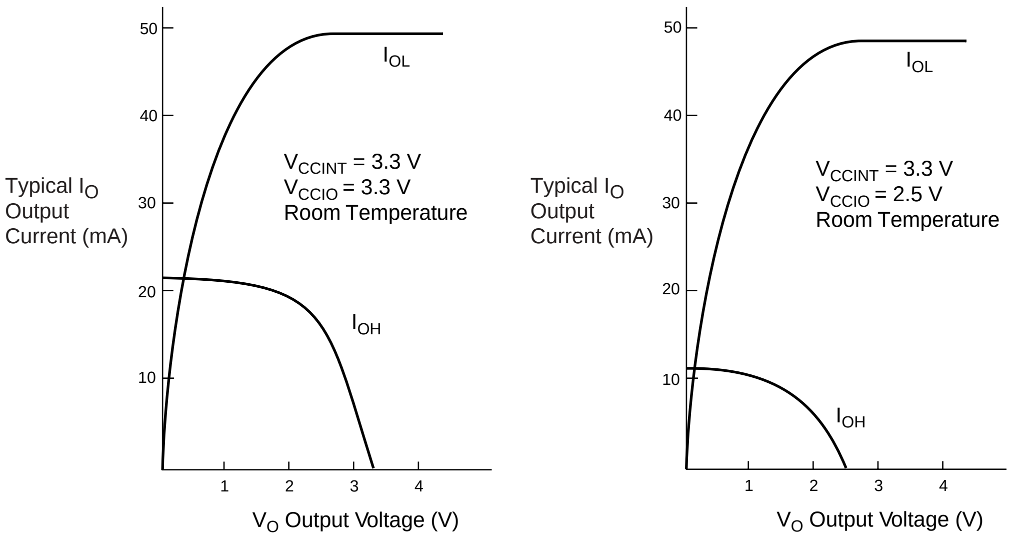
Table 31. 3.3-V Device Capacitance of EPF10K250A Devices *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC voltage input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) FLEX 10KA device inputs may be driven before V_{CCINT} and V_{CCIO} are powered.
(6) Typical values are for T_A = 25° C and V_{CC} = 3.3 V.
(7) These values are specified under the Recommended Operating Conditions shown in Table 27 on page 51.
(8) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
(9) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(10) This value is specified for normal device operation. The value may vary during power-up.
(11) This parameter applies to all -1 speed grade commercial temperature devices and all -2 speed grade industrial-temperature devices.
(12) Capacitance is sample-tested only.

Figure 23. Output Drive Characteristics for EPF10K250A Device



Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Device performance can be estimated by following the signal path from a source, through the interconnect, to the destination. For example, the registered performance between two LEs on the same row can be calculated by adding the following parameters:

- LE register clock-to-output delay (t_{CO})
- Interconnect delay ($t_{SAMEROW}$)
- LE look-up table delay (t_{LUT})
- LE register setup time (t_{SU})

The routing delay depends on the placement of the source and destination LEs. A more complex registered path may involve multiple combinatorial LEs between the source and destination LEs.

Table 42. EPF10K10 & EPF10K20 Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{EABAA}		13.7		17.0	ns
$t_{EABRCCOMB}$	13.7		17.0		ns
$t_{EABRCREG}$	9.7		11.9		ns
t_{EABWP}	5.8		7.2		ns
$t_{EABWCCOMB}$	7.3		9.0		ns
$t_{EABWCREG}$	13.0		16.0		ns
t_{EABDD}		10.0		12.5	ns
$t_{EABDATACO}$		2.0		3.4	ns
$t_{EABDATASU}$	5.3		5.6		ns
$t_{EABDATAH}$	0.0		0.0		ns
$t_{EABWESU}$	5.5		5.8		ns
t_{EABWEH}	0.0		0.0		ns
$t_{EABWDSU}$	5.5		5.8		ns
t_{EABWDH}	0.0		0.0		ns
$t_{EABWASU}$	2.1		2.7		ns
t_{EABWAH}	0.0		0.0		ns
t_{EABWO}		9.5		11.8	ns

Table 52. EPF10K30 Device Interconnect Timing Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{DIN2IOE}$		6.9		8.7	ns
t_{DIN2LE}		3.6		4.8	ns
$t_{DIN2DATA}$		5.5		7.2	ns
$t_{DCLK2IOE}$		4.6		6.2	ns
$t_{DCLK2LE}$		3.6		4.8	ns
$t_{SAMELAB}$		0.3		0.3	ns
$t_{SAMEROW}$		3.3		3.7	ns
$t_{SAMECOLUMN}$		2.5		2.7	ns
$t_{DIFFROW}$		5.8		6.4	ns
$t_{TWOROWS}$		9.1		10.1	ns
$t_{LEPERIPH}$		6.2		7.1	ns
$t_{LABCARRY}$		0.4		0.6	ns
$t_{LABCASC}$		2.4		3.0	ns

Table 53. EPF10K40 Device Interconnect Timing Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{DIN2IOE}$		7.6		9.4	ns
t_{DIN2LE}		3.6		4.8	ns
$t_{DIN2DATA}$		5.5		7.2	ns
$t_{DCLK2IOE}$		4.6		6.2	ns
$t_{DCLK2LE}$		3.6		4.8	ns
$t_{SAMELAB}$		0.3		0.3	ns
$t_{SAMEROW}$		3.3		3.7	ns
$t_{SAMECOLUMN}$		3.1		3.2	ns
$t_{DIFFROW}$		6.4		6.4	ns
$t_{TWOROWS}$		9.7		10.6	ns
$t_{LEPERIPH}$		6.4		7.1	ns
$t_{LABCARRY}$		0.4		0.6	ns
$t_{LABCASC}$		2.4		3.0	ns

Notes to tables:
(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Tables 57 through 63 show EPF10K70 device internal and external timing parameters.

Table 57. EPF10K70 Device LE Timing Microparameters *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		1.3		1.5		2.0	ns
t_{CLUT}		0.4		0.4		0.5	ns
t_{RLUT}		1.5		1.6		2.0	ns
t_{PACKED}		0.8		0.9		1.3	ns
t_{EN}		0.8		0.9		1.2	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		1.0		1.1		1.4	ns
t_{CGENR}		1.1		1.2		1.5	ns
t_{CASC}		1.0		1.1		1.3	ns
t_{C}		0.7		0.8		1.0	ns
t_{CO}		0.9		1.0		1.4	ns
t_{COMB}		0.4		0.5		0.7	ns
t_{SU}	1.9		2.1		2.6		ns
t_{H}	2.1		2.3		3.1		ns
t_{PRE}		0.9		1.0		1.4	ns
t_{CLR}		0.9		1.0		1.4	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns

Table 61. EPF10K70 Device Interconnect Timing Microparameters Note (1)

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		6.6		7.3		8.8	ns
t_{DIN2LE}		4.2		4.8		6.0	ns
$t_{DIN2DATA}$		6.5		7.1		10.8	ns
$t_{DCLK2IOE}$		5.5		6.2		7.7	ns
$t_{DCLK2LE}$		4.2		4.8		6.0	ns
$t_{SAMELAB}$		0.4		0.4		0.5	ns
$t_{SAMEROW}$		4.8		4.9		5.5	ns
$t_{SAMECOLUMN}$		3.3		3.4		3.7	ns
$t_{DIFFROW}$		8.1		8.3		9.2	ns
$t_{TWOROWS}$		12.9		13.2		14.7	ns
$t_{LEPERIPH}$		5.5		5.7		6.5	ns
$t_{LABCARRY}$		0.8		0.9		1.1	ns
$t_{LABCASC}$		2.7		3.0		3.2	ns

Table 62. EPF10K70 Device External Timing Parameters Note (1)

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		17.2		19.1		24.2	ns
t_{INSU} (2), (3)	6.6		7.3		8.0		ns
t_{INH} (3)	0.0		0.0		0.0		ns
t_{OUTCO} (3)	2.0	9.9	2.0	11.1	2.0	14.3	ns

Table 63. EPF10K70 Device External Bidirectional Timing Parameters Note (1)

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	7.4		8.1		10.4		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	9.9	2.0	11.1	2.0	14.3	ns
$t_{XZBIDIR}$		13.7		15.4		18.5	ns
$t_{ZXBIDIR}$		13.7		15.4		18.5	ns

Table 72. EPF10K50V Device IOE Timing Microparameters *Note (1)*									
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{IOD}		1.2		1.6		1.9		2.1	ns
t_{IOC}		0.3		0.4		0.5		0.5	ns
t_{IOCO}		0.3		0.3		0.4		0.4	ns
t_{IOCOMB}		0.0		0.0		0.0		0.0	ns
t_{IOSU}	2.8		2.8		3.4		3.9		ns
t_{IOH}	0.7		0.8		1.0		1.4		ns
t_{IOCLR}		0.5		0.6		0.7		0.7	ns
t_{OD1}		2.8		3.2		3.9		4.7	ns
t_{OD2}		–		–		–		–	ns
t_{OD3}		6.5		6.9		7.6		8.4	ns
t_{XZ}		2.8		3.1		3.8		4.6	ns
t_{ZX1}		2.8		3.1		3.8		4.6	ns
t_{ZX2}		–		–		–		–	ns
t_{ZX3}		6.5		6.8		7.5		8.3	ns
t_{INREG}		5.0		5.7		7.0		9.0	ns
t_{IOFD}		1.5		1.9		2.3		2.7	ns
t_{INCOMB}		1.5		1.9		2.3		2.7	ns

Notes to tables:
(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Tables 99 through 105 show EPF10K100A device internal and external timing parameters.

Table 99. EPF10K100A Device LE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		1.0		1.2		1.4	ns
t_{CLUT}		0.8		0.9		1.1	ns
t_{RLUT}		1.4		1.6		1.9	ns
t_{PACKED}		0.4		0.5		0.5	ns
t_{EN}		0.6		0.7		0.8	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		0.4		0.4		0.6	ns
t_{CGENR}		0.6		0.7		0.8	ns
t_{CASC}		0.7		0.9		1.0	ns
t_C		0.9		1.0		1.2	ns
t_{CO}		0.2		0.3		0.3	ns
t_{COMB}		0.6		0.7		0.8	ns
t_{SU}	0.8		1.0		1.2		ns
t_H	0.3		0.5		0.5		ns
t_{PRE}		0.3		0.3		0.4	ns
t_{CLR}		0.3		0.3		0.4	ns
t_{CH}	2.5		3.5		4.0		ns
t_{CL}	2.5		3.5		4.0		ns

Notes to tables:
(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Tables 106 through 112 show EPF10K250A device internal and external timing parameters.

Table 106. EPF10K250A Device LE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.9		1.0		1.4	ns
t_{CLUT}		1.2		1.3		1.6	ns
t_{RLUT}		2.0		2.3		2.7	ns
t_{PACKED}		0.4		0.4		0.5	ns
t_{EN}		1.4		1.6		1.9	ns
t_{CICO}		0.2		0.3		0.3	ns
t_{CGEN}		0.4		0.6		0.6	ns
t_{CGENR}		0.8		1.0		1.1	ns
t_{CASC}		0.7		0.8		1.0	ns
t_{C}		1.2		1.3		1.6	ns
t_{CO}		0.6		0.7		0.9	ns
t_{COMB}		0.5		0.6		0.7	ns
t_{SU}	1.2		1.4		1.7		ns
t_{H}	1.2		1.3		1.6		ns
t_{PRE}		0.7		0.8		0.9	ns
t_{CLR}		0.7		0.8		0.9	ns
t_{CH}	2.5		3.0		3.5		ns
t_{CL}	2.5		3.0		3.5		ns

Table 113. ClockLock & ClockBoost Parameters (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
$f_{CLKDEV1}$	Input deviation from user specification in MAX+PLUS II (ClockBoost clock multiplication factor equals 1) *(1)*			±1	MHz
$f_{CLKDEV2}$	Input deviation from user specification in MAX+PLUS II (ClockBoost clock multiplication factor equals 2) *(1)*			±0.5	MHz
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)			100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock *(2)*			10	µs
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock *(3)*			1	ns
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock	40	50	60	%

Notes:

(1) To implement the ClockLock and ClockBoost circuitry with the MAX+PLUS II software, designers must specify the input frequency. The MAX+PLUS II software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The f_{CLKDEV} parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.

(2) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the t_{LOCK} value is less than the time required for configuration.

(3) The t_{JITTER} specification is measured under long-term observation.

Power Consumption

The supply power (P) for FLEX 10K devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

Typical $I_{CCSTANDBY}$ values are shown as I_{CC0} in the FLEX 10K device DC operating conditions tables on pages 46, 49, and 52 of this data sheet. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value is calculated based on the amount of current that each LE typically consumes. The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

☞ Compared to the rest of the device, the embedded array consumes a negligible amount of power. Therefore, the embedded array can be ignored when calculating supply current.

The $I_{CCACTIVE}$ value is calculated with the following equation:

$$I_{CCACTIVE} = K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}} \times \frac{\mu A}{MHz \times LE}$$

The parameters in this equation are shown below: