Intel - EPF10K20RC240-3N Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	144
Number of Logic Elements/Cells	1152
Total RAM Bits	12288
Number of I/O	189
Number of Gates	63000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-RQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k20rc240-3n

Notes to tables:
(1) FLEX 10K and FLEX 10KA device package types include plastic J-lead chip carrier (PLCC), thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), ball-grid array (BGA), pin-grid array (PGA), and FineLine BGA™ packages.
(2) This option is supported with a 256-pin FineLine BGA package. By using SameFrame pin migration, all FineLine BGA packages are pin compatible. For example, a board can be designed to support both 256-pin and 484-pin FineLine BGA packages. The Altera software automatically avoids conflicting pins when future migration is set.

General Description

Altera's FLEX 10K devices are the industry's first embedded PLDs. Based on reconfigurable CMOS SRAM elements, the Flexible Logic Element MatriX (FLEX) architecture incorporates all features necessary to implement common gate array megafunctions. With up to 250,000 gates, the FLEX 10K family provides the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device.

FLEX 10K devices are reconfigurable, which allows 100% testing prior to shipment. As a result, the designer is not required to generate test vectors for fault coverage purposes. Additionally, the designer does not need to manage inventories of different ASIC designs; FLEX 10K devices can be configured on the board for the specific functionality required.

Table 6 shows FLEX 10K performance for some common designs. All performance values were obtained with Synopsys DesignWare or LPM functions. No special design technique was required to implement the applications; the designer simply inferred or instantiated a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

Table 6. FLEX 10K & FLEX 10KA Performance

Application	Resources Used		Performance				Units
	LEs	EABs	-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	-4 Speed Grade	
16-bit loadable counter *(1)*	16	0	204	166	125	95	MHz
16-bit accumulator *(1)*	16	0	204	166	125	95	MHz
16-to-1 multiplexer *(2)*	10	0	4.2	5.8	6.0	7.0	ns
256 × 8 RAM read cycle speed *(3)*	0	1	172	145	108	84	MHz
256 × 8 RAM write cycle speed *(3)*	0	1	106	89	68	63	MHz

Notes:
(1) The speed grade of this application is limited because of clock high and low specifications.
(2) This application uses combinatorial inputs and outputs.
(3) This application uses registered inputs and outputs.

LE Operating Modes

The FLEX 10K LE can operate in the following four modes:

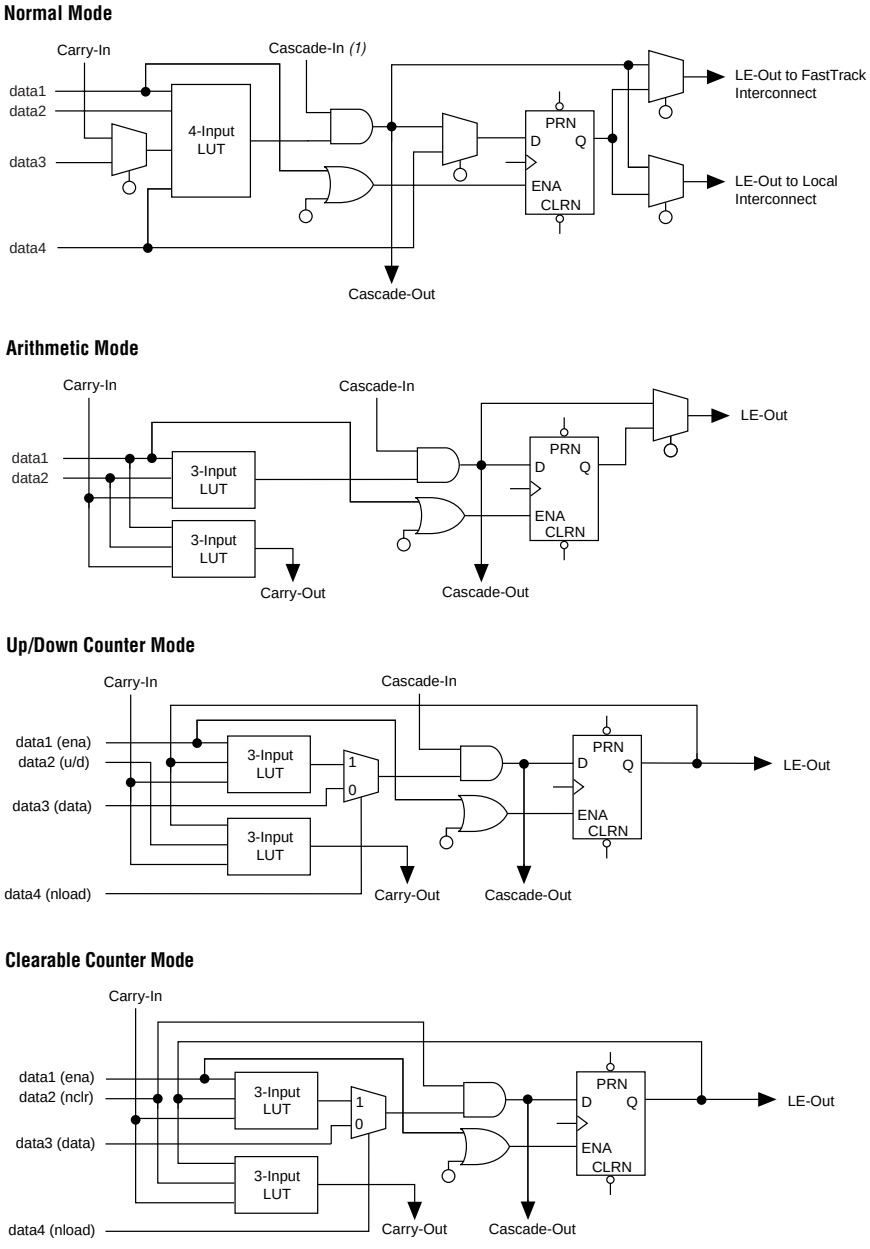
- Normal mode
- Arithmetic mode
- Up/down counter mode
- Clearable counter mode

Each of these modes uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. Three inputs to the LE provide clock, clear, and preset control for the register. The Altera software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions which use a specific LE operating mode for optimal performance.

The architecture provides a synchronous clock enable to the register in all four modes. The Altera software can set `DATA1` to enable the register synchronously, providing easy implementation of fully synchronous designs.

Figure 9 shows the LE operating modes.

Figure 9. FLEX 10K LE Operating Modes



Note:
(1) Packed registers cannot be used with the cascade chain.

I/O Element

An I/O element (IOE) contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. In some cases, using an LE register for an input register will result in a faster setup time than using an IOE register. IOEs can be used as input, output, or bidirectional pins. For bidirectional registered I/O implementation, the output register should be in the IOE and, the data input and output enable register should be LE registers placed adjacent to the bidirectional pin. The Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Figure 13 shows the bidirectional I/O registers.

Figure 13. Bidirectional I/O Registers

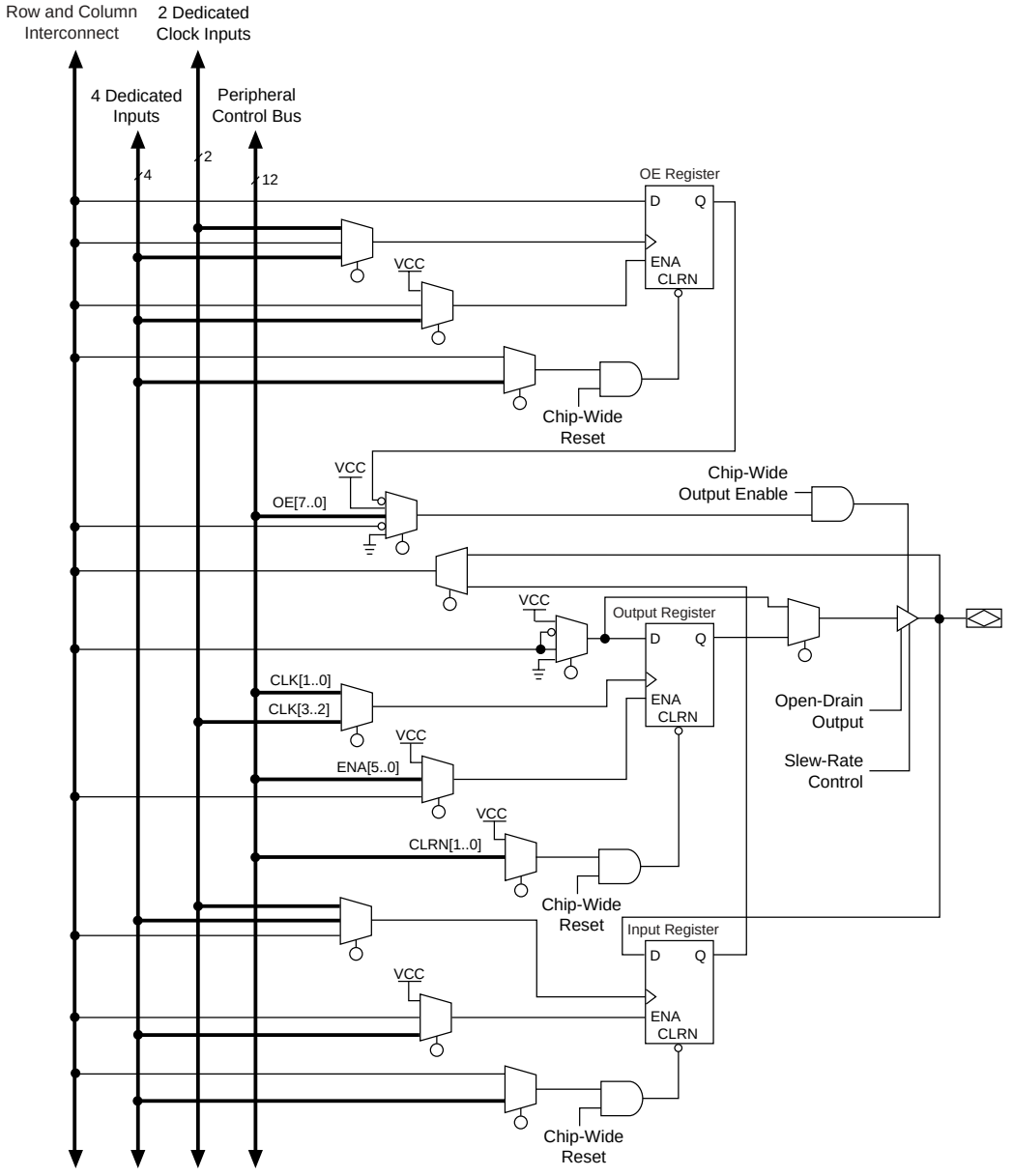


Table 12 describes the FLEX 10K device supply voltages and MultiVolt I/O support levels.

Table 12. Supply Voltages & MultiVolt I/O Support Levels

Devices	Supply Voltage (V)		MultiVolt I/O Support Levels (V)	
	V_{CCINT}	V_{CCIO}	Input	Output
FLEX 10K *(1)*	5.0	5.0	3.3 or 5.0	5.0
	5.0	3.3	3.3 or 5.0	3.3 or 5.0
EPF10K50V *(1)*	3.3	3.3	3.3 or 5.0	3.3 or 5.0
EPF10K130V	3.3	3.3	3.3 or 5.0	3.3 or 5.0
FLEX 10KA *(1)*	3.3	3.3	2.5, 3.3, or 5.0	3.3 or 5.0
	3.3	2.5	2.5, 3.3, or 5.0	2.5

Note
(1) 240-pin QFP packages do not support the MultiVolt I/O features, so they do not have separate V_{CCIO} pins.

Power Sequencing & Hot-Socketing

Because FLEX 10K devices can be used in a multi-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power supplies can be powered in any order.

Signals can be driven into FLEX 10KA devices before and during power up without damaging the device. Additionally, FLEX 10KA devices do not drive out during power up. Once operating conditions are reached, FLEX 10KA devices operate as specified by the user.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

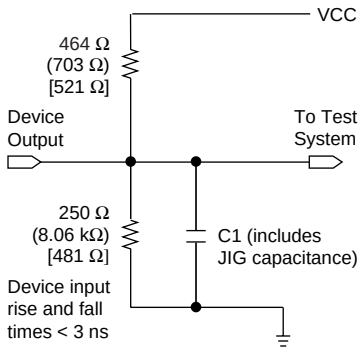
All FLEX 10K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. All FLEX 10K devices can also be configured using the JTAG pins through the BitBlaster serial download cable, or ByteBlasterMV parallel port download cable, or via hardware that uses the Jam™ programming and test language. JTAG BST can be performed before or after configuration, but not during configuration. FLEX 10K devices support the JTAG instructions shown in Table 13.

Generic Testing

Each FLEX 10K device is functionally tested. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% yield. AC test measurements for FLEX 10K devices are made under conditions equivalent to those shown in Figure 19. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 19. FLEX 10K AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers without parentheses are for 5.0-V devices or outputs. Numbers in parentheses are for 3.3-V devices or outputs. Numbers in brackets are for 2.5-V devices or outputs.



Operating Conditions

Tables 17 through 21 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 5.0-V FLEX 10K devices.

Table 17. FLEX 10K 5.0-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground *(2)*	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		PQFP, TQFP, RQFP, and BGA packages, under bias		135	° C

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms. V_{CC} must rise monotonically.
(5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(6) These values are specified under the Recommended Operation Condition shown in Table 18 on page 45.
(7) The I_{OH} parameter refers to high-level TTL or CMOS output current.
(8) The I_{OL} parameter refers to low-level TTL or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(9) This value is specified for normal device operation. The value may vary during power-up.
(10) Capacitance is sample-tested only.

Figure 20 shows the typical output drive characteristics of FLEX 10K devices with 5.0-V and 3.3-V V_{CCIO}. The output driver is compliant with the 5.0-V ***PCI Local Bus Specification, Revision 2.2*** (for 5.0-V V_{CCIO}).

Figure 20. Output Drive Characteristics of FLEX 10K Devices

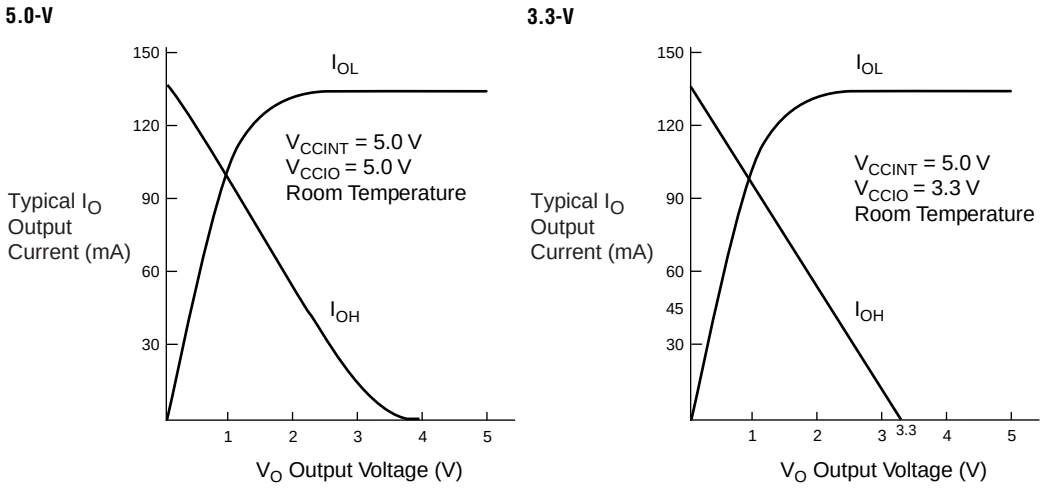


Table 24. EPF10K50V & EPF10K130V Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		5.75	V
V_{IL}	Low-level input voltage		–0.5		0.8	V
V_{OH}	3.3-V high-level TTL output voltage	I_{OH} = –8 mA DC *(8)*	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC *(8)*	V_{CCIO} – 0.2			V
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 8 mA DC *(9)*			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC *(9)*			0.2	V
I_I	Input pin leakage current	V_I = 5.3 V to –0.3 V *(10)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 5.3 V to –0.3 V *(10)*	–10		10	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load		0.3	10	mA
		V_I = ground, no load *(11)*		10		mA

Table 25. EPF10K50V & EPF10K130V Device Capacitance *(12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms. V_{CC} must rise monotonically.
(5) EPF10K50V and EPF10K130V device inputs may be driven before V_{CCINT} and V_{CCIO} are powered.
(6) Typical values are for T_A = 25° C and V_{CC} = 3.3 V.
(7) These values are specified under the EPF10K50V and EPF10K130V device Recommended Operating Conditions in Table 23 on page 48.
(8) The I_{OH} parameter refers to high-level TTL or CMOS output current.
(9) The I_{OL} parameter refers to low-level TTL or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(10) This value is specified for normal device operation. The value may vary during power-up.
(11) This parameter applies to -1 speed grade EPF10K50V devices, -2 speed grade EPF10K50V industrial temperature devices, and -2 speed grade EPF10K130V devices.
(12) Capacitance is sample-tested only.

Table 36. Interconnect Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
$t_{DIN2IOE}$	Delay from dedicated input pin to IOE control input	*(7)*
$t_{DCLK2LE}$	Delay from dedicated clock pin to LE or EAB clock	*(7)*
$t_{DIN2DATA}$	Delay from dedicated input or clock to LE or EAB data	*(7)*
$t_{DCLK2IOE}$	Delay from dedicated clock pin to IOE clock	*(7)*
t_{DIN2LE}	Delay from dedicated input pin to LE or EAB control input	*(7)*
$t_{SAMELAB}$	Routing delay for an LE driving another LE in the same LAB	
$t_{SAMEROW}$	Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row	*(7)*
$t_{SAMECOLUMN}$	Routing delay for an LE driving an IOE in the same column	*(7)*
$t_{DIFFROW}$	Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row	*(7)*
$t_{TWOROWS}$	Routing delay for a row IOE or EAB driving an LE or EAB in a different row	*(7)*
$t_{LEPERIPH}$	Routing delay for an LE driving a control signal of an IOE via the peripheral control bus	*(7)*
$t_{LABCARRY}$	Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	

Table 37. External Timing Parameters *Notes (8), (10)*

Symbol	Parameter	Conditions
t_{DRR}	Register-to-register delay via four LEs, three row interconnects, and four local interconnects	*(9)*
t_{INSU}	Setup time with global clock at IOE register	
t_{INH}	Hold time with global clock at IOE register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE register	

Table 38. External Bidirectional Timing Parameters *Note (10)*

Symbol	Parameter	Condition
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at adjacent LE register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at adjacent LE register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	
$t_{XZBIDIR}$	Synchronous IOE output buffer disable delay	
$t_{ZXBIDIR}$	Synchronous IOE output buffer enable delay, slow slew rate = off	

Table 40. EPF10K10 & EPF10K20 Device IOE Timing Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{IOD}		1.3		1.6	ns
t_{IOC}		0.5		0.7	ns
t_{IOCO}		0.2		0.2	ns
t_{IOCOMB}		0.0		0.0	ns
t_{IOSU}	2.8		3.2		ns
t_{IOH}	1.0		1.2		ns
t_{IOCLR}		1.0		1.2	ns
t_{OD1}		2.6		3.5	ns
t_{OD2}		4.9		6.4	ns
t_{OD3}		6.3		8.2	ns
t_{XZ}		4.5		5.4	ns
t_{ZX1}		4.5		5.4	ns
t_{ZX2}		6.8		8.3	ns
t_{ZX3}		8.2		10.1	ns
t_{INREG}		6.0		7.5	ns
t_{IOFD}		3.1		3.5	ns
t_{INCOMB}		3.1		3.5	ns

Table 43. EPF10K10 Device Interconnect Timing Microparameters *Note (1)*					
Symbol	**-3 Speed Grade**		**-4 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		4.8		6.2	ns
t_{DIN2LE}		2.6		3.8	ns
$t_{DIN2DATA}$		4.3		5.2	ns
$t_{DCLK2IOE}$		3.4		4.0	ns
$t_{DCLK2LE}$		2.6		3.8	ns
$t_{SAMELAB}$		0.6		0.6	ns
$t_{SAMEROW}$		3.6		3.8	ns
$t_{SAMECOLUMN}$		0.9		1.1	ns
$t_{DIFFROW}$		4.5		4.9	ns
$t_{TWOROWS}$		8.1		8.7	ns
$t_{LEPERIPH}$		3.3		3.9	ns
$t_{LABCARRY}$		0.5		0.8	ns
$t_{LABCASC}$		2.7		3.0	ns

Table 44. EPF10K20 Device Interconnect Timing Microparameters *Note (1)*					
Symbol	**-3 Speed Grade**		**-4 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		5.2		6.6	ns
t_{DIN2LE}		2.6		3.8	ns
$t_{DIN2DATA}$		4.3		5.2	ns
$t_{DCLK2IOE}$		4.3		4.0	ns
$t_{DCLK2LE}$		2.6		3.8	ns
$t_{SAMELAB}$		0.6		0.6	ns
$t_{SAMEROW}$		3.7		3.9	ns
$t_{SAMECOLUMN}$		1.4		1.6	ns
$t_{DIFFROW}$		5.1		5.5	ns
$t_{TWOROWS}$		8.8		9.4	ns
$t_{LEPERIPH}$		4.7		5.6	ns
$t_{LABCARRY}$		0.5		0.8	ns
$t_{LABCASC}$		2.7		3.0	ns

Table 50. EPF10K30, EPF10K40 & EPF10K50 Device EAB Internal Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{EABDATA1}$		1.5		1.9	ns
$t_{EABDATA2}$		4.8		6.0	ns
t_{EABWE1}		1.0		1.2	ns
t_{EABWE2}		5.0		6.2	ns
t_{EABCLK}		1.0		2.2	ns
t_{EABCO}		0.5		0.6	ns
$t_{EABBYPASS}$		1.5		1.9	ns
t_{EABSU}	1.5		1.8		ns
t_{EABH}	2.0		2.5		ns
t_{AA}		8.7		10.7	ns
t_{WP}	5.8		7.2		ns
t_{WDSU}	1.6		2.0		ns
t_{WDH}	0.3		0.4		ns
t_{WASU}	0.5		0.6		ns
t_{WAH}	1.0		1.2		ns
t_{WO}		5.0		6.2	ns
t_{DD}		5.0		6.2	ns
t_{EABOUT}		0.5		0.6	ns
t_{EABCH}	4.0		4.0		ns
t_{EABCL}	5.8		7.2		ns

Table 52. EPF10K30 Device Interconnect Timing Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{DIN2IOE}$		6.9		8.7	ns
t_{DIN2LE}		3.6		4.8	ns
$t_{DIN2DATA}$		5.5		7.2	ns
$t_{DCLK2IOE}$		4.6		6.2	ns
$t_{DCLK2LE}$		3.6		4.8	ns
$t_{SAMELAB}$		0.3		0.3	ns
$t_{SAMEROW}$		3.3		3.7	ns
$t_{SAMECOLUMN}$		2.5		2.7	ns
$t_{DIFFROW}$		5.8		6.4	ns
$t_{TWOROWS}$		9.1		10.1	ns
$t_{LEPERIPH}$		6.2		7.1	ns
$t_{LABCARRY}$		0.4		0.6	ns
$t_{LABCASC}$		2.4		3.0	ns

Table 53. EPF10K40 Device Interconnect Timing Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{DIN2IOE}$		7.6		9.4	ns
t_{DIN2LE}		3.6		4.8	ns
$t_{DIN2DATA}$		5.5		7.2	ns
$t_{DCLK2IOE}$		4.6		6.2	ns
$t_{DCLK2LE}$		3.6		4.8	ns
$t_{SAMELAB}$		0.3		0.3	ns
$t_{SAMEROW}$		3.3		3.7	ns
$t_{SAMECOLUMN}$		3.1		3.2	ns
$t_{DIFFROW}$		6.4		6.4	ns
$t_{TWOROWS}$		9.7		10.6	ns
$t_{LEPERIPH}$		6.4		7.1	ns
$t_{LABCARRY}$		0.4		0.6	ns
$t_{LABCASC}$		2.4		3.0	ns

Table 75. EPF10K50V Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		4.7		6.0		7.1		8.2	ns
t_{DIN2LE}		2.5		2.6		3.1		3.9	ns
$t_{DIN2DATA}$		4.4		5.9		6.8		7.7	ns
$t_{DCLK2IOE}$		2.5		3.9		4.7		5.5	ns
$t_{DCLK2LE}$		2.5		2.6		3.1		3.9	ns
$t_{SAMELAB}$		0.2		0.2		0.3		0.3	ns
$t_{SAMEROW}$		2.8		3.0		3.2		3.4	ns
$t_{SAMECOLUMN}$		3.0		3.2		3.4		3.6	ns
$t_{DIFFROW}$		5.8		6.2		6.6		7.0	ns
$t_{TWOROWS}$		8.6		9.2		9.8		10.4	ns
$t_{LEPERIPH}$		4.5		5.5		6.1		7.0	ns
$t_{LABCARRY}$		0.3		0.4		0.5		0.7	ns
$t_{LABCASC}$		0.0		1.3		1.6		2.0	ns

Table 76. EPF10K50V Device External Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{DRR}		11.2		14.0		17.2		21.1	ns
t_{INSU} *(2), (3)*	5.5		4.2		5.2		6.9		ns
t_{INH} *(3)*	0.0		0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	5.9	2.0	7.8	2.0	9.5	2.0	11.1	ns

Table 77. EPF10K50V Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.0		2.8		3.5		4.1		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	5.9	2.0	7.8	2.0	9.5	2.0	11.1	ns
$t_{XZBIDIR}$		8.0		9.8		11.8		14.3	ns
$t_{ZXBIDIR}$		8.0		9.8		11.8		14.3	ns

Notes to tables:
(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Tables 85 through 91 show EPF10K10A device internal and external timing parameters.

Table 85. EPF10K10A Device LE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.9		1.2		1.6	ns
t_{CLUT}		1.2		1.4		1.9	ns
t_{RLUT}		1.9		2.3		3.0	ns
t_{PACKED}		0.6		0.7		0.9	ns
t_{EN}		0.5		0.6		0.8	ns
t_{CICO}		02		0.3		0.4	ns
t_{CGEN}		0.7		0.9		1.1	ns
t_{CGENR}		0.7		0.9		1.1	ns
t_{CASC}		1.0		1.2		1.7	ns
t_{C}		1.2		1.4		1.9	ns
t_{CO}		0.5		0.6		0.8	ns
t_{COMB}		0.5		0.6		0.8	ns
t_{SU}	1.1		1.3		1.7		ns
t_{H}	0.6		0.7		0.9		ns
t_{PRE}		0.5		0.6		0.9	ns
t_{CLR}		0.5		0.6		0.9	ns
t_{CH}	3.0		3.5		4.0		ns
t_{CL}	3.0		3.5		4.0		ns

Table 86. EPF10K10A Device IOE Timing Microparameters *Note (1)* **(Part 1 of 2)**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
		1.3		1.5		2.0	ns
t_{IOC}		0.2		0.3		0.3	ns
t_{IOCO}		0.2		0.3		0.4	ns
t_{IOCOMB}		0.6		0.7		0.9	ns
t_{IOSU}	0.8		1.0		1.3		ns

Table 86. EPF10K10A Device IOE Timing Microparameters *Note (1)* *(Part 2 of 2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{IOH}	0.8		1.0		1.3		ns
t_{IOCLR}		1.2		1.4		1.9	ns
t_{OD1}		1.2		1.4		1.9	ns
t_{OD2}		2.9		3.5		4.7	ns
t_{OD3}		6.6		7.8		10.5	ns
t_{XZ}		1.2		1.4		1.9	ns
t_{ZX1}		1.2		1.4		1.9	ns
t_{ZX2}		2.9		3.5		4.7	ns
t_{ZX3}		6.6		7.8		10.5	ns
t_{INREG}		5.2		6.3		8.4	ns
t_{IOFD}		3.1		3.8		5.0	ns
t_{INCOMB}		3.1		3.8		5.0	ns

Table 103. EPF10K100A Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		4.8		5.4		6.0	ns
t_{DIN2LE}		2.0		2.4		2.7	ns
$t_{DIN2DATA}$		2.4		2.7		2.9	ns
$t_{DCLK2IOE}$		2.6		3.0		3.5	ns
$t_{DCLK2LE}$		2.0		2.4		2.7	ns
$t_{SAMELAB}$		0.1		0.1		0.1	ns
$t_{SAMEROW}$		1.5		1.7		1.9	ns
$t_{SAMECOLUMN}$		5.5		6.5		7.4	ns
$t_{DIFFROW}$		7.0		8.2		9.3	ns
$t_{TWOROWS}$		8.5		9.9		11.2	ns
$t_{LEPERIPH}$		3.9		4.2		4.5	ns
$t_{LABCARRY}$		0.2		0.2		0.3	ns
$t_{LABCASC}$		0.4		0.5		0.6	ns

Table 104. EPF10K100A Device External Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		12.5		14.5		17.0	ns
t_{INSU} *(2)*, *(3)*	3.7		4.5		5.1		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	5.3	2.0	6.1	2.0	7.2	ns

Table 105. EPF10K100A Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	4.9		5.8		6.8		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	5.3	2.0	6.1	2.0	7.2	ns
$t_{XZBIDIR}$		7.4		8.6		10.1	ns
$t_{ZXBIDIR}$		7.4		8.6		10.1	ns

Notes to tables:
(1) All timing parameters are described in Tables 32 through 37 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. Figure 31 illustrates the incoming and generated clock specifications.

Figure 31. Specifications for the Incoming & Generated Clocks

The t_I parameter refers to the nominal input clock period; the t_O parameter refers to the nominal output clock period.

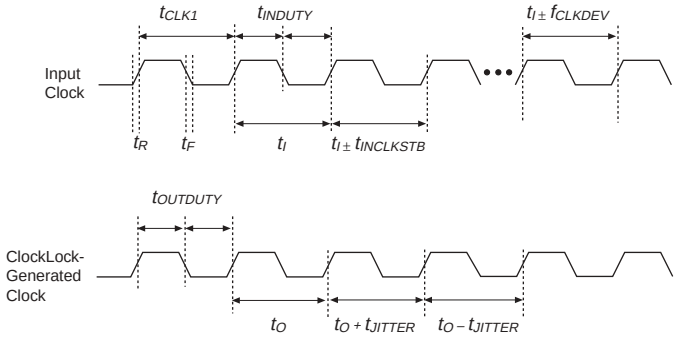


Table 113 summarizes the ClockLock and ClockBoost parameters.

Table 113. ClockLock & ClockBoost Parameters (Part 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
t_R	Input rise time			2	ns
t_F	Input fall time			2	ns
t_{INDUTY}	Input duty cycle	45		55	%
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)	30		80	MHz
t_{CLK1}	Input clock period (ClockBoost clock multiplication factor equals 1)	12.5		33.3	ns
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)	16		50	MHz
t_{CLK2}	Input clock period (ClockBoost clock multiplication factor equals 2)	20		62.5	ns

Notes: