Intel - EPF10K20RC240-4N Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	144
Number of Logic Elements/Cells	1152
Total RAM Bits	12288
Number of I/O	189
Number of Gates	63000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-RQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k20rc240-4n

Email: info@E-XFL.COM
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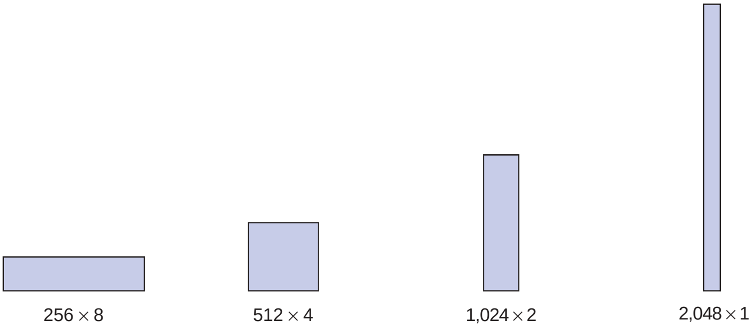
Logic functions are implemented by programming the EAB with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of EABs. The large capacity of EABs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or field-programmable gate array (FPGA) RAM blocks. For example, a single EAB can implement a 4 × 4 multiplier with eight inputs and eight outputs. Parameterized functions such as LPM functions can automatically take advantage of the EAB.

The EAB provides advantages over FPGAs, which implement on-board RAM as arrays of small, distributed RAM blocks. These FPGA RAM blocks contain delays that are less predictable as the size of the RAM increases. In addition, FPGA RAM blocks are prone to routing problems because small blocks of RAM must be connected together to make larger blocks. In contrast, EABs can be used to implement large, dedicated blocks of RAM that eliminate these timing and routing concerns.

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (`WE`) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the `WE` signal. In contrast, the EAB's synchronous RAM generates its own `WE` signal and is self-timed with respect to the global clock. A circuit using the EAB's self-timed RAM need only meet the setup and hold time specifications of the global clock.

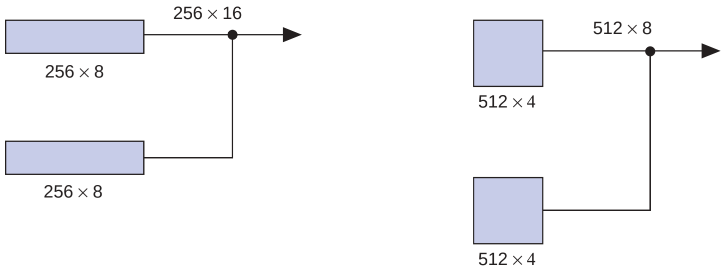
When used as RAM, each EAB can be configured in any of the following sizes: 256 × 8, 512 × 4, 1,024 × 2, or 2,048 × 1. See Figure 2.

Figure 2. EAB Memory Configurations



Larger blocks of RAM are created by combining multiple EABs. For example, two 256 × 8 RAM blocks can be combined to form a 256 × 16 RAM block; two 512 × 4 blocks of RAM can be combined to form a 512 × 8 RAM block. See Figure 3.

Figure 3. Examples of Combining EABs

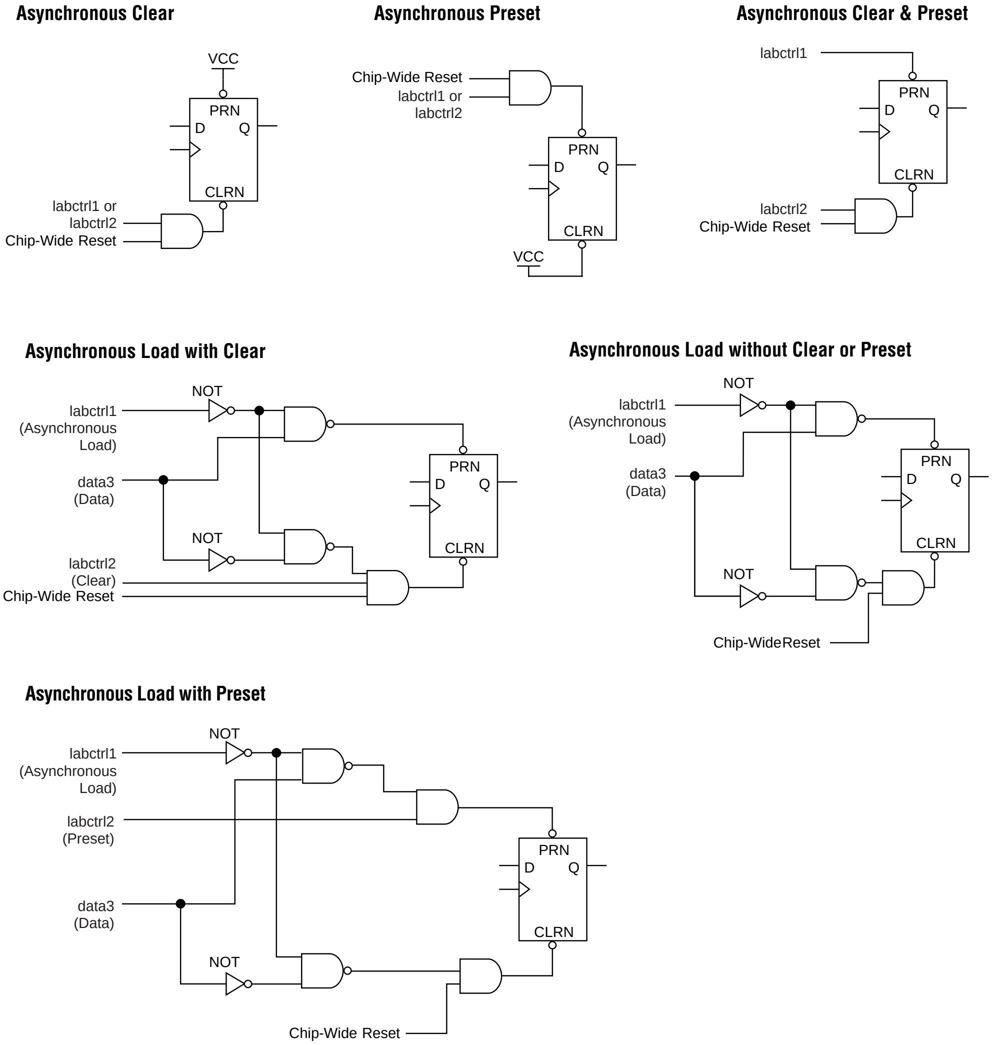


If necessary, all EABs in a device can be cascaded to form a single RAM block. EABs can be cascaded to form RAM blocks of up to 2,048 words without impacting timing. Altera's software automatically combines EABs to meet a designer's RAM specifications.

EABs provide flexible options for driving and controlling clock signals. Different clocks can be used for the EAB inputs and outputs. Registers can be independently inserted on the data input, EAB output, or the address and `WE` inputs. The global signals and the EAB local interconnect can drive the `WE` signal. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control the `WE` signal or the EAB clock signals.

Each EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs. See Figure 4.

Figure 10. LE Clear & Preset Modes



Asynchronous Clear

Asynchronous Preset

Asynchronous Clear & Preset

Asynchronous Load with Clear

Asynchronous Load without Clear or Preset

Asynchronous Load with Preset

Asynchronous Clear

The flipflop can be cleared by either `LABCTRL1` or `LABCTRL2`. In this mode, the preset signal is tied to V_{CC} to deactivate it.

Asynchronous Preset

An asynchronous preset is implemented as either an asynchronous load, or with an asynchronous clear. If `DATA3` is tied to V_{CC}, asserting `LABCTRL1` asynchronously loads a one into the register. Alternatively, the Altera software can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two `LABCTRL` signals, the `DATA3` input is not needed and can be used for one of the LE operating modes.

Asynchronous Preset & Clear

When implementing asynchronous clear and preset, `LABCTRL1` controls the preset and `LABCTRL2` controls the clear. `DATA3` is tied to V_{CC}, therefore, asserting `LABCTRL1` asynchronously loads a one into the register, effectively presetting the register. Asserting `LABCTRL2` clears the register.

Asynchronous Load with Clear

When implementing an asynchronous load in conjunction with the clear, `LABCTRL1` implements the asynchronous load of `DATA3` by controlling the register preset and clear. `LABCTRL2` implements the clear by controlling the register clear; `LABCTRL2` does not have to feed the preset circuits.

Asynchronous Load with Preset

When implementing an asynchronous load in conjunction with preset, the Altera software provides preset control by using the clear and inverting the input and output of the register. Asserting `LABCTRL2` presets the register, while asserting `LABCTRL1` loads the register. The Altera software inverts the signal that drives `DATA3` to account for the inversion of the register's output.

Asynchronous Load without Preset or Clear

When implementing an asynchronous load without preset or clear, `LABCTRL1` implements the asynchronous load of `DATA3` by controlling the register preset and clear.

FastTrack Interconnect

In the FLEX 10K architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, which is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect. The row interconnect can drive I/O pins and feed other LABs in the device. The column interconnect routes signals between rows and can drive I/O pins.

A row channel can be driven by an LE or by one of three column channels. These four signals feed dual 4-to-1 multiplexers that connect to two specific row channels. These multiplexers, which are connected to each LE, allow column channels to drive row channels even when all eight LEs in an LAB drive the row interconnect.

Each column of LABs is served by a dedicated column interconnect. The column interconnect can then drive I/O pins or another row's interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must be routed to the row interconnect before it can enter an LAB or EAB. Each row channel that is driven by an IOE or EAB can drive one specific column channel.

Access to row and column channels can be switched between LEs in adjacent pairs of LABs. For example, an LE in one LAB can drive the row and column channels normally driven by a particular LE in the adjacent LAB in the same row, and vice versa. This routing flexibility enables routing resources to be used more efficiently. See Figure 11.

I/O Element

An I/O element (IOE) contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. In some cases, using an LE register for an input register will result in a faster setup time than using an IOE register. IOEs can be used as input, output, or bidirectional pins. For bidirectional registered I/O implementation, the output register should be in the IOE and, the data input and output enable register should be LE registers placed adjacent to the bidirectional pin. The Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Figure 13 shows the bidirectional I/O registers.

Figure 15. FLEX 10K Column-to-IOE Connections

The values for m and n are provided in Table 11.

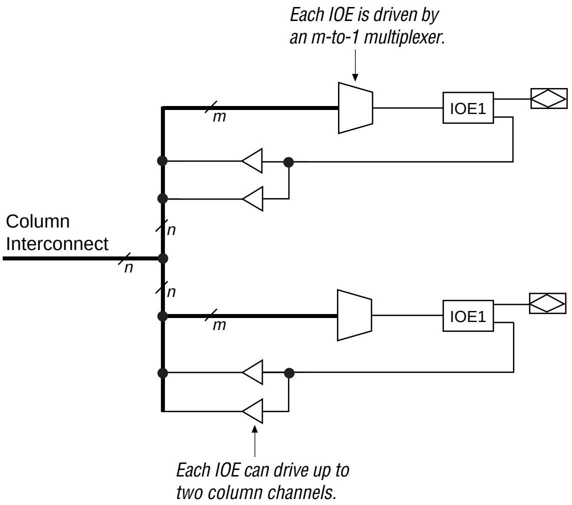


Table 11 lists the FLEX 10K column-to-IOE interconnect resources.

Table 11. FLEX 10K Column-to-IOE Interconnect Resources

Device	Channels per Column (*n*)	Column Channel per Pin (*m*)
EPF10K10 EPF10K10A	24	16
EPF10K20	24	16
EPF10K30 EPF10K30A	24	16
EPF10K40	24	16
EPF10K50 EPF10K50V	24	16
EPF10K70	24	16
EPF10K100 EPF10K100A	24	16
EPF10K130V	32	24
EPF10K250A	40	32

Tables 22 through 25 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for EPF10K50V and EPF10K130V devices.

Table 22. EPF10K50V & EPF10K130V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground *(2)*	–0.5	4.6	V
V_I	DC input voltage		–2.0	5.75	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		RQFP and BGA packages, under bias		135	° C

Table 23. EPF10K50V & EPF10K130V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
V_{CCIO}	Supply voltage for output buffers	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
V_I	Input voltage	*(5)*	-0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 27. FLEX 10KA 3.3-V Device Recommended Operating Conditions					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3)*, *(4)*	2.30 (2.30)	2.70 (2.70)	V
V_I	Input voltage	*(5)*	–0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 28. FLEX 10KA 3.3-V Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		1.7 or 0.5 × V_{CCINT}, whichever is lower		5.75	V
V_{IL}	Low-level input voltage		–0.5		0.3 × V_{CCINT}	V
V_{OH}	3.3-V high-level TTL output voltage	I_{OH} = –11 mA DC, V_{CCIO} = 3.00 V *(8)*	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(8)*	V_{CCIO} – 0.2			V
	3.3-V high-level PCI output voltage	I_{OH} = –0.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(8)*	0.9 × V_{CCIO}			V
	2.5-V high-level output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 2.30 V *(8)*	2.1			V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V *(8)*	2.0			V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V *(8)*	1.7			V
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 9 mA DC, V_{CCIO} = 3.00 V *(9)*			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(9)*			0.2	V
	3.3-V low-level PCI output voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(9)*			0.1 × V_{CCIO}	V
	2.5-V low-level output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V *(9)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(9)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(9)*			0.7	V
I_I	Input pin leakage current	V_I = 5.3 V to –0.3 V *(10)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 5.3 V to –0.3 V *(10)*	–10		10	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load		0.3	10	mA
		V_I = ground, no load *(11)*		10		mA

Table 32. LE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions
t_{SU}	LE register setup time for data and enable signals before clock; LE register recovery time after asynchronous clear, preset, or load	
t_{H}	LE register hold time for data and enable signals after clock	
t_{PRE}	LE register preset delay	
t_{CLR}	LE register clear delay	
t_{CH}	Minimum clock high time from clock pin	
t_{CL}	Minimum clock low time from clock pin	

Table 33. IOE Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
t_{IOD}	IOE data delay	
t_{IOC}	IOE register control signal delay	
t_{IOCO}	IOE register clock-to-output delay	
t_{IOCOMB}	IOE combinatorial delay	
t_{IOSU}	IOE register setup time for data and enable signals before clock; IOE register recovery time after asynchronous clear	
t_{IOH}	IOE register hold time for data and enable signals after clock	
t_{IOCLR}	IOE register clear time	
t_{OD1}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = V_{CCINT}	C1 = 35 pF *(2)*
t_{OD2}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = low voltage	C1 = 35 pF *(3)*
t_{OD3}	Output buffer and pad delay, slow slew rate = on	C1 = 35 pF *(4)*
t_{XZ}	IOE output buffer disable delay	
t_{ZX1}	IOE output buffer enable delay, slow slew rate = off, V_{CCIO} = V_{CCINT}	C1 = 35 pF *(2)*
t_{ZX2}	IOE output buffer enable delay, slow slew rate = off, V_{CCIO} = low voltage	C1 = 35 pF *(3)*
t_{ZX3}	IOE output buffer enable delay, slow slew rate = on	C1 = 35 pF *(4)*
t_{INREG}	IOE input pad and buffer to IOE register delay	
t_{IOFD}	IOE register feedback delay	
t_{INCOMB}	IOE input pad and buffer to FastTrack Interconnect delay	

Table 42. EPF10K10 & EPF10K20 Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{EABAA}		13.7		17.0	ns
$t_{EABRCCOMB}$	13.7		17.0		ns
$t_{EABRCREG}$	9.7		11.9		ns
t_{EABWP}	5.8		7.2		ns
$t_{EABWCCOMB}$	7.3		9.0		ns
$t_{EABWCREG}$	13.0		16.0		ns
t_{EABDD}		10.0		12.5	ns
$t_{EABDATACO}$		2.0		3.4	ns
$t_{EABDATASU}$	5.3		5.6		ns
$t_{EABDATAH}$	0.0		0.0		ns
$t_{EABWESU}$	5.5		5.8		ns
t_{EABWEH}	0.0		0.0		ns
$t_{EABWDSU}$	5.5		5.8		ns
t_{EABWDH}	0.0		0.0		ns
$t_{EABWASU}$	2.1		2.7		ns
t_{EABWAH}	0.0		0.0		ns
t_{EABWO}		9.5		11.8	ns

Tables 71 through 77 show EPF10K50V device internal and external timing parameters.

Table 71. EPF10K50V Device LE Timing Microparameters Note (1)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.9		1.0		1.3		1.6	ns
t_{CLUT}		0.1		0.5		0.6		0.6	ns
t_{RLUT}		0.5		0.8		0.9		1.0	ns
t_{PACKED}		0.4		0.4		0.5		0.7	ns
t_{EN}		0.7		0.9		1.1		1.4	ns
t_{CICO}		0.2		0.2		0.2		0.3	ns
t_{CGEN}		0.8		0.7		0.8		1.2	ns
t_{CGENR}		0.4		0.3		0.3		0.4	ns
t_{CASC}		0.7		0.7		0.8		0.9	ns
t_{C}		0.3		1.0		1.3		1.5	ns
t_{CO}		0.5		0.7		0.9		1.0	ns
t_{COMB}		0.4		0.4		0.5		0.6	ns
t_{SU}	0.8		1.6		2.2		2.5		ns
t_{H}	0.5		0.8		1.0		1.4		ns
t_{PRE}		0.8		0.4		0.5		0.5	ns
t_{CLR}		0.8		0.4		0.5		0.5	ns
t_{CH}	2.0		4.0		4.0		4.0		ns
t_{CL}	2.0		4.0		4.0		4.0		ns

Table 74. EPF10K50V Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{EABAA}		9.5		13.6		16.5		20.8	ns
$t_{EABRCCOMB}$	9.5		13.6		16.5		20.8		ns
$t_{EABRCREG}$	6.1		8.8		10.8		13.4		ns
t_{EABWP}	6.0		4.9		6.0		7.4		ns
$t_{EABWCCOMB}$	6.2		6.1		7.5		9.2		ns
$t_{EABWCREG}$	12.0		11.6		14.2		17.4		ns
t_{EABDD}		6.8		9.7		11.8		14.9	ns
$t_{EABDATACO}$		1.0		1.4		1.8		2.2	ns
$t_{EABDATASU}$	5.3		4.6		5.6		6.9		ns
$t_{EABDATAH}$	0.0		0.0		0.0		0.0		ns
$t_{EABWESU}$	4.4		4.8		5.8		7.2		ns
t_{EABWEH}	0.0		0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.8		1.1		1.4		2.1		ns
t_{EABWDH}	0.0		0.0		0.0		0.0		ns
$t_{EABWASU}$	4.5		4.6		5.6		7.4		ns
t_{EABWAH}	0.0		0.0		0.0		0.0		ns
t_{EABWO}		5.1		9.4		11.4		14.0	ns

Table 89. EPF10K10A Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		4.2		5.0		6.5	ns
t_{DIN2LE}		2.2		2.6		3.4	ns
$t_{DIN2DATA}$		4.3		5.2		7.1	ns
$t_{DCLK2IOE}$		4.2		4.9		6.6	ns
$t_{DCLK2LE}$		2.2		2.6		3.4	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		2.2		2.4		2.9	ns
$t_{SAMECOLUMN}$		0.8		1.0		1.4	ns
$t_{DIFFROW}$		3.0		3.4		4.3	ns
$t_{TWOROWS}$		5.2		5.8		7.2	ns
$t_{LEPERIPH}$		1.8		2.2		2.8	ns
$t_{LABCARRY}$		0.5		0.5		0.7	ns
$t_{LABCASC}$		0.9		1.0		1.5	ns

Table 90. EPF10K10A External Reference Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		10.0		12.0		16.0	ns
t_{INSU} *(2)*, *(3)*	1.6		2.1		2.8		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	5.8	2.0	6.9	2.0	9.2	ns

Table 91. EPF10K10A Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.4		3.3		4.5		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	5.8	2.0	6.9	2.0	9.2	ns
$t_{XZBIDIR}$		6.3		7.5		9.9	ns
$t_{ZXBIDIR}$		6.3		7.5		9.9	ns

Table 96. EPF10K30A Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		3.9		4.4		5.1	ns
t_{DIN2LE}		1.2		1.5		1.9	ns
$t_{DIN2DATA}$		3.2		3.6		4.5	ns
$t_{DCLK2IOE}$		3.0		3.5		4.6	ns
$t_{DCLK2LE}$		1.2		1.5		1.9	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		2.3		2.4		2.7	ns
$t_{SAMECOLUMN}$		1.3		1.4		1.9	ns
$t_{DIFFROW}$		3.6		3.8		4.6	ns
$t_{TWOROWS}$		5.9		6.2		7.3	ns
$t_{LEPERIPH}$		3.5		3.8		4.1	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.9		1.1		1.4	ns

Table 97. EPF10K30A External Reference Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		11.0		13.0		17.0	ns
t_{INSU} *(2), (3)*	2.5		3.1		3.9		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	5.4	2.0	6.2	2.0	8.3	ns

Table 98. EPF10K30A Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	4.2		4.9		6.8		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	5.4	2.0	6.2	2.0	8.3	ns
$t_{XZBIDIR}$		6.2		7.5		9.8	ns
$t_{ZXBIDIR}$		6.2		7.5		9.8	ns

Table 109. EPF10K250A Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		6.1		6.8		8.2	ns
$t_{EABRCCOMB}$	6.1		6.8		8.2		ns
$t_{EABRCREG}$	4.6		5.1		6.1		ns
t_{EABWP}	5.6		6.4		7.5		ns
$t_{EABWCCOMB}$	5.8		6.6		7.9		ns
$t_{EABWCREG}$	15.8		17.8		21.0		ns
t_{EABDD}		5.7		6.4		7.8	ns
$t_{EABDATACO}$		0.7		0.8		1.0	ns
$t_{EABDATASU}$	4.5		5.1		5.9		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	8.2		9.3		10.9		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.7		1.8		2.1		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	0.9		0.9		1.0		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		5.3		6.0		7.4	ns

Table 110. EPF10K250A Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		7.8		8.5		9.4	ns
t_{DIN2LE}		2.7		3.1		3.5	ns
$t_{DIN2DATA}$		1.6		1.6		1.7	ns
$t_{DCLK2IOE}$		3.6		4.0		4.6	ns
$t_{DCLK2LE}$		2.7		3.1		3.5	ns
$t_{SAMELAB}$		0.2		0.3		0.3	ns
$t_{SAMEROW}$		6.7		7.3		8.2	ns
$t_{SAMECOLUMN}$		2.5		2.7		3.0	ns
$t_{DIFFROW}$		9.2		10.0		11.2	ns
$t_{TWOROWS}$		15.9		17.3		19.4	ns
$t_{LEPERIPH}$		7.5		8.1		8.9	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.4		0.4		0.5	ns

Table 111. EPF10K250A Device External Reference Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		15.0		17.0		20.0	ns
t_{INSU} (2), (3)	6.9		8.0		9.4		ns
t_{INH} (3)	0.0		0.0		0.0		ns
t_{OUTCO} (3)	2.0	8.0	2.0	8.9	2.0	10.4	ns

Table 112. EPF10K250A Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	9.3		10.6		12.7		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	8.0	2.0	8.9	2.0	10.4	ns
$t_{XZBIDIR}$		10.8		12.2		14.2	ns
$t_{ZXBIDIR}$		10.8		12.2		14.2	ns

Table 113. ClockLock & ClockBoost Parameters (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
$f_{CLKDEV1}$	Input deviation from user specification in MAX+PLUS II (ClockBoost clock multiplication factor equals 1) *(1)*			±1	MHz
$f_{CLKDEV2}$	Input deviation from user specification in MAX+PLUS II (ClockBoost clock multiplication factor equals 2) *(1)*			±0.5	MHz
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)			100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock *(2)*			10	µs
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock *(3)*			1	ns
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock	40	50	60	%

Notes:

(1) To implement the ClockLock and ClockBoost circuitry with the MAX+PLUS II software, designers must specify the input frequency. The MAX+PLUS II software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The f_{CLKDEV} parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.

(2) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the t_{LOCK} value is less than the time required for configuration.

(3) The t_{JITTER} specification is measured under long-term observation.

Power Consumption

The supply power (P) for FLEX 10K devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

Typical $I_{CCSTANDBY}$ values are shown as I_{CC0} in the FLEX 10K device DC operating conditions tables on pages 46, 49, and 52 of this data sheet. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value is calculated based on the amount of current that each LE typically consumes. The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

☞ Compared to the rest of the device, the embedded array consumes a negligible amount of power. Therefore, the embedded array can be ignored when calculating supply current.

The $I_{CCACTIVE}$ value is calculated with the following equation:

$$I_{CCACTIVE} = K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}} \times \frac{\mu A}{MHz \times LE}$$

The parameters in this equation are shown below:

Multiple FLEX 10K devices can be configured in any of the five configuration schemes by connecting the configuration enable (`nCE`) and configuration enable output (`nCEO`) pins on each device.

Table 116. Data Sources for Configuration

Configuration Scheme	Data Source
Configuration device	EPC1, EPC2, EPC16, or EPC1441 configuration device
Passive serial (PS)	BitBlaster, MasterBlaster, or ByteBlasterMV download cable, or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	BitBlaster, MasterBlaster, or ByteBlasterMV download cable, or microprocessor with Jam STAPL file or Jam Byte-Code file

Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the Altera Digital Library for pin-out information.

Revision History

The information contained in the *FLEX 10K Embedded Programmable Logic Device Family Data Sheet* version 4.2 supersedes information published in previous versions.

Version 4.2 Changes

The following change was made to version 4.2 of the *FLEX 10K Embedded Programmable Logic Device Family Data Sheet*: updated Figure 13.

Version 4.1 Changes

The following changes were made to version 4.1 of the *FLEX 10K Embedded Programmable Logic Device Family Data Sheet*.

- Updated General Description section
- Updated I/O Element section
- Updated SameFrame Pin-Outs section
- Updated Figure 16
- Updated Tables 13 and 116
- Added Note 9 to Table 19
- Added Note 10 to Table 24
- Added Note 10 to Table 28