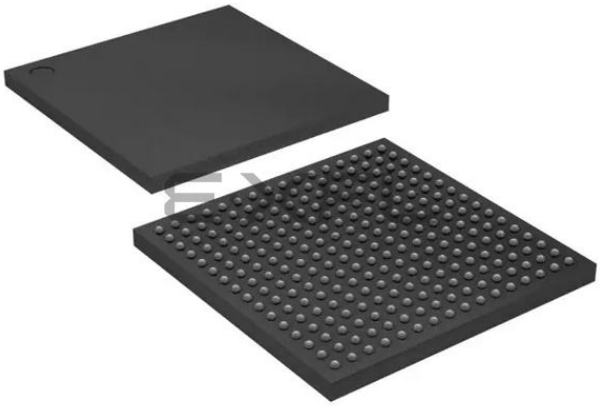

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

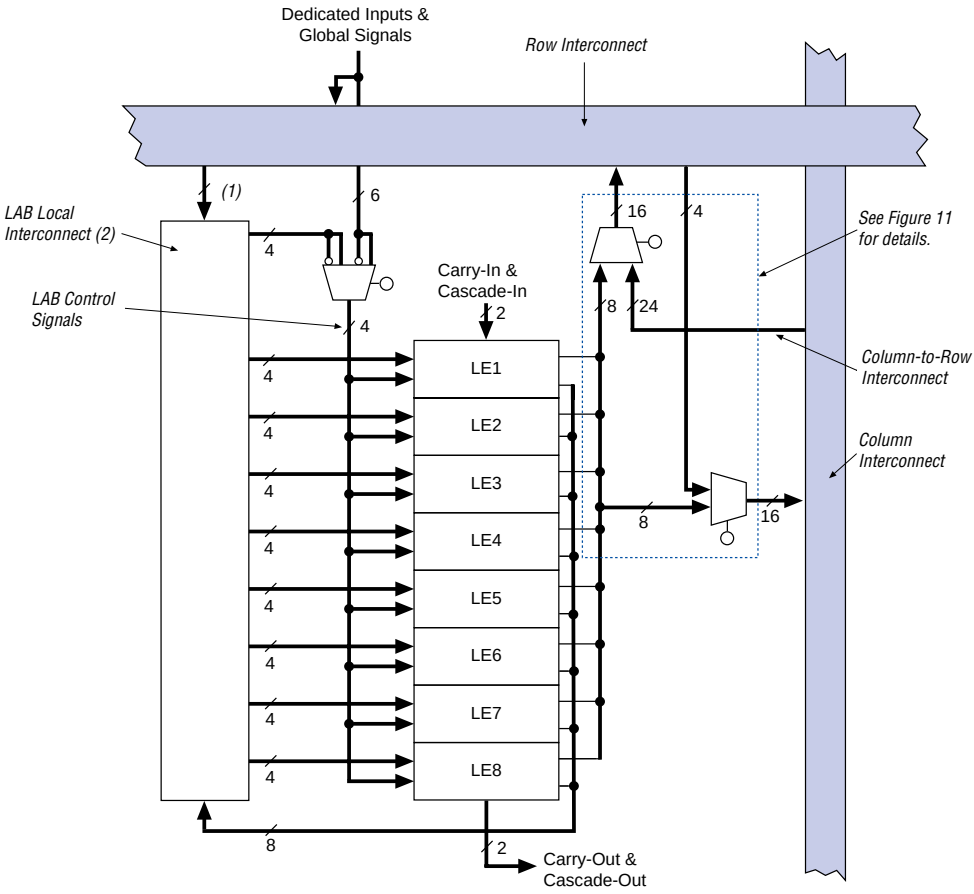
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 216 |
| Number of Logic Elements/Cells | 1728 |
| Total RAM Bits | 12288 |
| Number of I/O | 191 |
| Number of Gates | 69000 |
| Voltage - Supply | 3V ~ 3.6V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 256-BGA |
| Supplier Device Package | 256-FBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epf10k30afc256-2n |

## Logic Array Block

Each LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the FLEX 10K architecture, facilitating efficient routing with optimum device utilization and high performance. See Figure 5.

*Figure 5. FLEX 10K LAB*




*Notes:*

(1) EPF10K10, EPF10K10A, EPF10K20, EPF10K30, EPF10K30A, EPF10K40, EPF10K50, and EPF10K50V devices have 22 inputs to the LAB local interconnect channel from the row; EPF10K70, EPF10K100, EPF10K100A, EPF10K130V, and EPF10K250A devices have 26.

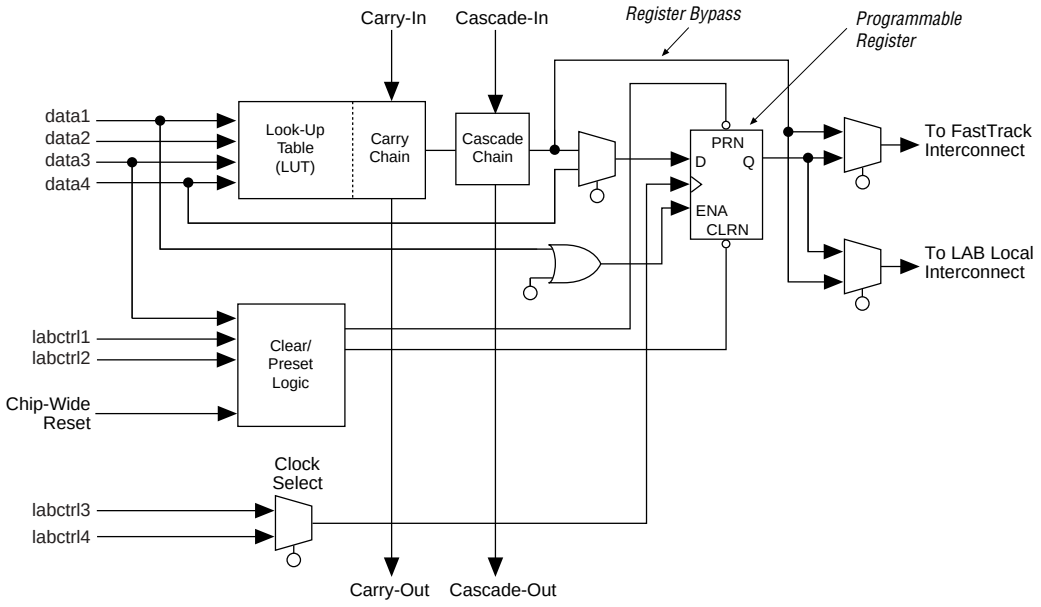
(2) EPF10K10, EPF10K10A, EPF10K20, EPF10K30, EPF10K30A, EPF10K40, EPF10K50, and EPF10K50V devices have 30 LAB local interconnect channels; EPF10K70, EPF10K100, EPF10K100A, EPF10K130V, and EPF10K250A devices have 34 LABs.

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks; the other two can be used for clear/preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I/O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I/O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

## Logic Element

The LE, the smallest unit of logic in the FLEX 10K architecture, has a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect. See Figure 6.

*Figure 6. FLEX 10K Logic Element*



### *LE Operating Modes*

The FLEX 10K LE can operate in the following four modes:

- Normal mode
- Arithmetic mode
- Up/down counter mode
- Clearable counter mode

Each of these modes uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. Three inputs to the LE provide clock, clear, and preset control for the register. The Altera software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions which use a specific LE operating mode for optimal performance.

The architecture provides a synchronous clock enable to the register in all four modes. The Altera software can set `DATA1` to enable the register synchronously, providing easy implementation of fully synchronous designs.

Figure 9 shows the LE operating modes.

During compilation, the Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six modes chosen during design entry:

- Asynchronous clear
- Asynchronous preset
- Asynchronous clear and preset
- Asynchronous load with clear
- Asynchronous load with preset
- Asynchronous load without clear or preset

In addition to the six clear and preset modes, FLEX 10K devices provide a chip-wide reset pin that can reset all registers in the device. Use of this feature is set during design entry. In any of the clear and preset modes, the chip-wide reset overrides all other signals. Registers with asynchronous presets may be preset when the chip-wide reset is asserted. Inversion can be used to implement the asynchronous preset. Figure 10 shows examples of how to enter a section of a design for the desired functionality.

### Asynchronous Preset

An asynchronous preset is implemented as either an asynchronous load, or with an asynchronous clear. If DATA3 is tied to $V_{CC}$, asserting LABCTRL1 asynchronously loads a one into the register. Alternatively, the Altera software can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

### Asynchronous Preset & Clear

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. DATA3 is tied to $V_{CC}$, therefore, asserting LABCTRL1 asynchronously loads a one into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

### Asynchronous Load with Clear

When implementing an asynchronous load in conjunction with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear; LABCTRL2 does not have to feed the preset circuits.

### Asynchronous Load with Preset

When implementing an asynchronous load in conjunction with preset, the Altera software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 presets the register, while asserting LABCTRL1 loads the register. The Altera software inverts the signal that drives DATA3 to account for the inversion of the register's output.

### Asynchronous Load without Preset or Clear

When implementing an asynchronous load without preset or clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

*Figure 11. LAB Connections to Row & Column Interconnect*

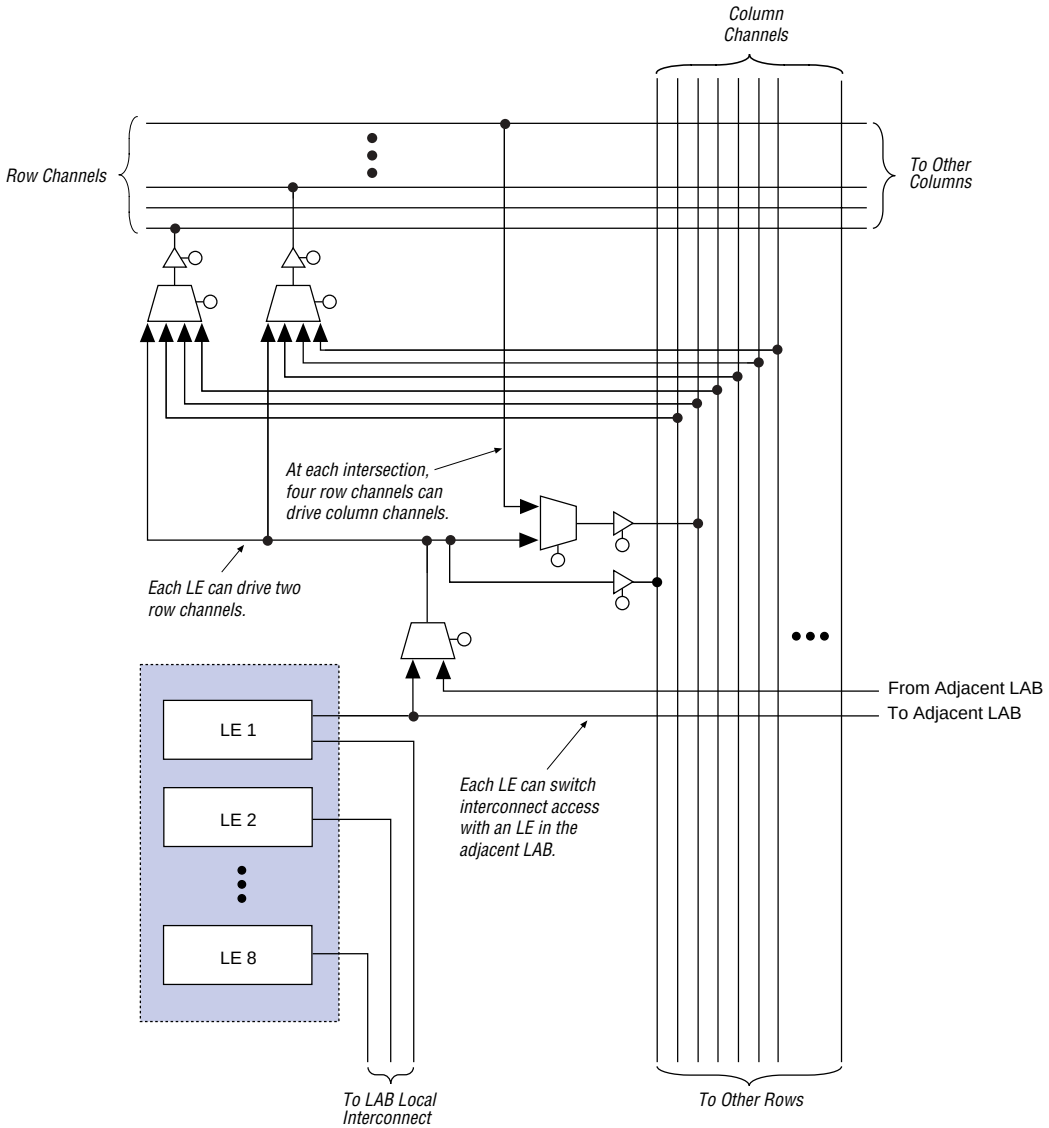
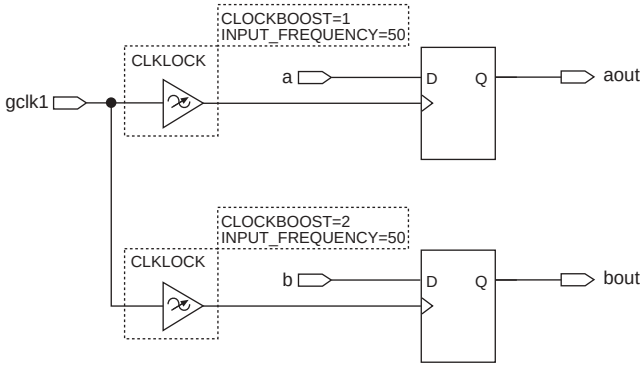


*Figure 17. Enabling ClockLock & ClockBoost in the Same Design*




To use both the ClockLock and ClockBoost circuits in the same design, designers must use Revision C EPF10K100GC503-3DX devices and MAX+PLUS II software versions 7.2 or higher. The die revision is indicated by the third digit of the nine-digit code on the top side of the device.

## Output Configuration

This section discusses the peripheral component interconnect (PCI) pull-up clamping diode option, slew-rate control, open-drain output option, MultiVolt I/O interface, and power sequencing for FLEX 10K devices. The PCI pull-up clamping diode, slew-rate control, and open-drain output options are controlled pin-by-pin via Altera logic options. The MultiVolt I/O interface is controlled by connecting $V_{CCIO}$ to a different voltage than $V_{CCINT}$. Its effect can be simulated in the Altera software via the **Global Project Device Options** dialog box (Assign menu).

### PCI Clamping Diodes

The EPF10K10A and EPF10K30A devices have a pull-up clamping diode on every I/O, dedicated input, and dedicated clock pin. PCI clamping diodes clamp the transient overshoot caused by reflected waves to the $V_{CCIO}$ value and are required for 3.3-V PCI compliance. Clamping diodes can also be used to limit overshoot in other systems.

Clamping diodes are controlled on a pin-by-pin basis via a logic option in the Altera software. When $V_{CCIO}$ is 3.3 V, a pin that has the clamping diode turned on can be driven by a 2.5-V or 3.3-V signal, but not a 5.0-V signal. When $V_{CCIO}$ is 2.5 V, a pin that has the clamping diode turned on can be driven by a 2.5-V signal, but not a 3.3-V or 5.0-V signal. However, a clamping diode can be turned on for a subset of pins, which allows devices to bridge between a 3.3-V PCI bus and a 5.0-V device.

*Table 18. FLEX 10K 5.0-V Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)* | 4.75 (4.50) | 5.25 (5.50) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 5.0-V operation | *(3)*, *(4)* | 4.75 (4.50) | 5.25 (5.50) | V |
| | Supply voltage for output buffers, 3.3-V operation | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| $V_I$ | Input voltage | | –0.5 | $V_{CCINT}$ + 0.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | For commercial use | 0 | 70 | ° C |
| | | For industrial use | –40 | 85 | ° C |
| $T_J$ | Operating temperature | For commercial use | 0 | 85 | ° C |
| | | For industrial use | –40 | 100 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

**Table 29. 3.3-V Device Capacitance of EPF10K10A & EPF10K30A Devices** *Note (12)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 12 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |

**Table 30. 3.3-V Device Capacitance of EPF10K100A Devices** *Note (12)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 10 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 15 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 10 | pF |

**Table 31. 3.3-V Device Capacitance of EPF10K250A Devices** *Note (12)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 10 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 15 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 10 | pF |

*Notes to tables:*

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC voltage input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum $V_{CC}$ rise time is 100 ms, and $V_{CC}$ must rise monotonically.
(5) FLEX 10KA device inputs may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.
(6) Typical values are for $T_A$ = 25° C and $V_{CC}$ = 3.3 V.
(7) These values are specified under the Recommended Operating Conditions shown in Table 27 on page 51.
(8) The $I_{OH}$ parameter refers to high-level TTL, PCI, or CMOS output current.
(9) The $I_{OL}$ parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(10) This value is specified for normal device operation. The value may vary during power-up.
(11) This parameter applies to all -1 speed grade commercial temperature devices and all -2 speed grade industrial-temperature devices.
(12) Capacitance is sample-tested only.

| *Table 35. EAB Timing Macroparameters* *Notes (1), (6)* | | |
|---|---|---|
| **Symbol** | **Parameter** | **Conditions** |
| $t_{EABAA}$ | EAB address access delay | |
| $t_{EABRCCOMB}$ | EAB asynchronous read cycle time | |
| $t_{EABRCREG}$ | EAB synchronous read cycle time | |
| $t_{EABWP}$ | EAB write pulse width | |
| $t_{EABWCCOMB}$ | EAB asynchronous write cycle time | |
| $t_{EABWCREG}$ | EAB synchronous write cycle time | |
| $t_{EABDD}$ | EAB data-in to data-out valid delay | |
| $t_{EABDATACO}$ | EAB clock-to-output delay when using output registers | |
| $t_{EABDATASU}$ | EAB data/address setup time before clock when using input register | |
| $t_{EABDATAH}$ | EAB data/address hold time after clock when using input register | |
| $t_{EABWESU}$ | EAB WE setup time before clock when using input register | |
| $t_{EABWEH}$ | EAB WE hold time after clock when using input register | |
| $t_{EABWDSU}$ | EAB data setup time before falling edge of write pulse when not using input registers | |
| $t_{EABWDH}$ | EAB data hold time after falling edge of write pulse when not using input registers | |
| $t_{EABWASU}$ | EAB address setup time before rising edge of write pulse when not using input registers | |
| $t_{EABWAH}$ | EAB address hold time after falling edge of write pulse when not using input registers | |
| $t_{EABWO}$ | EAB write enable to data output valid delay | |

*Table 40. EPF10K10 & EPF10K20 Device IOE Timing Microparameters* *Note (1)*

| Symbol | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| $t_{IOD}$ | | 1.3 | | 1.6 | ns |
| $t_{IOC}$ | | 0.5 | | 0.7 | ns |
| $t_{IOCO}$ | | 0.2 | | 0.2 | ns |
| $t_{IOCOMB}$ | | 0.0 | | 0.0 | ns |
| $t_{IOSU}$ | 2.8 | | 3.2 | | ns |
| $t_{IOH}$ | 1.0 | | 1.2 | | ns |
| $t_{IOCLR}$ | | 1.0 | | 1.2 | ns |
| $t_{OD1}$ | | 2.6 | | 3.5 | ns |
| $t_{OD2}$ | | 4.9 | | 6.4 | ns |
| $t_{OD3}$ | | 6.3 | | 8.2 | ns |
| $t_{XZ}$ | | 4.5 | | 5.4 | ns |
| $t_{ZX1}$ | | 4.5 | | 5.4 | ns |
| $t_{ZX2}$ | | 6.8 | | 8.3 | ns |
| $t_{ZX3}$ | | 8.2 | | 10.1 | ns |
| $t_{INREG}$ | | 6.0 | | 7.5 | ns |
| $t_{IOFD}$ | | 3.1 | | 3.5 | ns |
| $t_{INCOMB}$ | | 3.1 | | 3.5 | ns |

**Table 45. EPF10K10 & EPF10K20 Device External Timing Parameters** *Note (1)*

| Symbol | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| $t_{DRR}$ | | 16.1 | | 20.0 | ns |
| $t_{INSU}$ *(2)*, *(3)* | 5.5 | | 6.0 | | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(3)* | 2.0 | 6.7 | 2.0 | 8.4 | ns |

**Table 46. EPF10K10 Device External Bidirectional Timing Parameters** *Note (1)*

| Symbol | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 4.5 | | 5.6 | | ns |
| $t_{INHBIDIR}$ | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ | 2.0 | 6.7 | 2.0 | 8.4 | ns |
| $t_{XZBIDIR}$ | | 10.5 | | 13.4 | ns |
| $t_{ZXBIDIR}$ | | 10.5 | | 13.4 | ns |

**Table 47. EPF10K20 Device External Bidirectional Timing Parameters** *Note (1)*

| Symbol | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 4.6 | | 5.7 | | ns |
| $t_{INHBIDIR}$ | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ | 2.0 | 6.7 | 2.0 | 8.4 | ns |
| $t_{XZBIDIR}$ | | 10.5 | | 13.4 | ns |
| $t_{ZXBIDIR}$ | | 10.5 | | 13.4 | ns |

*Notes to tables:*

(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

*Table 58. EPF10K70 Device IOE Timing Microparameters* *Note (1)*

| Symbol | -2 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOC}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{IOCO}$ | | 0.4 | | 0.4 | | 0.9 | ns |
| $t_{IOCOMB}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOSU}$ | 4.5 | | 5.0 | | 6.2 | | ns |
| $t_{IOH}$ | 0.4 | | 0.5 | | 0.7 | | ns |
| $t_{IOCLR}$ | | 0.6 | | 0.7 | | 1.6 | ns |
| $t_{OD1}$ | | 3.6 | | 4.0 | | 5.0 | ns |
| $t_{OD2}$ | | 5.6 | | 6.3 | | 7.3 | ns |
| $t_{OD3}$ | | 6.9 | | 7.7 | | 8.7 | ns |
| $t_{XZ}$ | | 5.5 | | 6.2 | | 6.8 | ns |
| $t_{ZX1}$ | | 5.5 | | 6.2 | | 6.8 | ns |
| $t_{ZX2}$ | | 7.5 | | 8.5 | | 9.1 | ns |
| $t_{ZX3}$ | | 8.8 | | 9.9 | | 10.5 | ns |
| $t_{INREG}$ | | 8.0 | | 9.0 | | 10.2 | ns |
| $t_{IOFD}$ | | 7.2 | | 8.1 | | 10.3 | ns |
| $t_{INCOMB}$ | | 7.2 | | 8.1 | | 10.3 | ns |

*Table 59. EPF10K70 Device EAB Internal Microparameters* *Note (1)*

| Symbol | -2 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.3 | | 1.5 | | 1.9 | ns |
| $t_{EABDATA2}$ | | 4.3 | | 4.8 | | 6.0 | ns |
| $t_{EABWE1}$ | | 0.9 | | 1.0 | | 1.2 | ns |
| $t_{EABWE2}$ | | 4.5 | | 5.0 | | 6.2 | ns |
| $t_{EABCLK}$ | | 0.9 | | 1.0 | | 2.2 | ns |
| $t_{EABCO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{EABBYPASS}$ | | 1.3 | | 1.5 | | 1.9 | ns |
| $t_{EABSU}$ | 1.3 | | 1.5 | | 1.8 | | ns |
| $t_{EABH}$ | 1.8 | | 2.0 | | 2.5 | | ns |
| $t_{AA}$ | | 7.8 | | 8.7 | | 10.7 | ns |
| $t_{WP}$ | 5.2 | | 5.8 | | 7.2 | | ns |
| $t_{WDSU}$ | 1.4 | | 1.6 | | 2.0 | | ns |
| $t_{WDH}$ | 0.3 | | 0.3 | | 0.4 | | ns |
| $t_{WASU}$ | 0.4 | | 0.5 | | 0.6 | | ns |
| $t_{WAH}$ | 0.9 | | 1.0 | | 1.2 | | ns |
| $t_{WO}$ | | 4.5 | | 5.0 | | 6.2 | ns |
| $t_{DD}$ | | 4.5 | | 5.0 | | 6.2 | ns |
| $t_{EABOUT}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{EABCH}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{EABCL}$ | 5.2 | | 5.8 | | 7.2 | | ns |

*Table 68. EPF10K100 Device Interconnect Timing Microparameters* *Note (1)*

| Symbol | -3DX Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 10.3 | | 10.3 | | 12.2 | ns |
| $t_{DIN2LE}$ | | 4.8 | | 4.8 | | 6.0 | ns |
| $t_{DIN2DATA}$ | | 7.3 | | 7.3 | | 11.0 | ns |
| $t_{DCLK2IOE}$ without ClockLock or ClockBoost circuitry | | 6.2 | | 6.2 | | 7.7 | ns |
| $t_{DCLK2IOE}$ with ClockLock or ClockBoost circuitry | | 2.3 | | – | | – | ns |
| $t_{DCLK2LE}$ without ClockLock or ClockBoost circuitry | | 4.8 | | 4.8 | | 6.0 | ns |
| $t_{DCLK2LE}$ with ClockLock or ClockBoost circuitry | | 2.3 | | – | | – | ns |
| $t_{SAMELAB}$ | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{SAMEROW}$ | | 4.9 | | 4.9 | | 5.5 | ns |
| $t_{SAMECOLUMN}$ | | 5.1 | | 5.1 | | 5.4 | ns |
| $t_{DIFFROW}$ | | 10.0 | | 10.0 | | 10.9 | ns |
| $t_{TWOROWS}$ | | 14.9 | | 14.9 | | 16.4 | ns |
| $t_{LEPERIPH}$ | | 6.9 | | 6.9 | | 8.1 | ns |
| $t_{LABCARRY}$ | | 0.9 | | 0.9 | | 1.1 | ns |
| $t_{LABCASC}$ | | 3.0 | | 3.0 | | 3.2 | ns |

*Table 79. EPF10K130V Device IOE Timing Microparameters* *Note (1)*

| Symbol | -2 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 1.3 | | 1.6 | | 2.0 | ns |
| $t_{IOC}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{IOCO}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{IOCOMB}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOSU}$ | 2.6 | | 3.3 | | 3.8 | | ns |
| $t_{IOH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{IOCLR}$ | | 1.7 | | 2.2 | | 2.7 | ns |
| $t_{OD1}$ | | 3.5 | | 4.4 | | 5.0 | ns |
| $t_{OD2}$ | | – | | – | | – | ns |
| $t_{OD3}$ | | 8.2 | | 8.1 | | 9.7 | ns |
| $t_{XZ}$ | | 4.9 | | 6.3 | | 7.4 | ns |
| $t_{ZX1}$ | | 4.9 | | 6.3 | | 7.4 | ns |
| $t_{ZX2}$ | | – | | – | | – | ns |
| $t_{ZX3}$ | | 9.6 | | 10.0 | | 12.1 | ns |
| $t_{INREG}$ | | 7.9 | | 10.0 | | 12.6 | ns |
| $t_{IOFD}$ | | 6.2 | | 7.9 | | 9.9 | ns |
| $t_{INCOMB}$ | | 6.2 | | 7.9 | | 9.9 | ns |

*Table 82. EPF10K130V Device Interconnect Timing Microparameters* *Note (1)*

| Symbol | -2 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 8.0 | | 9.0 | | 9.5 | ns |
| $t_{DIN2LE}$ | | 2.4 | | 3.0 | | 3.1 | ns |
| $t_{DIN2DATA}$ | | 5.0 | | 6.3 | | 7.4 | ns |
| $t_{DCLK2IOE}$ | | 3.6 | | 4.6 | | 5.1 | ns |
| $t_{DCLK2LE}$ | | 2.4 | | 3.0 | | 3.1 | ns |
| $t_{SAMELAB}$ | | 0.4 | | 0.6 | | 0.8 | ns |
| $t_{SAMEROW}$ | | 4.5 | | 5.3 | | 6.5 | ns |
| $t_{SAMECOLUMN}$ | | 9.0 | | 9.5 | | 9.7 | ns |
| $t_{DIFFROW}$ | | 13.5 | | 14.8 | | 16.2 | ns |
| $t_{TWOROWS}$ | | 18.0 | | 20.1 | | 22.7 | ns |
| $t_{LEPERIPH}$ | | 8.1 | | 8.6 | | 9.5 | ns |
| $t_{LABCARRY}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{LABCASC}$ | | 0.8 | | 1.0 | | 1.2 | ns |

*Table 83. EPF10K130V Device External Timing Parameters* *Note (1)*

| Symbol | -2 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 15.0 | | 19.1 | | 24.2 | ns |
| $t_{INSU}$ *(2)*, *(3)* | 6.9 | | 8.6 | | 11.0 | | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(3)* | 2.0 | 7.8 | 2.0 | 9.9 | 2.0 | 11.3 | ns |

*Table 84. EPF10K130V Device External Bidirectional Timing Parameters* *Note (1)*

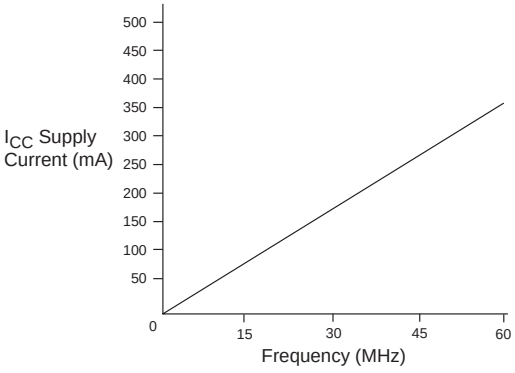
| Symbol | -2 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 6.7 | | 8.5 | | 10.8 | | ns |
| $t_{INHBIDIR}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ | 2.0 | 6.9 | 2.0 | 8.8 | 2.0 | 10.2 | ns |
| $t_{XZBIDIR}$ | | 12.9 | | 16.4 | | 19.3 | ns |
| $t_{ZXBIDIR}$ | | 12.9 | | 16.4 | | 19.3 | ns |

*Table 86. EPF10K10A Device IOE Timing Microparameters* *Note (1)* *(Part 2 of 2)*

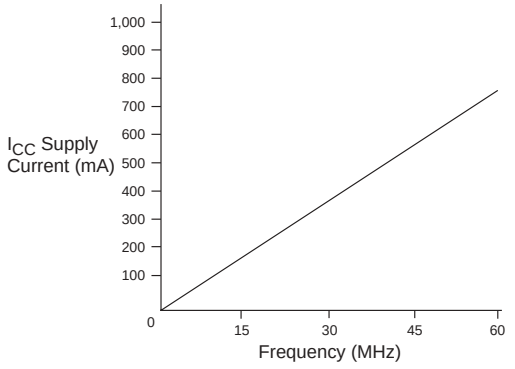
| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOH}$ | 0.8 | | 1.0 | | 1.3 | | ns |
| $t_{IOCLR}$ | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{OD1}$ | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{OD2}$ | | 2.9 | | 3.5 | | 4.7 | ns |
| $t_{OD3}$ | | 6.6 | | 7.8 | | 10.5 | ns |
| $t_{XZ}$ | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{ZX1}$ | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{ZX2}$ | | 2.9 | | 3.5 | | 4.7 | ns |
| $t_{ZX3}$ | | 6.6 | | 7.8 | | 10.5 | ns |
| $t_{INREG}$ | | 5.2 | | 6.3 | | 8.4 | ns |
| $t_{IOFD}$ | | 3.1 | | 3.8 | | 5.0 | ns |
| $t_{INCOMB}$ | | 3.1 | | 3.8 | | 5.0 | ns |

*Figure 32. $I_{CCACTIVE}$ vs. Operating Frequency (Part 1 of 3)*

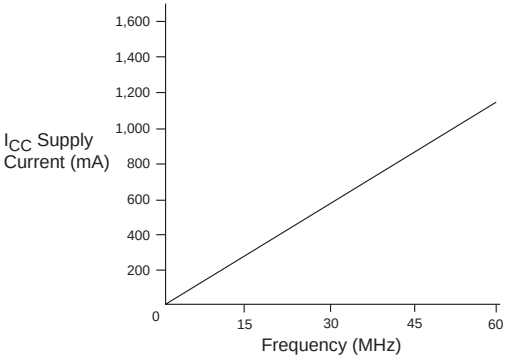
**EPF10K10**



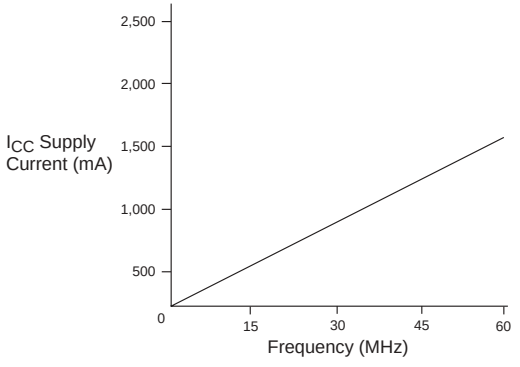

**EPF10K20**



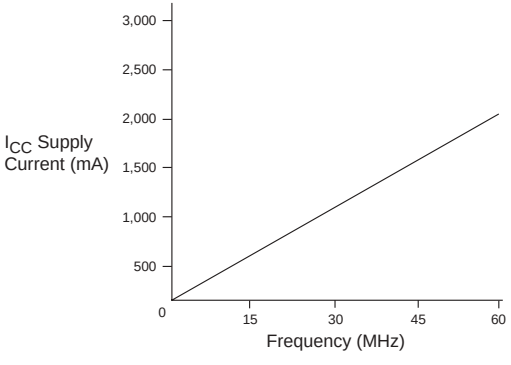

**EPF10K30**



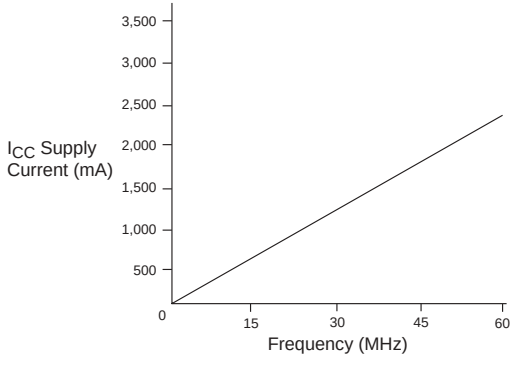

**EPF10K40**




**EPF10K50**




**EPF10K70**



101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com
Applications Hotline:
(800) 800-EPLD
Customer Marketing:
(408) 544-7104
Literature Services:
lit_req@altera.com