Intel - EPF10K30AQC240-2 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

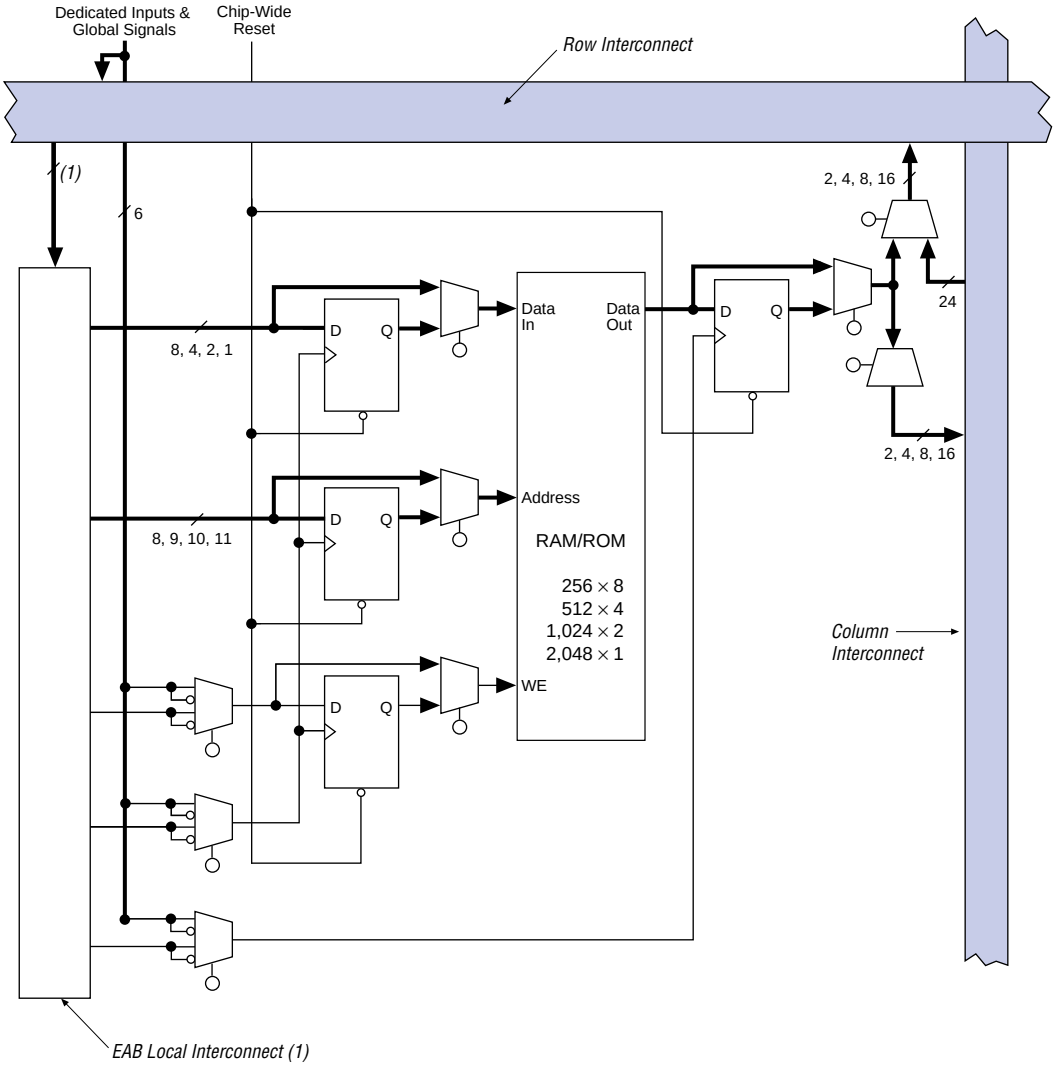
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	216
Number of Logic Elements/Cells	1728
Total RAM Bits	12288
Number of I/O	189
Number of Gates	69000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k30aqc240-2

Figure 4. FLEX 10K Embedded Array Block



Note:

(1) EPF10K10, EPF10K10A, EPF10K20, EPF10K30, EPF10K30A, EPF10K40, EPF10K50, and EPF10K50V devices have 22 EAB local interconnect channels; EPF10K70, EPF10K100, EPF10K100A, EPF10K130V, and EPF10K250A devices have 26.

Figure 7 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can either be bypassed for simple adders or be used for an accumulator function. The carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal.

Figure 7. Carry Chain Operation (n-bit Full Adder)

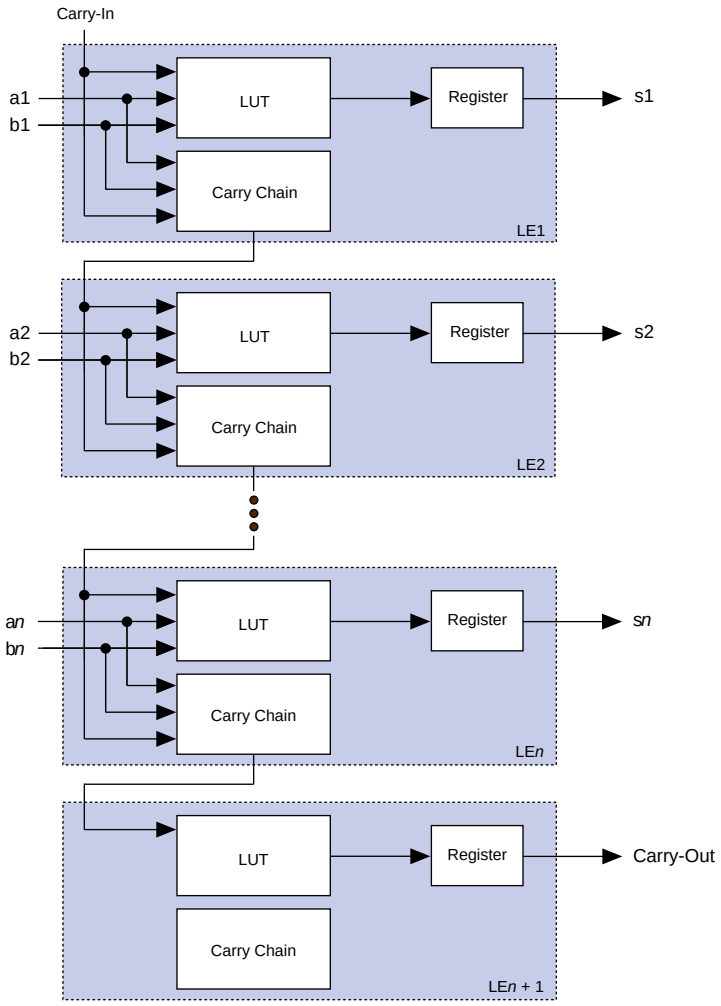
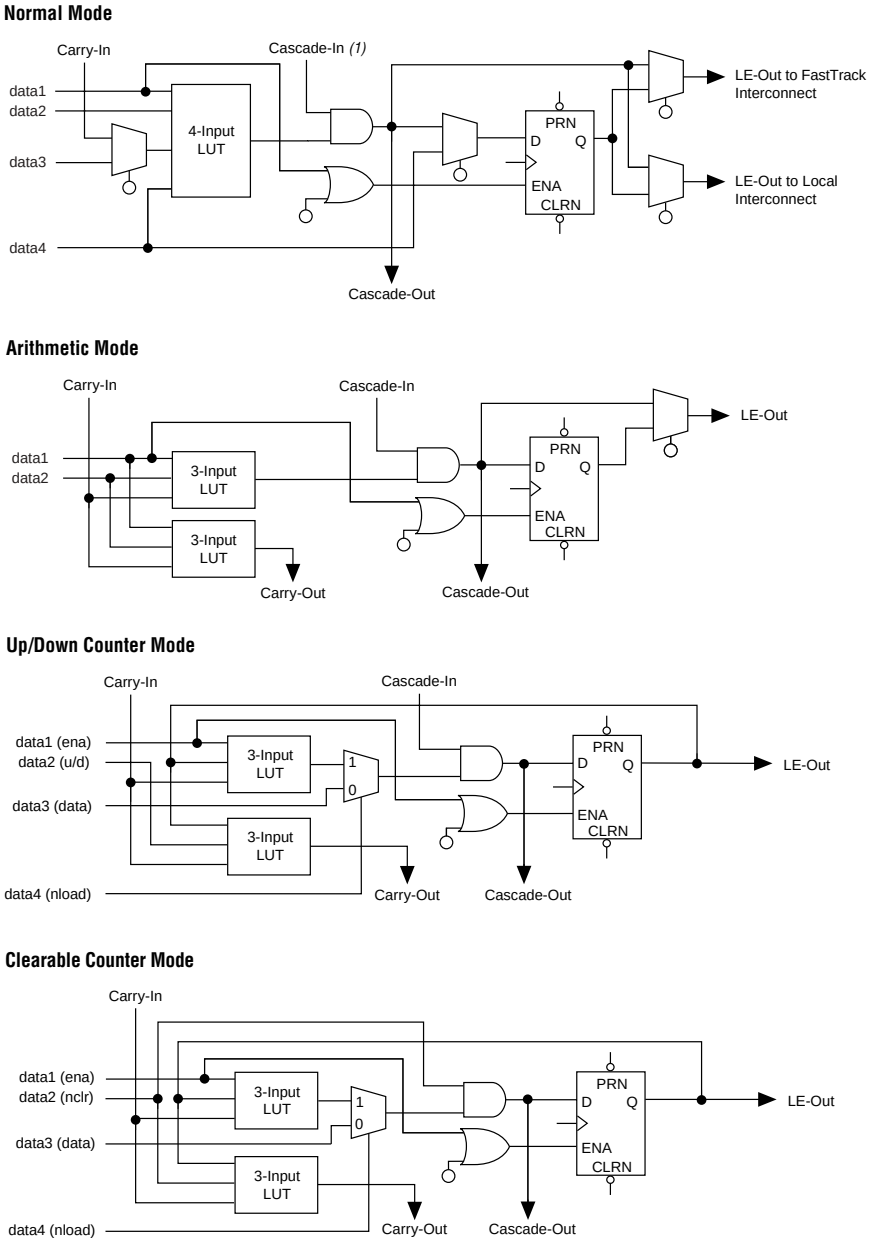


Figure 9. FLEX 10K LE Operating Modes



Note:
(1) Packed registers cannot be used with the cascade chain.

Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces system noise and adds a maximum delay of approximately 2.9 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a device-wide basis. The slow slew rate setting affects only the falling edge of the output.

Open-Drain Output Option

FLEX 10K devices provide an optional open-drain (electrically equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane. Additionally, the Altera software can convert tri-state buffers with grounded data inputs to open-drain pins automatically.

Open-drain output pins on FLEX 10K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Output pins on 5.0-V FLEX 10K devices with V_{CCIO} = 3.3 V or 5.0 V (with a pull-up resistor to the 5.0-V supply) can also drive 5.0-V CMOS input pins. In this case, the pull-up transistor will turn off when the pin voltage exceeds 3.3 V. Therefore, the pin does not have to be open-drain.

MultiVolt I/O Interface

The FLEX 10K device architecture supports the MultiVolt I/O interface feature, which allows FLEX 10K devices to interface with systems of differing supply voltages. These devices have one set of V_{CC} pins for internal operation and input buffers (VCCINT) and another set for I/O output drivers (VCCIO).

Figure 18 shows the timing requirements for the JTAG signals.

Figure 18. JTAG Waveforms

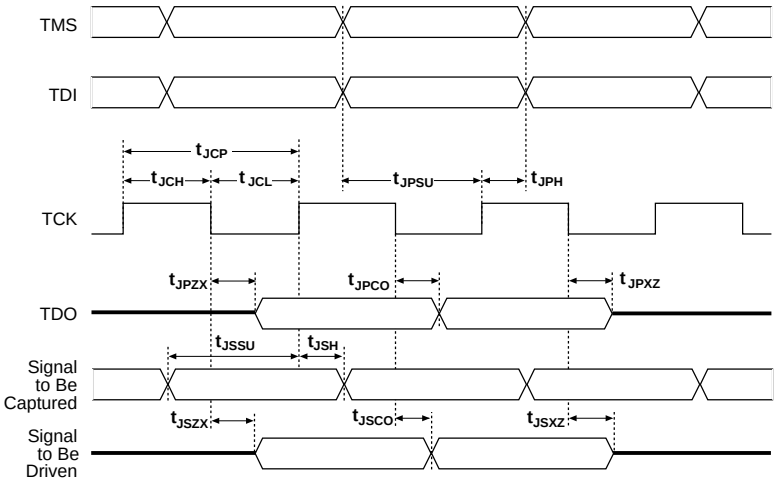


Table 16 shows the timing parameters and values for FLEX 10K devices.

Table 16. JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high-impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

Figures 25 through 27 show the delays that correspond to various paths and functions within the LE, IOE, and EAB timing models.

Figure 25. FLEX 10K Device LE Timing Model

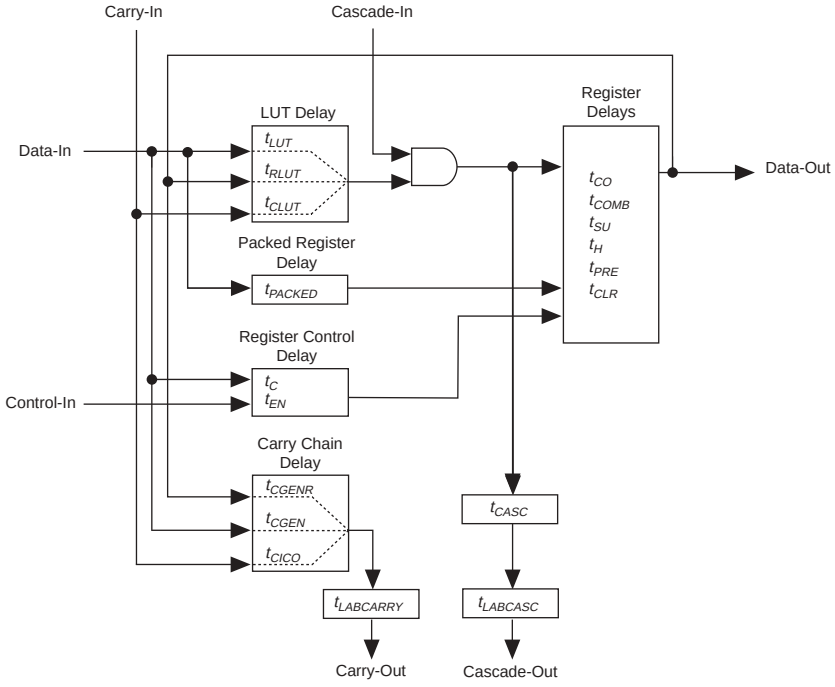


Figure 26. FLEX 10K Device IOE Timing Model

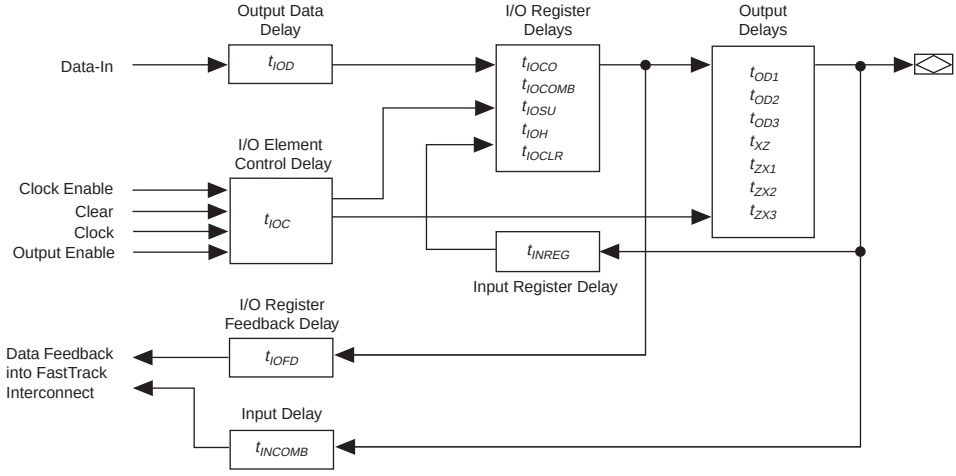
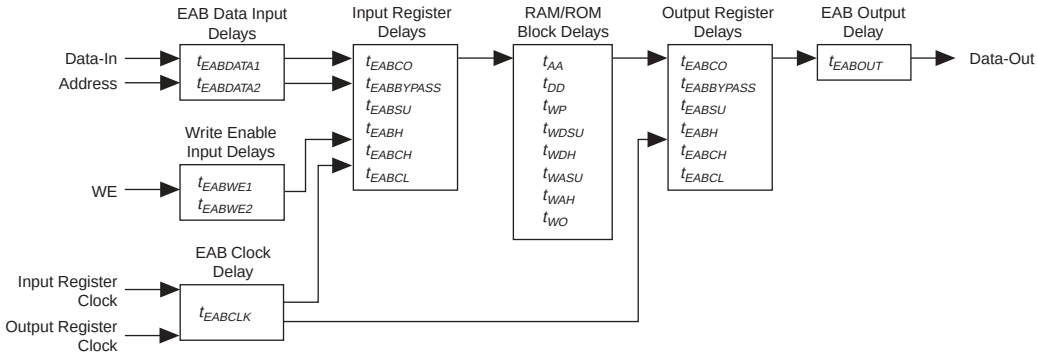


Figure 27. FLEX 10K Device EAB Timing Model



Figures 28 shows the timing model for bidirectional I/O pin timing.

Table 45. EPF10K10 & EPF10K20 Device External Timing Parameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{DRR}		16.1		20.0	ns
t_{INSU} *(2)*, *(3)*	5.5		6.0		ns
t_{INH} *(3)*	0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	6.7	2.0	8.4	ns

Table 46. EPF10K10 Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{INSUBIDIR}$	4.5		5.6		ns
$t_{INHBIDIR}$	0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	6.7	2.0	8.4	ns
$t_{XZBIDIR}$		10.5		13.4	ns
$t_{ZXBIDIR}$		10.5		13.4	ns

Table 47. EPF10K20 Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{INSUBIDIR}$	4.6		5.7		ns
$t_{INHBIDIR}$	0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	6.7	2.0	8.4	ns
$t_{XZBIDIR}$		10.5		13.4	ns
$t_{ZXBIDIR}$		10.5		13.4	ns

Notes to tables:

(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Table 49. EPF10K30, EPF10K40 & EPF10K50 Device IOE Timing Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{IOD}		0.4		0.6	ns
t_{IOC}		0.5		0.9	ns
t_{IOCO}		0.4		0.5	ns
t_{IOCOMB}		0.0		0.0	ns
t_{IOSU}	3.1		3.5		ns
t_{IOH}	1.0		1.9		ns
t_{IOCLR}		1.0		1.2	ns
t_{OD1}		3.3		3.6	ns
t_{OD2}		5.6		6.5	ns
t_{OD3}		7.0		8.3	ns
t_{XZ}		5.2		5.5	ns
t_{ZX1}		5.2		5.5	ns
t_{ZX2}		7.5		8.4	ns
t_{ZX3}		8.9		10.2	ns
t_{INREG}		7.7		10.0	ns
t_{IOFD}		3.3		4.0	ns
t_{INCOMB}		3.3		4.0	ns

Table 50. EPF10K30, EPF10K40 & EPF10K50 Device EAB Internal Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{EABDATA1}$		1.5		1.9	ns
$t_{EABDATA2}$		4.8		6.0	ns
t_{EABWE1}		1.0		1.2	ns
t_{EABWE2}		5.0		6.2	ns
t_{EABCLK}		1.0		2.2	ns
t_{EABCO}		0.5		0.6	ns
$t_{EABBYPASS}$		1.5		1.9	ns
t_{EABSU}	1.5		1.8		ns
t_{EABH}	2.0		2.5		ns
t_{AA}		8.7		10.7	ns
t_{WP}	5.8		7.2		ns
t_{WDSU}	1.6		2.0		ns
t_{WDH}	0.3		0.4		ns
t_{WASU}	0.5		0.6		ns
t_{WAH}	1.0		1.2		ns
t_{WO}		5.0		6.2	ns
t_{DD}		5.0		6.2	ns
t_{EABOUT}		0.5		0.6	ns
t_{EABCH}	4.0		4.0		ns
t_{EABCL}	5.8		7.2		ns

Table 59. EPF10K70 Device EAB Internal Microparameters *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.3		1.5		1.9	ns
$t_{EABDATA2}$		4.3		4.8		6.0	ns
t_{EABWE1}		0.9		1.0		1.2	ns
t_{EABWE2}		4.5		5.0		6.2	ns
t_{EABCLK}		0.9		1.0		2.2	ns
t_{EABCO}		0.4		0.5		0.6	ns
$t_{EABBYPASS}$		1.3		1.5		1.9	ns
t_{EABSU}	1.3		1.5		1.8		ns
t_{EABH}	1.8		2.0		2.5		ns
t_{AA}		7.8		8.7		10.7	ns
t_{WP}	5.2		5.8		7.2		ns
t_{WDSU}	1.4		1.6		2.0		ns
t_{WDH}	0.3		0.3		0.4		ns
t_{WASU}	0.4		0.5		0.6		ns
t_{WAH}	0.9		1.0		1.2		ns
t_{WO}		4.5		5.0		6.2	ns
t_{DD}		4.5		5.0		6.2	ns
t_{EABOUT}		0.4		0.5		0.6	ns
t_{EABCH}	4.0		4.0		4.0		ns
t_{EABCL}	5.2		5.8		7.2		ns

Table 60. EPF10K70 Device EAB Internal Timing Macroparameters *Note (1)*							
Symbol	**-2 Speed Grade**		**-3 Speed Grade**		**-4 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		12.1		13.7		17.0	ns
$t_{EABRCCOMB}$	12.1		13.7		17.0		ns
$t_{EABRCREG}$	8.6		9.7		11.9		ns
t_{EABWP}	5.2		5.8		7.2		ns
$t_{EABWCCOMB}$	6.5		7.3		9.0		ns
$t_{EABWCREG}$	11.6		13.0		16.0		ns
t_{EABDD}		8.8		10.0		12.5	ns
$t_{EABDATACO}$		1.7		2.0		3.4	ns
$t_{EABDATASU}$	4.7		5.3		5.6		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	4.9		5.5		5.8		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.8		2.1		2.7		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	4.1		4.7		5.8		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		8.4		9.5		11.8	ns

Table 66. EPF10K100 Device EAB Internal Microparameters *Note (1)*

Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.5		1.5		1.9	ns
$t_{EABDATA2}$		4.8		4.8		6.0	ns
t_{EABWE1}		1.0		1.0		1.2	ns
t_{EABWE2}		5.0		5.0		6.2	ns
t_{EABCLK}		1.0		1.0		2.2	ns
t_{EABCO}		0.5		0.5		0.6	ns
$t_{EABBYPASS}$		1.5		1.5		1.9	ns
t_{EABSU}	1.5		1.5		1.8		ns
t_{EABH}	2.0		2.0		2.5		ns
t_{AA}		8.7		8.7		10.7	ns
t_{WP}	5.8		5.8		7.2		ns
t_{WDSU}	1.6		1.6		2.0		ns
t_{WDH}	0.3		0.3		0.4		ns
t_{WASU}	0.5		0.5		0.6		ns
t_{WAH}	1.0		1.0		1.2		ns
t_{WO}		5.0		5.0		6.2	ns
t_{DD}		5.0		5.0		6.2	ns
t_{EABOUT}		0.5		0.5		0.6	ns
t_{EABCH}	4.0		4.0		4.0		ns
t_{EABCL}	5.8		5.8		7.2		ns

Table 80. EPF10K130V Device EAB Internal Microparameters *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.9		2.4		2.4	ns
$t_{EABDATA2}$		3.7		4.7		4.7	ns
t_{EABWE1}		1.9		2.4		2.4	ns
t_{EABWE2}		3.7		4.7		4.7	ns
t_{EABCLK}		0.7		0.9		0.9	ns
t_{EABCO}		0.5		0.6		0.6	ns
$t_{EABBYPASS}$		0.6		0.8		0.8	ns
t_{EABSU}	1.4		1.8		1.8		ns
t_{EABH}	0.0		0.0		0.0		ns
t_{AA}		5.6		7.1		7.1	ns
t_{WP}	3.7		4.7		4.7		ns
t_{WDSU}	4.6		5.9		5.9		ns
t_{WDH}	0.0		0.0		0.0		ns
t_{WASU}	3.9		5.0		5.0		ns
t_{WAH}	0.0		0.0		0.0		ns
t_{WO}		5.6		7.1		7.1	ns
t_{DD}		5.6		7.1		7.1	ns
t_{EABOUT}		2.4		3.1		3.1	ns
t_{EABCH}	4.0		4.0		4.0		ns
t_{EABCL}	4.0		4.7		4.7		ns

Table 81. EPF10K130V Device EAB Internal Timing Macroparameters *Note (1)*							
Symbol	**-2 Speed Grade**		**-3 Speed Grade**		**-4 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		11.2		14.2		14.2	ns
$t_{EABRCCOMB}$	11.1		14.2		14.2		ns
$t_{EABRCREG}$	8.5		10.8		10.8		ns
t_{EABWP}	3.7		4.7		4.7		ns
$t_{EABWCCOMB}$	7.6		9.7		9.7		ns
$t_{EABWCREG}$	14.0		17.8		17.8		ns
t_{EABDD}		11.1		14.2		14.2	ns
$t_{EABDATACO}$		3.6		4.6		4.6	ns
$t_{EABDATASU}$	4.4		5.6		5.6		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	4.4		5.6		5.6		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	4.6		5.9		5.9		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.9		5.0		5.0		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		11.1		14.2		14.2	ns

Table 100. EPF10K100A Device IOE Timing Microparameters *Note (1)*							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		2.5		2.9		3.4	ns
t_{IOC}		0.3		0.3		0.4	ns
t_{IOCO}		0.2		0.2		0.3	ns
t_{IOCOMB}		0.5		0.6		0.7	ns
t_{IOSU}	1.3		1.7		1.8		ns
t_{IOH}	0.2		0.2		0.3		ns
t_{IOCLR}		1.0		1.2		1.4	ns
t_{OD1}		2.2		2.6		3.0	ns
t_{OD2}		4.5		5.3		6.1	ns
t_{OD3}		6.8		7.9		9.3	ns
t_{XZ}		2.7		3.1		3.7	ns
t_{ZX1}		2.7		3.1		3.7	ns
t_{ZX2}		5.0		5.8		6.8	ns
t_{ZX3}		7.3		8.4		10.0	ns
t_{INREG}		5.3		6.1		7.2	ns
t_{IOFD}		4.7		5.5		6.4	ns
t_{INCOMB}		4.7		5.5		6.4	ns

Notes to tables:
(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Tables 106 through 112 show EPF10K250A device internal and external timing parameters.

Table 106. EPF10K250A Device LE Timing Microparameters *Note (1)*

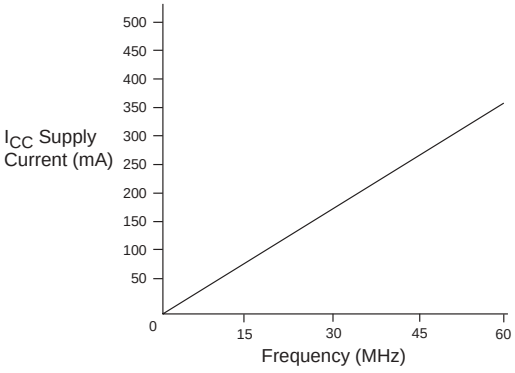
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.9		1.0		1.4	ns
t_{CLUT}		1.2		1.3		1.6	ns
t_{RLUT}		2.0		2.3		2.7	ns
t_{PACKED}		0.4		0.4		0.5	ns
t_{EN}		1.4		1.6		1.9	ns
t_{CICO}		0.2		0.3		0.3	ns
t_{CGEN}		0.4		0.6		0.6	ns
t_{CGENR}		0.8		1.0		1.1	ns
t_{CASC}		0.7		0.8		1.0	ns
t_{C}		1.2		1.3		1.6	ns
t_{CO}		0.6		0.7		0.9	ns
t_{COMB}		0.5		0.6		0.7	ns
t_{SU}	1.2		1.4		1.7		ns
t_{H}	1.2		1.3		1.6		ns
t_{PRE}		0.7		0.8		0.9	ns
t_{CLR}		0.7		0.8		0.9	ns
t_{CH}	2.5		3.0		3.5		ns
t_{CL}	2.5		3.0		3.5		ns

Table 107. EPF10K250A Device IOE Timing Microparameters *Note (1)*

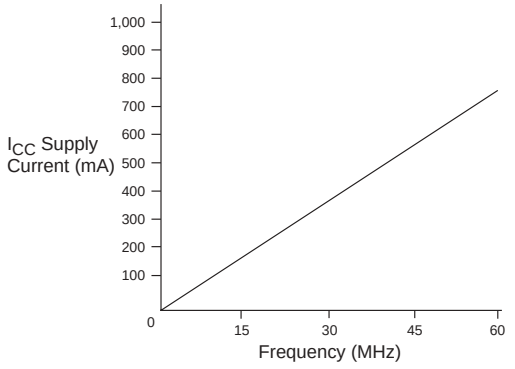
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{IOD}		1.2		1.3		1.6	ns
t_{IOC}		0.4		0.4		0.5	ns
t_{IOCO}		0.8		0.9		1.1	ns
t_{IOCOMB}		0.7		0.7		0.8	ns
t_{IOSU}	2.7		3.1		3.6		ns
t_{IOH}	0.2		0.3		0.3		ns
t_{IOCLR}		1.2		1.3		1.6	ns
t_{OD1}		3.2		3.6		4.2	ns
t_{OD2}		5.9		6.7		7.8	ns
t_{OD3}		8.7		9.8		11.5	ns
t_{XZ}		3.8		4.3		5.0	ns
t_{ZX1}		3.8		4.3		5.0	ns
t_{ZX2}		6.5		7.4		8.6	ns
t_{ZX3}		9.3		10.5		12.3	ns
t_{INREG}		8.2		9.3		10.9	ns
t_{IOFD}		9.0		10.2		12.0	ns
t_{INCOMB}		9.0		10.2		12.0	ns

Figure 32. $I_{CCACTIVE}$ vs. Operating Frequency (Part 1 of 3)

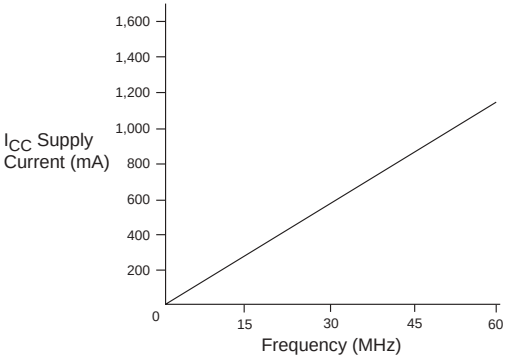
EPF10K10



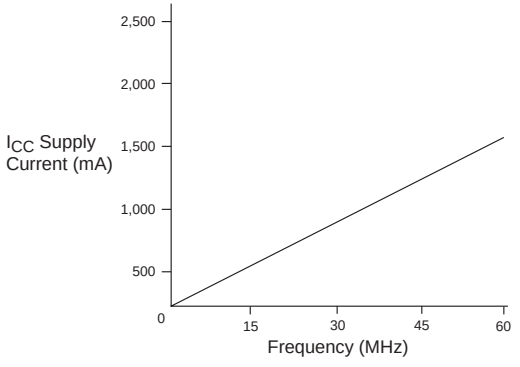
EPF10K20



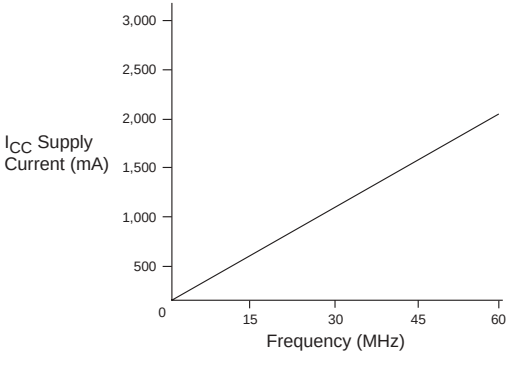
EPF10K30



EPF10K40



EPF10K50



EPF10K70

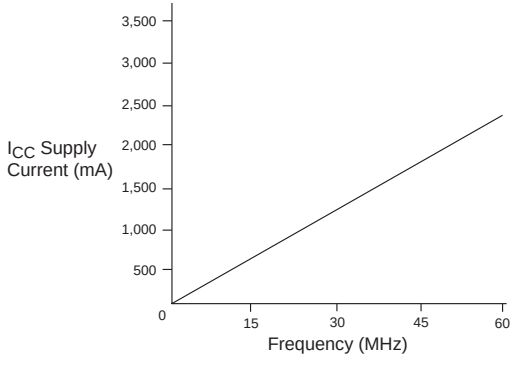
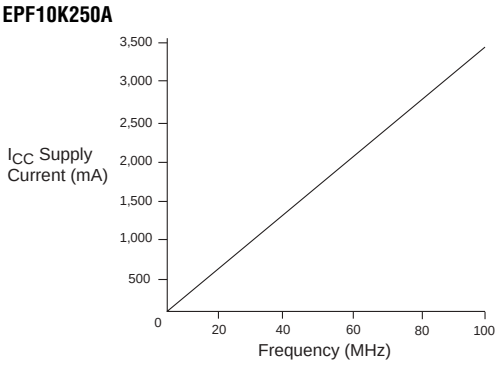


Figure 32. $I_{CCACTIVE}$ vs. Operating Frequency (Part 3 of 3)



Configuration & Operation

The FLEX 10K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

See *Application Note 116 (Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices)* for detailed descriptions of device configuration options, device configuration pins, and for information on configuring FLEX 10K devices, including sample schematics, timing diagrams, and configuration parameters.

Operating Modes

The FLEX 10K architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. The process of physically loading the SRAM data into the device is called *configuration*. Before configuration, as VCC rises, the device initiates a Power-On Reset (POR). This POR event clears the device and prepares it for configuration. The FLEX 10K POR time does not exceed 50 µs.

During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.