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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 216 |
| Number of Logic Elements/Cells | 1728 |
| Total RAM Bits | 12288 |
| Number of I/O | 189 |
| Number of Gates | 69000 |
| Voltage - Supply | 3V ~ 3.6V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 240-BFQFP |
| Supplier Device Package | 240-PQFP (32x32) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epf10k30aqi240-3 |

For more information, see the following documents:

- *Configuration Devices for APEX & FLEX Devices Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Application Note 116 (Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices)*

FLEX 10K devices are supported by Altera development systems; single, integrated packages that offer schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The Altera software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Altera software works easily with common gate array EDA tools for synthesis and simulation. For example, the Altera software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Altera software contains EDA libraries that use device-specific features such as carry chains which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Altera development systems include DesignWare functions that are optimized for the FLEX 10K architecture.

The Altera development systems run on Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations.

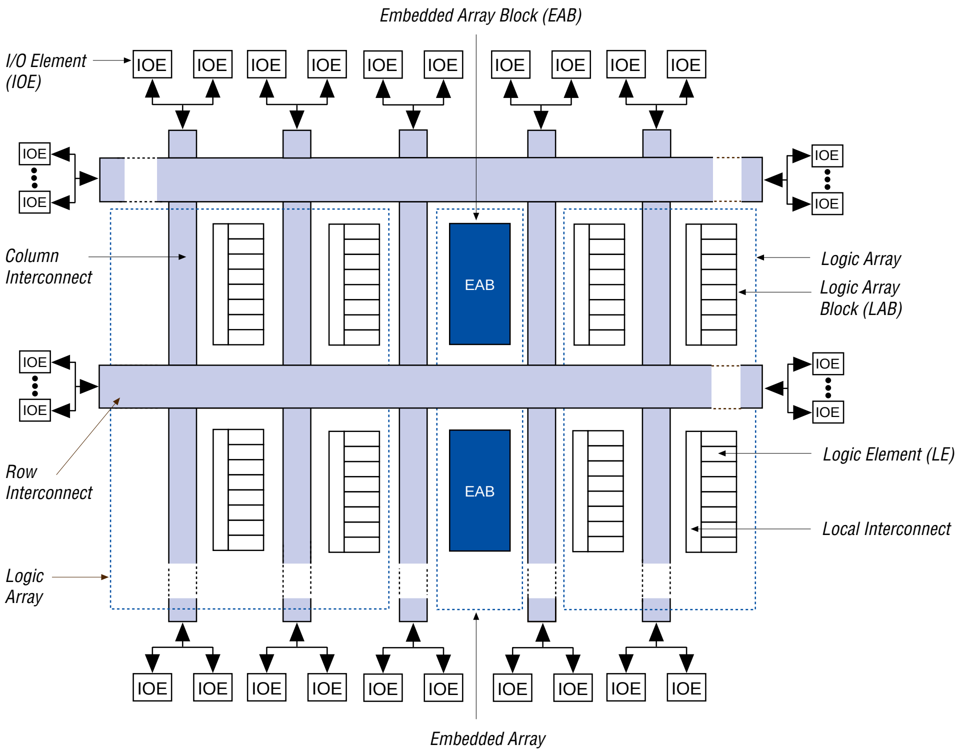
See the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* for more information.

## Functional Description

Each FLEX 10K device contains an embedded array to implement memory and specialized logic functions, and a logic array to implement general logic.

The embedded array consists of a series of EABs. When implementing memory functions, each EAB provides 2,048 bits, which can be used to create RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. When implementing logic, each EAB can contribute 100 to 600 gates towards complex logic functions, such as multipliers, microcontrollers, state machines, and DSP functions. EABs can be used independently, or multiple EABs can be combined to implement larger functions.

*Figure 1. FLEX 10K Device Block Diagram*



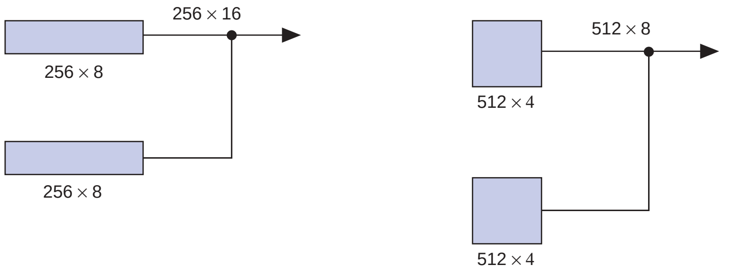

FLEX 10K devices provide six dedicated inputs that drive the flipflops' control inputs to ensure the efficient distribution of high-speed, low-skew (less than 1.5 ns) control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

## Embedded Array Block

The EAB is a flexible block of RAM with registers on the input and output ports, and is used to implement common gate array megafunctions. The EAB is also suitable for functions such as multipliers, vector scalars, and error correction circuits, because it is large and flexible. These functions can be combined in applications such as digital filters and microcontrollers.

Larger blocks of RAM are created by combining multiple EABs. For example, two 256 × 8 RAM blocks can be combined to form a 256 × 16 RAM block; two 512 × 4 blocks of RAM can be combined to form a 512 × 8 RAM block. See Figure 3.

*Figure 3. Examples of Combining EABs*




If necessary, all EABs in a device can be cascaded to form a single RAM block. EABs can be cascaded to form RAM blocks of up to 2,048 words without impacting timing. Altera's software automatically combines EABs to meet a designer's RAM specifications.

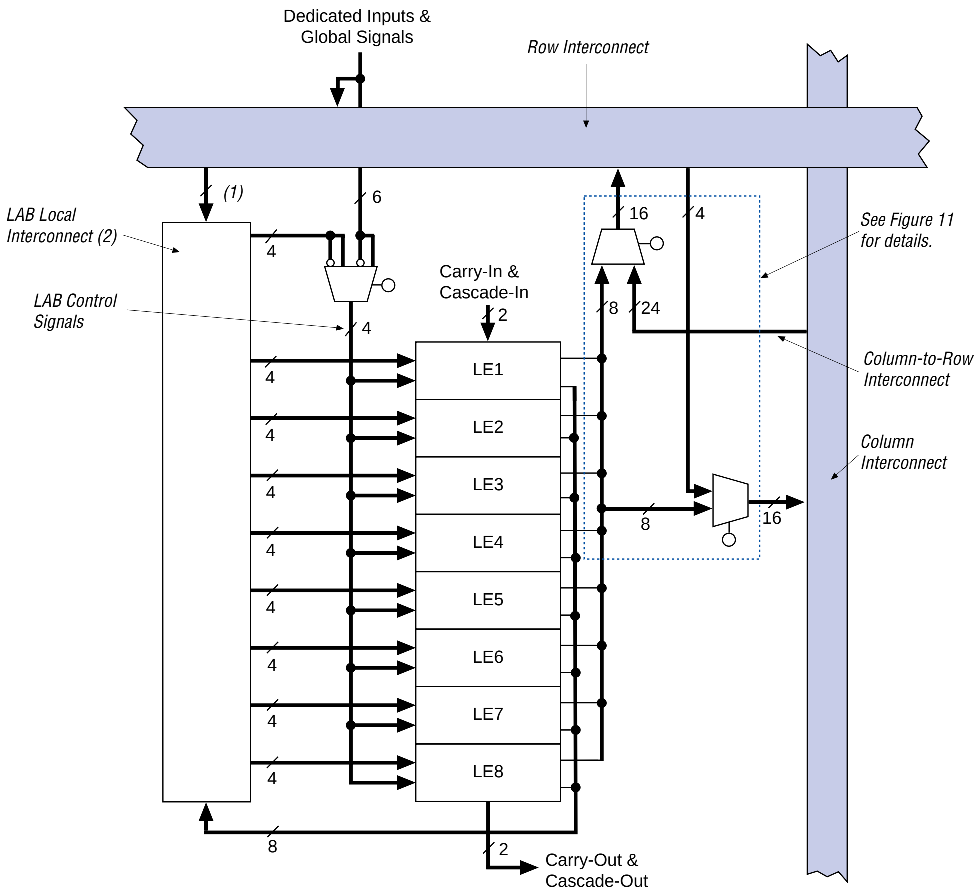
EABs provide flexible options for driving and controlling clock signals. Different clocks can be used for the EAB inputs and outputs. Registers can be independently inserted on the data input, EAB output, or the address and `WE` inputs. The global signals and the EAB local interconnect can drive the `WE` signal. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control the `WE` signal or the EAB clock signals.

Each EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs. See Figure 4.

## Logic Array Block

Each LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the FLEX 10K architecture, facilitating efficient routing with optimum device utilization and high performance. See Figure 5.

***Figure 5. FLEX 10K LAB***



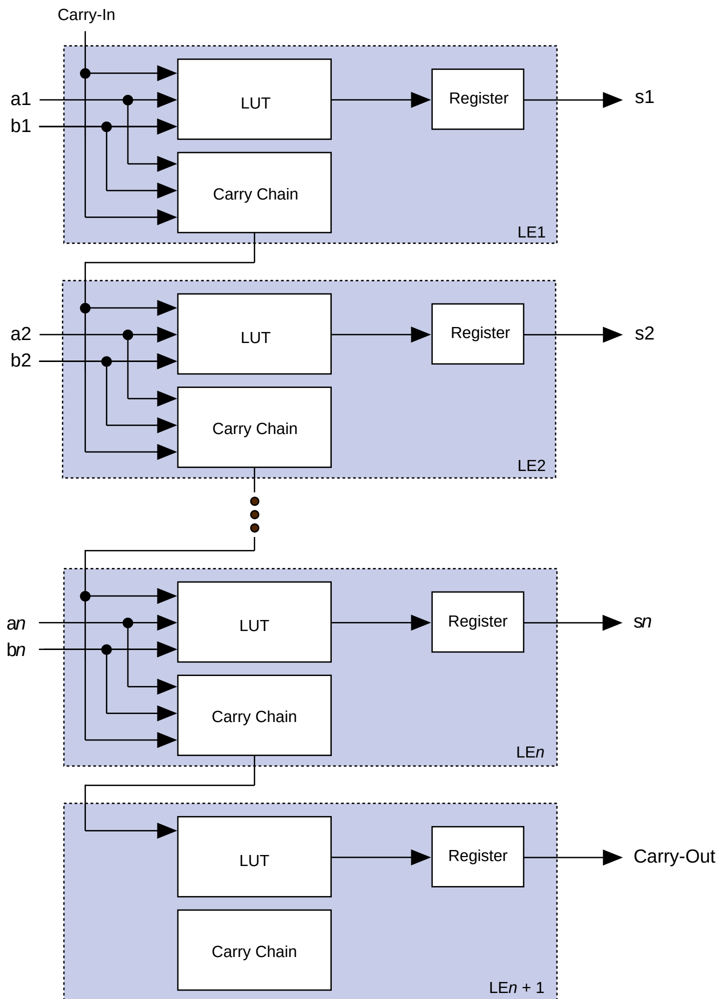

*Notes:*

(1) EPF10K10, EPF10K10A, EPF10K20, EPF10K30, EPF10K30A, EPF10K40, EPF10K50, and EPF10K50V devices have 22 inputs to the LAB local interconnect channel from the row; EPF10K70, EPF10K100, EPF10K100A, EPF10K130V, and EPF10K250A devices have 26.

(2) EPF10K10, EPF10K10A, EPF10K20, EPF10K30, EPF10K30A, EPF10K40, EPF10K50, and EPF10K50V devices have 30 LAB local interconnect channels; EPF10K70, EPF10K100, EPF10K100A, EPF10K130V, and EPF10K250A devices have 34 LABs.

Figure 7 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can either be bypassed for simple adders or be used for an accumulator function. The carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal.

***Figure 7. Carry Chain Operation (n-bit Full Adder)***



#### Asynchronous Preset

An asynchronous preset is implemented as either an asynchronous load, or with an asynchronous clear. If DATA3 is tied to $V_{CC}$, asserting LABCTRL1 asynchronously loads a one into the register. Alternatively, the Altera software can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

#### Asynchronous Preset & Clear

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. DATA3 is tied to $V_{CC}$, therefore, asserting LABCTRL1 asynchronously loads a one into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

#### Asynchronous Load with Clear

When implementing an asynchronous load in conjunction with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear; LABCTRL2 does not have to feed the preset circuits.

#### Asynchronous Load with Preset

When implementing an asynchronous load in conjunction with preset, the Altera software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 presets the register, while asserting LABCTRL1 loads the register. The Altera software inverts the signal that drives DATA3 to account for the inversion of the register's output.

#### Asynchronous Load without Preset or Clear

When implementing an asynchronous load without preset or clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

*Table 8. EPF10K10, EPF10K20, EPF10K30, EPF10K40 & EPF10K50 Peripheral Bus Sources*

| Peripheral Control Signal | EPF10K10 EPF10K10A | EPF10K20 | EPF10K30 EPF10K30A | EPF10K40 | EPF10K50 EPF10K50V |
|---|---|---|---|---|---|
| OE0 | Row A | Row A | Row A | Row A | Row A |
| OE1 | Row A | Row B | Row B | Row C | Row B |
| OE2 | Row B | Row C | Row C | Row D | Row D |
| OE3 | Row B | Row D | Row D | Row E | Row F |
| OE4 | Row C | Row E | Row E | Row F | Row H |
| OE5 | Row C | Row F | Row F | Row G | Row J |
| CLKENA0/CLK0/GLOBAL0 | Row A | Row A | Row A | Row B | Row A |
| CLKENA1/OE6/GLOBAL1 | Row A | Row B | Row B | Row C | Row C |
| CLKENA2/CLR0 | Row B | Row C | Row C | Row D | Row E |
| CLKENA3/OE7/GLOBAL2 | Row B | Row D | Row D | Row E | Row G |
| CLKENA4/CLR1 | Row C | Row E | Row E | Row F | Row I |
| CLKENA5/CLK1/GLOBAL3 | Row C | Row F | Row F | Row H | Row J |

*Table 9. EPF10K70, EPF10K100, EPF10K130V & EPF10K250A Peripheral Bus Sources*

| Peripheral Control Signal | EPF10K70 | EPF10K100 EPF10K100A | EPF10K130V | EPF10K250A |
|---|---|---|---|---|
| OE0 | Row A | Row A | Row C | Row E |
| OE1 | Row B | Row C | Row E | Row G |
| OE2 | Row D | Row E | Row G | Row I |
| OE3 | Row I | Row L | Row N | Row P |
| OE4 | Row G | Row I | Row K | Row M |
| OE5 | Row H | Row K | Row M | Row O |
| CLKENA0/CLK0/GLOBAL0 | Row E | Row F | Row H | Row J |
| CLKENA1/OE6/GLOBAL1 | Row C | Row D | Row F | Row H |
| CLKENA2/CLR0 | Row B | Row B | Row D | Row F |
| CLKENA3/OE7/GLOBAL2 | Row F | Row H | Row J | Row L |
| CLKENA4/CLR1 | Row H | Row J | Row L | Row N |
| CLKENA5/CLK1/GLOBAL3 | Row E | Row G | Row I | Row K |

*Table 28. FLEX 10KA 3.3-V Device DC Operating Conditions* *Notes (6), (7)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 1.7 or $0.5 \times V_{CCINT}$, whichever is lower | | 5.75 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | $0.3 \times V_{CCINT}$ | V |
| $V_{OH}$ | 3.3-V high-level TTL output voltage | $I_{OH}$ = –11 mA DC, $V_{CCIO}$ = 3.00 V *(8)* | 2.4 | | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(8)* | $V_{CCIO} - 0.2$ | | | V |
| | 3.3-V high-level PCI output voltage | $I_{OH}$ = –0.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(8)* | $0.9 \times V_{CCIO}$ | | | V |
| | 2.5-V high-level output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 2.30 V *(8)* | 2.1 | | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(8)* | 2.0 | | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(8)* | 1.7 | | | V |
| $V_{OL}$ | 3.3-V low-level TTL output voltage | $I_{OL}$ = 9 mA DC, $V_{CCIO}$ = 3.00 V *(9)* | | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(9)* | | | 0.2 | V |
| | 3.3-V low-level PCI output voltage | $I_{OL}$ = 1.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(9)* | | | $0.1 \times V_{CCIO}$ | V |
| | 2.5-V low-level output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 2.30 V *(9)* | | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V *(9)* | | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 2.30 V *(9)* | | | 0.7 | V |
| $I_I$ | Input pin leakage current | $V_I$ = 5.3 V to –0.3 V *(10)* | –10 | | 10 | μA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O$ = 5.3 V to –0.3 V *(10)* | –10 | | 10 | μA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) | $V_I$ = ground, no load | | 0.3 | 10 | mA |
| | | $V_I$ = ground, no load *(11)* | | 10 | | mA |

**Table 29. 3.3-V Device Capacitance of EPF10K10A & EPF10K30A Devices** *Note (12)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 12 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |

**Table 30. 3.3-V Device Capacitance of EPF10K100A Devices** *Note (12)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 10 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 15 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 10 | pF |

**Table 31. 3.3-V Device Capacitance of EPF10K250A Devices** *Note (12)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 10 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 15 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 10 | pF |

***Notes to tables:***

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC voltage input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum $V_{CC}$ rise time is 100 ms, and $V_{CC}$ must rise monotonically.
(5) FLEX 10KA device inputs may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.
(6) Typical values are for $T_A$ = 25° C and $V_{CC}$ = 3.3 V.
(7) These values are specified under the Recommended Operating Conditions shown in Table 27 on page 51.
(8) The $I_{OH}$ parameter refers to high-level TTL, PCI, or CMOS output current.
(9) The $I_{OL}$ parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(10) This value is specified for normal device operation. The value may vary during power-up.
(11) This parameter applies to all -1 speed grade commercial temperature devices and all -2 speed grade industrial-temperature devices.
(12) Capacitance is sample-tested only.

| *Table 42. EPF10K10 & EPF10K20 Device EAB Internal Timing Macroparameters* *Note (1)* | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **-3 Speed Grade** | | **-4 Speed Grade** | | **Unit** |
| | **Min** | **Max** | **Min** | **Max** | |
| $t_{EABAA}$ | | 13.7 | | 17.0 | ns |
| $t_{EABRCCOMB}$ | 13.7 | | 17.0 | | ns |
| $t_{EABRCREG}$ | 9.7 | | 11.9 | | ns |
| $t_{EABWP}$ | 5.8 | | 7.2 | | ns |
| $t_{EABWCCOMB}$ | 7.3 | | 9.0 | | ns |
| $t_{EABWCREG}$ | 13.0 | | 16.0 | | ns |
| $t_{EABDD}$ | | 10.0 | | 12.5 | ns |
| $t_{EABDATACO}$ | | 2.0 | | 3.4 | ns |
| $t_{EABDATASU}$ | 5.3 | | 5.6 | | ns |
| $t_{EABDATAH}$ | 0.0 | | 0.0 | | ns |
| $t_{EABWESU}$ | 5.5 | | 5.8 | | ns |
| $t_{EABWEH}$ | 0.0 | | 0.0 | | ns |
| $t_{EABWDSU}$ | 5.5 | | 5.8 | | ns |
| $t_{EABWDH}$ | 0.0 | | 0.0 | | ns |
| $t_{EABWASU}$ | 2.1 | | 2.7 | | ns |
| $t_{EABWAH}$ | 0.0 | | 0.0 | | ns |
| $t_{EABWO}$ | | 9.5 | | 11.8 | ns |

**Table 49. EPF10K30, EPF10K40 & EPF10K50 Device IOE Timing Microparameters** *Note (1)*

| Symbol | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| $t_{IOD}$ | | 0.4 | | 0.6 | ns |
| $t_{IOC}$ | | 0.5 | | 0.9 | ns |
| $t_{IOCO}$ | | 0.4 | | 0.5 | ns |
| $t_{IOCOMB}$ | | 0.0 | | 0.0 | ns |
| $t_{IOSU}$ | 3.1 | | 3.5 | | ns |
| $t_{IOH}$ | 1.0 | | 1.9 | | ns |
| $t_{IOCLR}$ | | 1.0 | | 1.2 | ns |
| $t_{OD1}$ | | 3.3 | | 3.6 | ns |
| $t_{OD2}$ | | 5.6 | | 6.5 | ns |
| $t_{OD3}$ | | 7.0 | | 8.3 | ns |
| $t_{XZ}$ | | 5.2 | | 5.5 | ns |
| $t_{ZX1}$ | | 5.2 | | 5.5 | ns |
| $t_{ZX2}$ | | 7.5 | | 8.4 | ns |
| $t_{ZX3}$ | | 8.9 | | 10.2 | ns |
| $t_{INREG}$ | | 7.7 | | 10.0 | ns |
| $t_{IOFD}$ | | 3.3 | | 4.0 | ns |
| $t_{INCOMB}$ | | 3.3 | | 4.0 | ns |

| *Table 51. EPF10K30, EPF10K40 & EPF10K50 Device EAB Internal Timing Macroparameters Note (1)* | | | | | |
|---|---|---|---|---|---|
| Symbol | -3 Speed Grade | | -4 Speed Grade | | Unit |
| | Min | Max | Min | Max | |
| $t_{EABAA}$ | | 13.7 | | 17.0 | ns |
| $t_{EABRCCOMB}$ | 13.7 | | 17.0 | | ns |
| $t_{EABRCREG}$ | 9.7 | | 11.9 | | ns |
| $t_{EABWP}$ | 5.8 | | 7.2 | | ns |
| $t_{EABWCCOMB}$ | 7.3 | | 9.0 | | ns |
| $t_{EABWCREG}$ | 13.0 | | 16.0 | | ns |
| $t_{EABDD}$ | | 10.0 | | 12.5 | ns |
| $t_{EABDATACO}$ | | 2.0 | | 3.4 | ns |
| $t_{EABDATASU}$ | 5.3 | | 5.6 | | ns |
| $t_{EABDATAH}$ | 0.0 | | 0.0 | | ns |
| $t_{EABWESU}$ | 5.5 | | 5.8 | | ns |
| $t_{EABWEH}$ | 0.0 | | 0.0 | | ns |
| $t_{EABWDSU}$ | 5.5 | | 5.8 | | ns |
| $t_{EABWDH}$ | 0.0 | | 0.0 | | ns |
| $t_{EABWASU}$ | 2.1 | | 2.7 | | ns |
| $t_{EABWAH}$ | 0.0 | | 0.0 | | ns |
| $t_{EABWO}$ | | 9.5 | | 11.8 | ns |

*Table 52. EPF10K30 Device Interconnect Timing Microparameters* *Note (1)*

| Symbol | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 6.9 | | 8.7 | ns |
| $t_{DIN2LE}$ | | 3.6 | | 4.8 | ns |
| $t_{DIN2DATA}$ | | 5.5 | | 7.2 | ns |
| $t_{DCLK2IOE}$ | | 4.6 | | 6.2 | ns |
| $t_{DCLK2LE}$ | | 3.6 | | 4.8 | ns |
| $t_{SAMELAB}$ | | 0.3 | | 0.3 | ns |
| $t_{SAMEROW}$ | | 3.3 | | 3.7 | ns |
| $t_{SAMECOLUMN}$ | | 2.5 | | 2.7 | ns |
| $t_{DIFFROW}$ | | 5.8 | | 6.4 | ns |
| $t_{TWOROWS}$ | | 9.1 | | 10.1 | ns |
| $t_{LEPERIPH}$ | | 6.2 | | 7.1 | ns |
| $t_{LABCARRY}$ | | 0.4 | | 0.6 | ns |
| $t_{LABCASC}$ | | 2.4 | | 3.0 | ns |

*Table 53. EPF10K40 Device Interconnect Timing Microparameters* *Note (1)*

| Symbol | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 7.6 | | 9.4 | ns |
| $t_{DIN2LE}$ | | 3.6 | | 4.8 | ns |
| $t_{DIN2DATA}$ | | 5.5 | | 7.2 | ns |
| $t_{DCLK2IOE}$ | | 4.6 | | 6.2 | ns |
| $t_{DCLK2LE}$ | | 3.6 | | 4.8 | ns |
| $t_{SAMELAB}$ | | 0.3 | | 0.3 | ns |
| $t_{SAMEROW}$ | | 3.3 | | 3.7 | ns |
| $t_{SAMECOLUMN}$ | | 3.1 | | 3.2 | ns |
| $t_{DIFFROW}$ | | 6.4 | | 6.4 | ns |
| $t_{TWOROWS}$ | | 9.7 | | 10.6 | ns |
| $t_{LEPERIPH}$ | | 6.4 | | 7.1 | ns |
| $t_{LABCARRY}$ | | 0.4 | | 0.6 | ns |
| $t_{LABCASC}$ | | 2.4 | | 3.0 | ns |

*Notes to tables:*
(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Tables 57 through 63 show EPF10K70 device internal and external timing parameters.

**Table 57. EPF10K70 Device LE Timing Microparameters** *Note (1)*

| Symbol | -2 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 1.3 | | 1.5 | | 2.0 | ns |
| $t_{CLUT}$ | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{RLUT}$ | | 1.5 | | 1.6 | | 2.0 | ns |
| $t_{PACKED}$ | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{EN}$ | | 0.8 | | 0.9 | | 1.2 | ns |
| $t_{CICO}$ | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{CGEN}$ | | 1.0 | | 1.1 | | 1.4 | ns |
| $t_{CGENR}$ | | 1.1 | | 1.2 | | 1.5 | ns |
| $t_{CASC}$ | | 1.0 | | 1.1 | | 1.3 | ns |
| $t_C$ | | 0.7 | | 0.8 | | 1.0 | ns |
| $t_{CO}$ | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{SU}$ | 1.9 | | 2.1 | | 2.6 | | ns |
| $t_H$ | 2.1 | | 2.3 | | 3.1 | | ns |
| $t_{PRE}$ | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{CLR}$ | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{CH}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | 4.0 | | 4.0 | | 4.0 | | ns |

*Table 69. EPF10K100 Device External Timing Parameters* *Note (1)*

| Symbol | -3DX Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 19.1 | | 19.1 | | 24.2 | ns |
| $t_{INSU}$ *(2)*, *(3)*, *(4)* | 7.8 | | 7.8 | | 8.5 | | ns |
| $t_{OUTCO}$ *(3)*, *(4)* | 2.0 | 11.1 | 2.0 | 11.1 | 2.0 | 14.3 | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ *(2)*, *(3)*, *(5)* | 6.2 | | – | | – | | ns |
| $t_{OUTCO}$ *(3)*, *(5)* | 2.0 | 6.7 | | – | | – | ns |

*Table 70. EPF10K100 Device External Bidirectional Timing Parameters* *Note (1)*

| Symbol | -3DX Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ *(4)* | 8.1 | | 8.1 | | 10.4 | | ns |
| $t_{INHBIDIR}$ *(4)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ *(4)* | 2.0 | 11.1 | 2.0 | 11.1 | 2.0 | 14.3 | ns |
| $t_{XZBIDIR}$ *(4)* | | 15.3 | | 15.3 | | 18.4 | ns |
| $t_{ZXBIDIR}$ *(4)* | | 15.3 | | 15.3 | | 18.4 | ns |
| $t_{INSUBIDIR}$ *(5)* | 9.1 | | – | | – | | ns |
| $t_{INHBIDIR}$ *(5)* | 0.0 | | – | | – | | ns |
| $t_{OUTCOBIDIR}$ *(5)* | 2.0 | 7.2 | – | – | – | – | ns |
| $t_{XZBIDIR}$ *(5)* | | 14.3 | | – | | – | ns |
| $t_{ZXBIDIR}$ *(5)* | | 14.3 | | – | | – | ns |

*Notes to tables:*

(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.
(4) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(5) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

*Table 73. EPF10K50V Device EAB Internal Microparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.7 | | 2.8 | | 3.4 | | 4.6 | ns |
| $t_{EABDATA2}$ | | 4.9 | | 3.9 | | 4.8 | | 5.9 | ns |
| $t_{EABWE1}$ | | 0.0 | | 2.5 | | 3.0 | | 3.7 | ns |
| $t_{EABWE2}$ | | 4.0 | | 4.1 | | 5.0 | | 6.2 | ns |
| $t_{EABCLK}$ | | 0.4 | | 0.8 | | 1.0 | | 1.2 | ns |
| $t_{EABCO}$ | | 0.1 | | 0.2 | | 0.3 | | 0.4 | ns |
| $t_{EABBYPASS}$ | | 0.9 | | 1.1 | | 1.3 | | 1.6 | ns |
| $t_{EABSU}$ | 0.8 | | 1.5 | | 1.8 | | 2.2 | | ns |
| $t_{EABH}$ | 0.8 | | 1.6 | | 2.0 | | 2.5 | | ns |
| $t_{AA}$ | | 5.5 | | 8.2 | | 10.0 | | 12.4 | ns |
| $t_{WP}$ | 6.0 | | 4.9 | | 6.0 | | 7.4 | | ns |
| $t_{WDSU}$ | 0.1 | | 0.8 | | 1.0 | | 1.2 | | ns |
| $t_{WDH}$ | 0.1 | | 0.2 | | 0.3 | | 0.4 | | ns |
| $t_{WASU}$ | 0.1 | | 0.4 | | 0.5 | | 0.6 | | ns |
| $t_{WAH}$ | 0.1 | | 0.8 | | 1.0 | | 1.2 | | ns |
| $t_{WO}$ | | 2.8 | | 4.3 | | 5.3 | | 6.5 | ns |
| $t_{DD}$ | | 2.8 | | 4.3 | | 5.3 | | 6.5 | ns |
| $t_{EABOUT}$ | | 0.5 | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{EABCH}$ | 2.0 | | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{EABCL}$ | 6.0 | | 4.9 | | 6.0 | | 7.4 | | ns |

*Table 75. EPF10K50V Device Interconnect Timing Microparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 4.7 | | 6.0 | | 7.1 | | 8.2 | ns |
| $t_{DIN2LE}$ | | 2.5 | | 2.6 | | 3.1 | | 3.9 | ns |
| $t_{DIN2DATA}$ | | 4.4 | | 5.9 | | 6.8 | | 7.7 | ns |
| $t_{DCLK2IOE}$ | | 2.5 | | 3.9 | | 4.7 | | 5.5 | ns |
| $t_{DCLK2LE}$ | | 2.5 | | 2.6 | | 3.1 | | 3.9 | ns |
| $t_{SAMELAB}$ | | 0.2 | | 0.2 | | 0.3 | | 0.3 | ns |
| $t_{SAMEROW}$ | | 2.8 | | 3.0 | | 3.2 | | 3.4 | ns |
| $t_{SAMECOLUMN}$ | | 3.0 | | 3.2 | | 3.4 | | 3.6 | ns |
| $t_{DIFFROW}$ | | 5.8 | | 6.2 | | 6.6 | | 7.0 | ns |
| $t_{TWOROWS}$ | | 8.6 | | 9.2 | | 9.8 | | 10.4 | ns |
| $t_{LEPERIPH}$ | | 4.5 | | 5.5 | | 6.1 | | 7.0 | ns |
| $t_{LABCARRY}$ | | 0.3 | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{LABCASC}$ | | 0.0 | | 1.3 | | 1.6 | | 2.0 | ns |

*Table 76. EPF10K50V Device External Timing Parameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 11.2 | | 14.0 | | 17.2 | | 21.1 | ns |
| $t_{INSU}$ *(2), (3)* | 5.5 | | 4.2 | | 5.2 | | 6.9 | | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(3)* | 2.0 | 5.9 | 2.0 | 7.8 | 2.0 | 9.5 | 2.0 | 11.1 | ns |

*Table 77. EPF10K50V Device External Bidirectional Timing Parameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.0 | | 2.8 | | 3.5 | | 4.1 | | ns |
| $t_{INHBIDIR}$ | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ | 2.0 | 5.9 | 2.0 | 7.8 | 2.0 | 9.5 | 2.0 | 11.1 | ns |
| $t_{XZBIDIR}$ | | 8.0 | | 9.8 | | 11.8 | | 14.3 | ns |
| $t_{ZXBIDIR}$ | | 8.0 | | 9.8 | | 11.8 | | 14.3 | ns |

| *Table 103. EPF10K100A Device Interconnect Timing Microparameters* *Note (1)* | | | | | | | |
|---|---|---|---|---|---|---|---|
| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
| | Min | Max | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 4.8 | | 5.4 | | 6.0 | ns |
| $t_{DIN2LE}$ | | 2.0 | | 2.4 | | 2.7 | ns |
| $t_{DIN2DATA}$ | | 2.4 | | 2.7 | | 2.9 | ns |
| $t_{DCLK2IOE}$ | | 2.6 | | 3.0 | | 3.5 | ns |
| $t_{DCLK2LE}$ | | 2.0 | | 2.4 | | 2.7 | ns |
| $t_{SAMELAB}$ | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{SAMEROW}$ | | 1.5 | | 1.7 | | 1.9 | ns |
| $t_{SAMECOLUMN}$ | | 5.5 | | 6.5 | | 7.4 | ns |
| $t_{DIFFROW}$ | | 7.0 | | 8.2 | | 9.3 | ns |
| $t_{TWOROWS}$ | | 8.5 | | 9.9 | | 11.2 | ns |
| $t_{LEPERIPH}$ | | 3.9 | | 4.2 | | 4.5 | ns |
| $t_{LABCARRY}$ | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{LABCASC}$ | | 0.4 | | 0.5 | | 0.6 | ns |

| *Table 104. EPF10K100A Device External Timing Parameters* *Note (1)* | | | | | | | |
|---|---|---|---|---|---|---|---|
| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 12.5 | | 14.5 | | 17.0 | ns |
| $t_{INSU}$ *(2)*, *(3)* | 3.7 | | 4.5 | | 5.1 | | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(3)* | 2.0 | 5.3 | 2.0 | 6.1 | 2.0 | 7.2 | ns |

| *Table 105. EPF10K100A Device External Bidirectional Timing Parameters* *Note (1)* | | | | | | | |
|---|---|---|---|---|---|---|---|
| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 4.9 | | 5.8 | | 6.8 | | ns |
| $t_{INHBIDIR}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ | 2.0 | 5.3 | 2.0 | 6.1 | 2.0 | 7.2 | ns |
| $t_{XZBIDIR}$ | | 7.4 | | 8.6 | | 10.1 | ns |
| $t_{ZXBIDIR}$ | | 7.4 | | 8.6 | | 10.1 | ns |

*Notes to tables:*
(1) All timing parameters are described in Tables 32 through 37 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

## ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. Figure 31 illustrates the incoming and generated clock specifications.

***Figure 31. Specifications for the Incoming & Generated Clocks***

*The $t_I$ parameter refers to the nominal input clock period; the $t_O$ parameter refers to the nominal output clock period.*

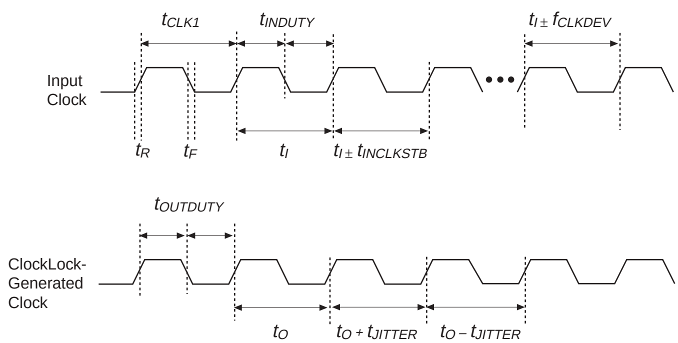



Table 113 summarizes the ClockLock and ClockBoost parameters.

**Table 113. ClockLock & ClockBoost Parameters (Part 1 of 2)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_R$ | Input rise time | | | 2 | ns |
| $t_F$ | Input fall time | | | 2 | ns |
| $t_{INDUTY}$ | Input duty cycle | 45 | | 55 | % |
| $f_{CLK1}$ | Input clock frequency (ClockBoost clock multiplication factor equals 1) | 30 | | 80 | MHz |
| $t_{CLK1}$ | Input clock period (ClockBoost clock multiplication factor equals 1) | 12.5 | | 33.3 | ns |
| $f_{CLK2}$ | Input clock frequency (ClockBoost clock multiplication factor equals 2) | 16 | | 50 | MHz |
| $t_{CLK2}$ | Input clock period (ClockBoost clock multiplication factor equals 2) | 20 | | 62.5 | ns |

$f_{MAX}$ = Maximum operating frequency in MHz
$N$ = Total number of logic cells used in the device
$tog_{LC}$ = Average percent of logic cells toggling at each clock (typically 12.5%)
$K$ = Constant, shown in Tables 114 and 115

*Table 114. FLEX 10K K Constant Values*

| Device | K Value |
|---|---|
| EPF10K10 | 82 |
| EPF10K20 | 89 |
| EPF10K30 | 88 |
| EPF10K40 | 92 |
| EPF10K50 | 95 |
| EPF10K70 | 85 |
| EPF10K100 | 88 |

*Table 115. FLEX 10KA K Constant Values*

| Device | K Value |
|---|---|
| EPF10K10A | 17 |
| EPF10K30A | 17 |
| EPF10K50V | 19 |
| EPF10K100A | 19 |
| EPF10K130V | 22 |
| EPF10K250A | 23 |

This calculation provides an $I_{CC}$ estimate based on typical conditions with no output load. The actual $I_{CC}$ should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

To better reflect actual designs, the power model (and the constant *K* in the power calculation equations) for continuous interconnect FLEX devices assumes that logic cells drive FastTrack Interconnect channels. In contrast, the power model of segmented FPGAs assumes that all logic cells drive only one short interconnect segment. This assumption may lead to inaccurate results, compared to measured power consumption for an actual design in a segmented interconnect FPGA.

Figure 32 shows the relationship between the current and operating frequency of FLEX 10K devices.