



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

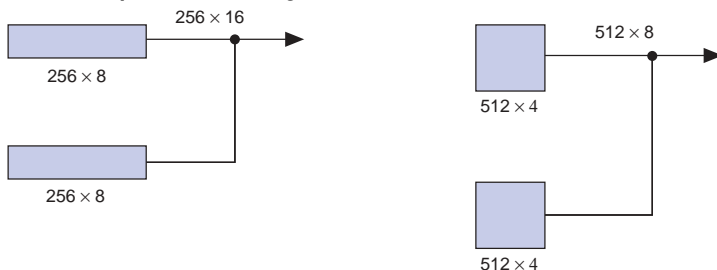
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	216
Number of Logic Elements/Cells	1728
Total RAM Bits	12288
Number of I/O	102
Number of Gates	69000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epf10k30atc144-2n">https://www.e-xfl.com/product-detail/intel/epf10k30atc144-2n</a>

Larger blocks of RAM are created by combining multiple EABs. For example, two  $256 \times 8$  RAM blocks can be combined to form a  $256 \times 16$  RAM block; two  $512 \times 4$  blocks of RAM can be combined to form a  $512 \times 8$  RAM block. See [Figure 3](#).

**Figure 3. Examples of Combining EABs**

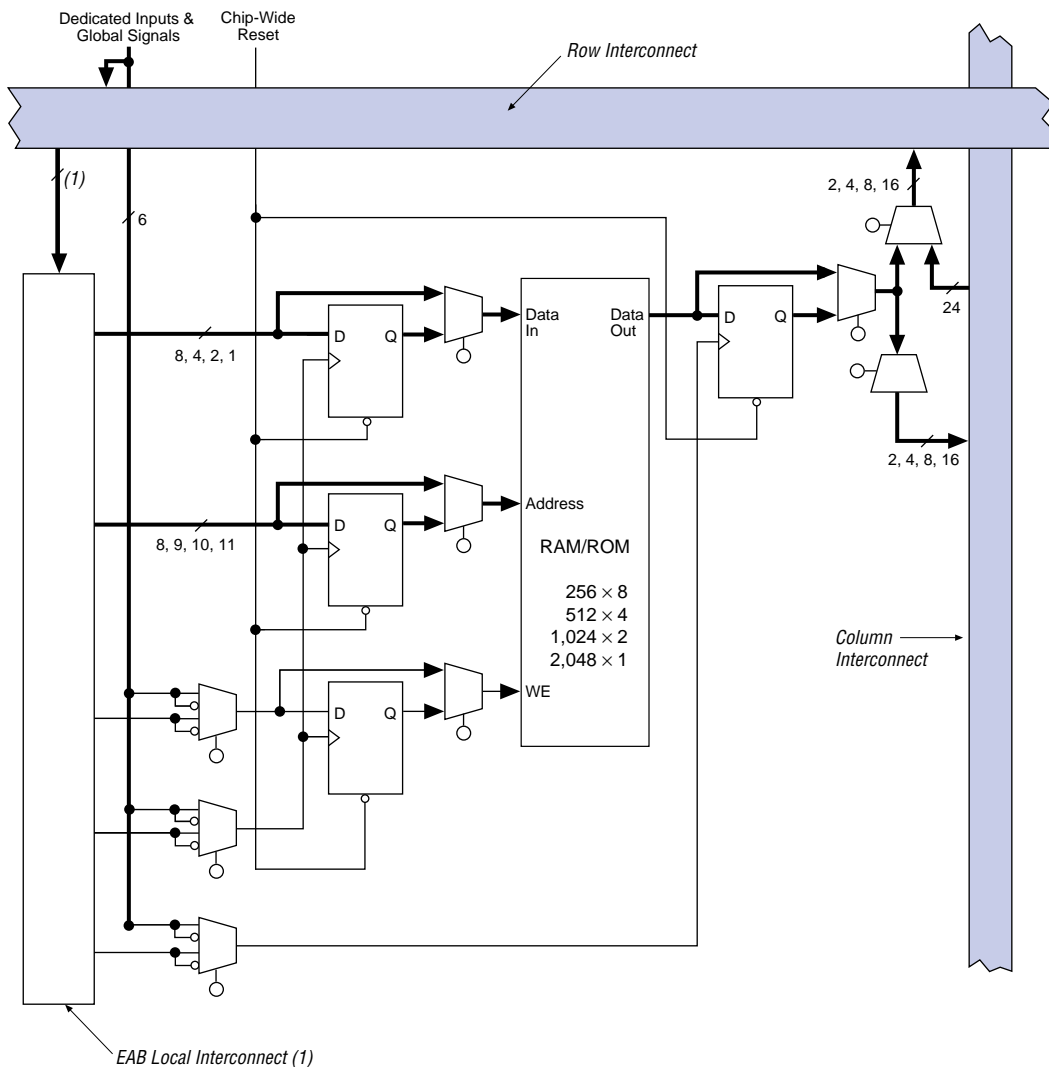


If necessary, all EABs in a device can be cascaded to form a single RAM block. EABs can be cascaded to form RAM blocks of up to 2,048 words without impacting timing. Altera's software automatically combines EABs to meet a designer's RAM specifications.

EABs provide flexible options for driving and controlling clock signals. Different clocks can be used for the EAB inputs and outputs. Registers can be independently inserted on the data input, EAB output, or the address and  $\overline{WE}$  inputs. The global signals and the EAB local interconnect can drive the  $\overline{WE}$  signal. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control the  $\overline{WE}$  signal or the EAB clock signals.

Each EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs. See [Figure 4](#).

**Figure 4. FLEX 10K Embedded Array Block**



**Note:**

- (1) EPF10K10, EPF10K10A, EPF10K20, EPF10K30, EPF10K30A, EPF10K40, EPF10K50, and EPF10K50V devices have 22 EAB local interconnect channels; EPF10K70, EPF10K100, EPF10K100A, EPF10K130V, and EPF10K250A devices have 26.

The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the flipflop is bypassed and the output of the LUT drives the output of the LE.

The LE has two outputs that drive the interconnect; one drives the local interconnect and the other drives either the row or column FastTrack Interconnect. The two outputs can be controlled independently. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, can improve LE utilization because the register and the LUT can be used for unrelated functions.

The FLEX 10K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. The carry chain supports high-speed counters and adders; the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in an LAB and all LABs in the same row. Intensive use of carry and cascade chains can reduce routing flexibility. Therefore, the use of these chains should be limited to speed-critical portions of a design.

### *Carry Chain*

The carry chain provides a very fast (as low as 0.2 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 10K architecture to implement high-speed counters, adders, and comparators of arbitrary width efficiently. Carry chain logic can be created automatically by the Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of carry chains.

Carry chains longer than eight LEs are automatically implemented by linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a row. A carry chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB. For example, the last LE of the first LAB in a row carries to the first LE of the third LAB in the row. The carry chain does not cross the EAB at the middle of the row. For instance, in the EPF10K50 device, the carry chain stops at the eighteenth LAB and a new one begins at the nineteenth LAB.

## FastTrack Interconnect

In the FLEX 10K architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, which is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect. The row interconnect can drive I/O pins and feed other LABs in the device. The column interconnect routes signals between rows and can drive I/O pins.

A row channel can be driven by an LE or by one of three column channels. These four signals feed dual 4-to-1 multiplexers that connect to two specific row channels. These multiplexers, which are connected to each LE, allow column channels to drive row channels even when all eight LEs in an LAB drive the row interconnect.

Each column of LABs is served by a dedicated column interconnect. The column interconnect can then drive I/O pins or another row's interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must be routed to the row interconnect before it can enter an LAB or EAB. Each row channel that is driven by an IOE or EAB can drive one specific column channel.

Access to row and column channels can be switched between LEs in adjacent pairs of LABs. For example, an LE in one LAB can drive the row and column channels normally driven by a particular LE in the adjacent LAB in the same row, and vice versa. This routing flexibility enables routing resources to be used more efficiently. See [Figure 11](#).

Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across devices; it provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock enable or eight output enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by specific LEs. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, an LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal. The chip-wide reset signal will reset all IOE registers, overriding any other control signals.

Tables 8 and 9 list the sources for each peripheral control signal, and the rows that can drive global signals. These tables also show how the output enable, clock enable, clock, and clear signals share 12 peripheral control signals.

**Table 8. EPF10K10, EPF10K20, EPF10K30, EPF10K40 & EPF10K50 Peripheral Bus Sources**

Peripheral Control Signal	EPF10K10 EPF10K10A	EPF10K20	EPF10K30 EPF10K30A	EPF10K40	EPF10K50 EPF10K50V
OE0	Row A	Row A	Row A	Row A	Row A
OE1	Row A	Row B	Row B	Row C	Row B
OE2	Row B	Row C	Row C	Row D	Row D
OE3	Row B	Row D	Row D	Row E	Row F
OE4	Row C	Row E	Row E	Row F	Row H
OE5	Row C	Row F	Row F	Row G	Row J
CLKENA0/CLK0/GLOBAL0	Row A	Row A	Row A	Row B	Row A
CLKENA1/OE6/GLOBAL1	Row A	Row B	Row B	Row C	Row C
CLKENA2/CLR0	Row B	Row C	Row C	Row D	Row E
CLKENA3/OE7/GLOBAL2	Row B	Row D	Row D	Row E	Row G
CLKENA4/CLR1	Row C	Row E	Row E	Row F	Row I
CLKENA5/CLK1/GLOBAL3	Row C	Row F	Row F	Row H	Row J

**Table 9. EPF10K70, EPF10K100, EPF10K130V & EPF10K250A Peripheral Bus Sources**

Peripheral Control Signal	EPF10K70	EPF10K100 EPF10K100A	EPF10K130V	EPF10K250A
OE0	Row A	Row A	Row C	Row E
OE1	Row B	Row C	Row E	Row G
OE2	Row D	Row E	Row G	Row I
OE3	Row I	Row L	Row N	Row P
OE4	Row G	Row I	Row K	Row M
OE5	Row H	Row K	Row M	Row O
CLKENA0/CLK0/GLOBAL0	Row E	Row F	Row H	Row J
CLKENA1/OE6/GLOBAL1	Row C	Row D	Row F	Row H
CLKENA2/CLR0	Row B	Row B	Row D	Row F
CLKENA3/OE7/GLOBAL2	Row F	Row H	Row J	Row L
CLKENA4/CLR1	Row H	Row J	Row L	Row N
CLKENA5/CLK1/GLOBAL3	Row E	Row G	Row I	Row K

**Table 15. 32-Bit FLEX 10K Device IDCODE** *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)
EPF10K10, EPF10K10A	0000	0001 0000 0001 0000	00001101110	1
EPF10K20	0000	0001 0000 0010 0000	00001101110	1
EPF10K30, EPF10K30A	0000	0001 0000 0011 0000	00001101110	1
EPF10K40	0000	0001 0000 0100 0000	00001101110	1
EPF10K50, EPF10K50V	0000	0001 0000 0101 0000	00001101110	1
EPF10K70	0000	0001 0000 0111 0000	00001101110	1
EPF10K100, EPF10K100A	0000	0000 0001 0000 0000	00001101110	1
EPF10K130V	0000	0000 0001 0011 0000	00001101110	1
EPF10K250A	0000	0000 0010 0101 0000	00001101110	1

**Notes:**

- (1) The most significant bit (MSB) is on the left.  
 (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

FLEX 10K devices include weak pull-ups on JTAG pins.



For more information, see the following documents:

- *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Jam Programming & Test Language Specification*

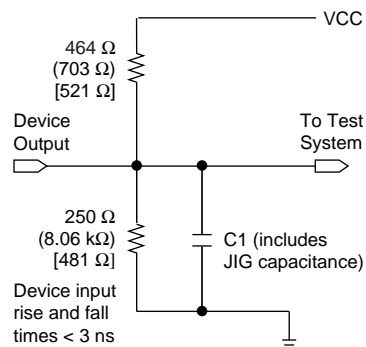


## Generic Testing

Each FLEX 10K device is functionally tested. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% yield. AC test measurements for FLEX 10K devices are made under conditions equivalent to those shown in Figure 19. Multiple test patterns can be used to configure devices during all stages of the production flow.

**Figure 19. FLEX 10K AC Test Conditions**

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers without parentheses are for 5.0-V devices or outputs. Numbers in parentheses are for 3.3-V devices or outputs. Numbers in brackets are for 2.5-V devices or outputs.



## Operating Conditions

Tables 17 through 21 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 5.0-V FLEX 10K devices.

**Table 17. FLEX 10K 5.0-V Device Absolute Maximum Ratings** *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	Supply voltage	With respect to ground (2)	-2.0	7.0	V
$V_I$	DC input voltage		-2.0	7.0	V
$I_{OUT}$	DC output current, per pin		-25	25	mA
$T_{STG}$	Storage temperature	No bias	-65	150	°C
$T_{AMB}$	Ambient temperature	Under bias	-65	135	°C
$T_J$	Junction temperature	Ceramic packages, under bias		150	°C
		PQFP, TQFP, RQFP, and BGA packages, under bias		135	°C

**Table 18. FLEX 10K 5.0-V Device Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage for internal logic and input buffers	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
$V_{CCIO}$	Supply voltage for output buffers, 5.0-V operation	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
$V_I$	Input voltage		−0.5	$V_{CCINT} + 0.5$	V
$V_O$	Output voltage		0	$V_{CCIO}$	V
$T_A$	Ambient temperature	For commercial use	0	70	° C
		For industrial use	−40	85	° C
$T_J$	Operating temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
$t_R$	Input rise time			40	ns
$t_F$	Input fall time			40	ns

**Table 36. Interconnect Timing Microparameters** *Note (1)*

Symbol	Parameter	Conditions
$t_{DIN2IOE}$	Delay from dedicated input pin to IOE control input	(7)
$t_{DCLK2LE}$	Delay from dedicated clock pin to LE or EAB clock	(7)
$t_{DIN2DATA}$	Delay from dedicated input or clock to LE or EAB data	(7)
$t_{DCLK2IOE}$	Delay from dedicated clock pin to IOE clock	(7)
$t_{DIN2LE}$	Delay from dedicated input pin to LE or EAB control input	(7)
$t_{SAMELAB}$	Routing delay for an LE driving another LE in the same LAB	
$t_{SAMEROW}$	Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row	(7)
$t_{SAMECOLUMN}$	Routing delay for an LE driving an IOE in the same column	(7)
$t_{DIFFROW}$	Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row	(7)
$t_{TROWROWS}$	Routing delay for a row IOE or EAB driving an LE or EAB in a different row	(7)
$t_{LEPERIPH}$	Routing delay for an LE driving a control signal of an IOE via the peripheral control bus	(7)
$t_{LABCARRY}$	Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	

**Table 37. External Timing Parameters** *Notes (8), (10)*

Symbol	Parameter	Conditions
$t_{DRR}$	Register-to-register delay via four LEs, three row interconnects, and four local interconnects	(9)
$t_{INSU}$	Setup time with global clock at IOE register	
$t_{INH}$	Hold time with global clock at IOE register	
$t_{OUTCO}$	Clock-to-output delay with global clock at IOE register	

**Table 38. External Bidirectional Timing Parameters** *Note (10)*

Symbol	Parameter	Condition
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at adjacent LE register	
$t_{INHBDIR}$	Hold time for bidirectional pins with global clock at adjacent LE register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	
$t_{XZBIDIR}$	Synchronous IOE output buffer disable delay	
$t_{ZXBIDIR}$	Synchronous IOE output buffer enable delay, slow slew rate = off	

**Table 66. EPF10K100 Device EAB Internal Microparameters** *Note (1)*

Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.5		1.5		1.9	ns
$t_{EABDATA2}$		4.8		4.8		6.0	ns
$t_{EABWE1}$		1.0		1.0		1.2	ns
$t_{EABWE2}$		5.0		5.0		6.2	ns
$t_{EABCLK}$		1.0		1.0		2.2	ns
$t_{EABCO}$		0.5		0.5		0.6	ns
$t_{EABYPASS}$		1.5		1.5		1.9	ns
$t_{EABSU}$	1.5		1.5		1.8		ns
$t_{EABH}$	2.0		2.0		2.5		ns
$t_{AA}$		8.7		8.7		10.7	ns
$t_{WP}$	5.8		5.8		7.2		ns
$t_{WDSU}$	1.6		1.6		2.0		ns
$t_{WDH}$	0.3		0.3		0.4		ns
$t_{WASU}$	0.5		0.5		0.6		ns
$t_{WAH}$	1.0		1.0		1.2		ns
$t_{WO}$		5.0		5.0		6.2	ns
$t_{DD}$		5.0		5.0		6.2	ns
$t_{EABOUT}$		0.5		0.5		0.6	ns
$t_{EABCH}$	4.0		4.0		4.0		ns
$t_{EABCL}$	5.8		5.8		7.2		ns

**Table 72. EPF10K50V Device IOE Timing Microparameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{IOD}$		1.2		1.6		1.9		2.1	ns
$t_{IOC}$		0.3		0.4		0.5		0.5	ns
$t_{IOCO}$		0.3		0.3		0.4		0.4	ns
$t_{IOCOMB}$		0.0		0.0		0.0		0.0	ns
$t_{IOSU}$	2.8		2.8		3.4		3.9		ns
$t_{IOH}$	0.7		0.8		1.0		1.4		ns
$t_{IOCLR}$		0.5		0.6		0.7		0.7	ns
$t_{OD1}$		2.8		3.2		3.9		4.7	ns
$t_{OD2}$		—		—		—		—	ns
$t_{OD3}$		6.5		6.9		7.6		8.4	ns
$t_{XZ}$		2.8		3.1		3.8		4.6	ns
$t_{ZX1}$		2.8		3.1		3.8		4.6	ns
$t_{ZX2}$		—		—		—		—	ns
$t_{ZX3}$		6.5		6.8		7.5		8.3	ns
$t_{INREG}$		5.0		5.7		7.0		9.0	ns
$t_{IOFD}$		1.5		1.9		2.3		2.7	ns
$t_{INCOMB}$		1.5		1.9		2.3		2.7	ns

**Table 73. EPF10K50V Device EAB Internal Microparameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.7		2.8		3.4		4.6	ns
$t_{EABDATA2}$		4.9		3.9		4.8		5.9	ns
$t_{EABWE1}$		0.0		2.5		3.0		3.7	ns
$t_{EABWE2}$		4.0		4.1		5.0		6.2	ns
$t_{EABCLK}$		0.4		0.8		1.0		1.2	ns
$t_{EABCO}$		0.1		0.2		0.3		0.4	ns
$t_{EABYPASS}$		0.9		1.1		1.3		1.6	ns
$t_{EABSU}$	0.8		1.5		1.8		2.2		ns
$t_{EABH}$	0.8		1.6		2.0		2.5		ns
$t_{AA}$		5.5		8.2		10.0		12.4	ns
$t_{WP}$	6.0		4.9		6.0		7.4		ns
$t_{WDSU}$	0.1		0.8		1.0		1.2		ns
$t_{WDH}$	0.1		0.2		0.3		0.4		ns
$t_{WASU}$	0.1		0.4		0.5		0.6		ns
$t_{WAH}$	0.1		0.8		1.0		1.2		ns
$t_{WO}$		2.8		4.3		5.3		6.5	ns
$t_{DD}$		2.8		4.3		5.3		6.5	ns
$t_{EABOUT}$		0.5		0.4		0.5		0.6	ns
$t_{EABCH}$	2.0		4.0		4.0		4.0		ns
$t_{EABCL}$	6.0		4.9		6.0		7.4		ns

**Table 79. EPF10K130V Device IOE Timing Microparameters** *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{IOD}$		1.3		1.6		2.0	ns
$t_{IOC}$		0.4		0.5		0.7	ns
$t_{IOCO}$		0.3		0.4		0.5	ns
$t_{IOCOMB}$		0.0		0.0		0.0	ns
$t_{IOSU}$	2.6		3.3		3.8		ns
$t_{IOH}$	0.0		0.0		0.0		ns
$t_{IOCLR}$		1.7		2.2		2.7	ns
$t_{OD1}$		3.5		4.4		5.0	ns
$t_{OD2}$		—		—		—	ns
$t_{OD3}$		8.2		8.1		9.7	ns
$t_{XZ}$		4.9		6.3		7.4	ns
$t_{ZX1}$		4.9		6.3		7.4	ns
$t_{ZX2}$		—		—		—	ns
$t_{ZX3}$		9.6		10.0		12.1	ns
$t_{INREG}$		7.9		10.0		12.6	ns
$t_{IOFD}$		6.2		7.9		9.9	ns
$t_{INCOMB}$		6.2		7.9		9.9	ns

**Table 94. EPF10K30A Device EAB Internal Microparameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		5.5		6.5		8.5	ns
$t_{EABDATA2}$		1.1		1.3		1.8	ns
$t_{EABWE1}$		2.4		2.8		3.7	ns
$t_{EABWE2}$		2.1		2.5		3.2	ns
$t_{EABCLK}$		0.0		0.0		0.2	ns
$t_{EABCO}$		1.7		2.0		2.6	ns
$t_{EABYPASS}$		0.0		0.0		0.3	ns
$t_{EABSU}$	1.2		1.4		1.9		ns
$t_{EABH}$	0.1		0.1		0.3		ns
$t_{AA}$		4.2		5.0		6.5	ns
$t_{WP}$	3.8		4.5		5.9		ns
$t_{WDSU}$	0.1		0.1		0.2		ns
$t_{WDH}$	0.1		0.1		0.2		ns
$t_{WASU}$	0.1		0.1		0.2		ns
$t_{WAH}$	0.1		0.1		0.2		ns
$t_{WO}$		3.7		4.4		6.4	ns
$t_{DD}$		3.7		4.4		6.4	ns
$t_{EABOUT}$		0.0		0.1		0.6	ns
$t_{EABCH}$	3.0		3.5		4.0		ns
$t_{EABCL}$	3.8		4.5		5.9		ns



**Notes to tables:**

- (1) All timing parameters are described in Tables 32 through 38 in this data sheet.
- (2) Using an LE to register the signal may provide a lower setup time.
- (3) This parameter is specified by characterization.

Tables 99 through 105 show EPF10K100A device internal and external timing parameters.

**Table 99. EPF10K100A Device LE Timing Microparameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{LUT}$		1.0		1.2		1.4	ns
$t_{CLUT}$		0.8		0.9		1.1	ns
$t_{RLUT}$		1.4		1.6		1.9	ns
$t_{PACKED}$		0.4		0.5		0.5	ns
$t_{EN}$		0.6		0.7		0.8	ns
$t_{CICO}$		0.2		0.2		0.3	ns
$t_{CGEN}$		0.4		0.4		0.6	ns
$t_{CGENR}$		0.6		0.7		0.8	ns
$t_{CASC}$		0.7		0.9		1.0	ns
$t_C$		0.9		1.0		1.2	ns
$t_{CO}$		0.2		0.3		0.3	ns
$t_{COMB}$		0.6		0.7		0.8	ns
$t_{SU}$	0.8		1.0		1.2		ns
$t_H$	0.3		0.5		0.5		ns
$t_{PRE}$		0.3		0.3		0.4	ns
$t_{CLR}$		0.3		0.3		0.4	ns
$t_{CH}$	2.5		3.5		4.0		ns
$t_{CL}$	2.5		3.5		4.0		ns

**Table 103. EPF10K100A Device Interconnect Timing Microparameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		4.8		5.4		6.0	ns
$t_{DIN2LE}$		2.0		2.4		2.7	ns
$t_{DIN2DATA}$		2.4		2.7		2.9	ns
$t_{DCLK2IOE}$		2.6		3.0		3.5	ns
$t_{DCLK2LE}$		2.0		2.4		2.7	ns
$t_{SAMELAB}$		0.1		0.1		0.1	ns
$t_{SAMEROW}$		1.5		1.7		1.9	ns
$t_{SAMECOLUMN}$		5.5		6.5		7.4	ns
$t_{DIFFROW}$		7.0		8.2		9.3	ns
$t_{TWOROWS}$		8.5		9.9		11.2	ns
$t_{LEPERIPH}$		3.9		4.2		4.5	ns
$t_{LABCARRY}$		0.2		0.2		0.3	ns
$t_{LABCASC}$		0.4		0.5		0.6	ns

**Table 104. EPF10K100A Device External Timing Parameters** *Note (1)*

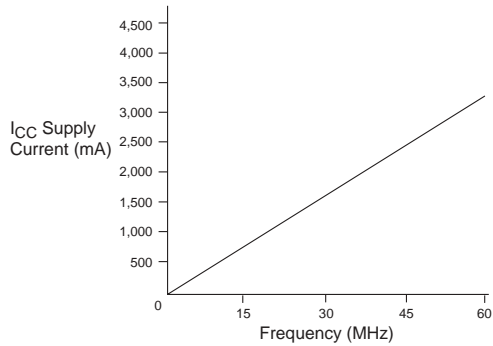
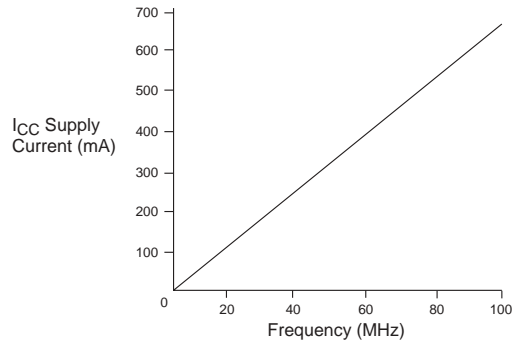
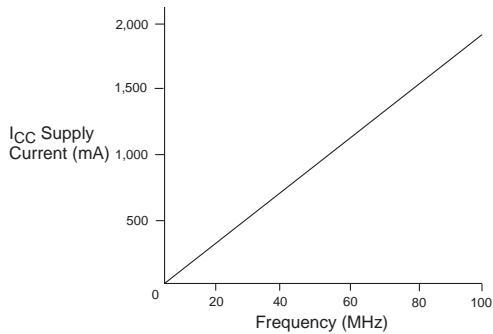
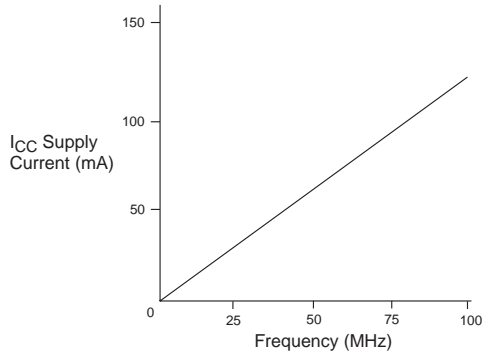
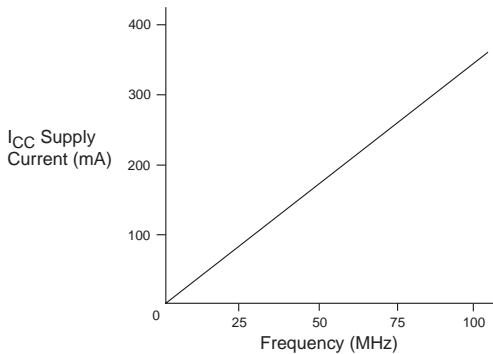
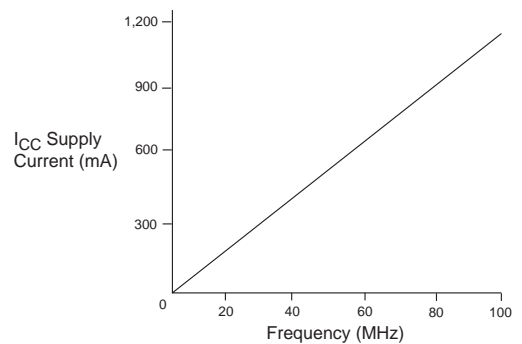
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DRR}$		12.5		14.5		17.0	ns
$t_{INSU}$ (2), (3)	3.7		4.5		5.1		ns
$t_{INH}$ (3)	0.0		0.0		0.0		ns
$t_{OUTCO}$ (3)	2.0	5.3	2.0	6.1	2.0	7.2	ns

**Table 105. EPF10K100A Device External Bidirectional Timing Parameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	4.9		5.8		6.8		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	5.3	2.0	6.1	2.0	7.2	ns
$t_{XZBIDIR}$		7.4		8.6		10.1	ns
$t_{ZXBIDIR}$		7.4		8.6		10.1	ns

**Table 107. EPF10K250A Device IOE Timing Microparameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{IOD}$		1.2		1.3		1.6	ns
$t_{IOC}$		0.4		0.4		0.5	ns
$t_{IOCO}$		0.8		0.9		1.1	ns
$t_{IOCOMB}$		0.7		0.7		0.8	ns
$t_{IOSU}$	2.7		3.1		3.6		ns
$t_{IOH}$	0.2		0.3		0.3		ns
$t_{IOCLR}$		1.2		1.3		1.6	ns
$t_{OD1}$		3.2		3.6		4.2	ns
$t_{OD2}$		5.9		6.7		7.8	ns
$t_{OD3}$		8.7		9.8		11.5	ns
$t_{XZ}$		3.8		4.3		5.0	ns
$t_{ZX1}$		3.8		4.3		5.0	ns
$t_{ZX2}$		6.5		7.4		8.6	ns
$t_{ZX3}$		9.3		10.5		12.3	ns
$t_{INREG}$		8.2		9.3		10.9	ns
$t_{IOFD}$		9.0		10.2		12.0	ns
$t_{INCOMB}$		9.0		10.2		12.0	ns

**Figure 32.  $I_{CCACTIVE}$  vs. Operating Frequency (Part 2 of 3)****EPF10K100****EPF10K50V****EPF10K130V****EPF10K10A****EPF10K30A****EPF10K100A**



101 Innovation Drive  
San Jose, CA 95134  
(408) 544-7000  
<http://www.altera.com>  
**Applications Hotline:**  
(800) 800-EPLD  
**Customer Marketing:**  
(408) 544-7104  
**Literature Services:**  
[lit\\_req@altera.com](mailto:lit_req@altera.com)

Copyright © 2003 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.



I.S. EN ISO 9001