Intel - EPF10K30ATC144-3N Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	216
Number of Logic Elements/Cells	1728
Total RAM Bits	12288
Number of I/O	102
Number of Gates	69000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k30atc144-3n

Notes to tables:

(1) FLEX 10K and FLEX 10KA device package types include plastic J-lead chip carrier (PLCC), thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), ball-grid array (BGA), pin-grid array (PGA), and FineLine BGA™ packages.

(2) This option is supported with a 256-pin FineLine BGA package. By using SameFrame pin migration, all FineLine BGA packages are pin compatible. For example, a board can be designed to support both 256-pin and 484-pin FineLine BGA packages. The Altera software automatically avoids conflicting pins when future migration is set.

General Description

Altera's FLEX 10K devices are the industry's first embedded PLDs. Based on reconfigurable CMOS SRAM elements, the Flexible Logic Element MatriX (FLEX) architecture incorporates all features necessary to implement common gate array megafunctions. With up to 250,000 gates, the FLEX 10K family provides the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device.

FLEX 10K devices are reconfigurable, which allows 100% testing prior to shipment. As a result, the designer is not required to generate test vectors for fault coverage purposes. Additionally, the designer does not need to manage inventories of different ASIC designs; FLEX 10K devices can be configured on the board for the specific functionality required.

Table 6 shows FLEX 10K performance for some common designs. All performance values were obtained with Synopsys DesignWare or LPM functions. No special design technique was required to implement the applications; the designer simply inferred or instantiated a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

Table 6. FLEX 10K & FLEX 10KA Performance

Application	Resources Used		Performance				Units
	LEs	EABs	-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	-4 Speed Grade	
16-bit loadable counter *(1)*	16	0	204	166	125	95	MHz
16-bit accumulator *(1)*	16	0	204	166	125	95	MHz
16-to-1 multiplexer *(2)*	10	0	4.2	5.8	6.0	7.0	ns
256 × 8 RAM read cycle speed *(3)*	0	1	172	145	108	84	MHz
256 × 8 RAM write cycle speed *(3)*	0	1	106	89	68	63	MHz

Notes:

(1) The speed grade of this application is limited because of clock high and low specifications.

(2) This application uses combinatorial inputs and outputs.

(3) This application uses registered inputs and outputs.

The FLEX 10K architecture is similar to that of embedded gate arrays, the fastest-growing segment of the gate array market. As with standard gate arrays, embedded gate arrays implement general logic in a conventional "sea-of-gates" architecture. In addition, embedded gate arrays have dedicated die areas for implementing large, specialized functions. By embedding functions in silicon, embedded gate arrays provide reduced die area and increased speed compared to standard gate arrays. However, embedded megafunctions typically cannot be customized, limiting the designer's options. In contrast, FLEX 10K devices are programmable, providing the designer with full control over embedded megafunctions and general logic while facilitating iterative design changes during debugging.

Each FLEX 10K device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), microcontroller, wide-data-path manipulation, and data-transformation functions. The logic array performs the same function as the sea-of-gates in the gate array: it is used to implement general logic, such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

FLEX 10K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers the EPC1, EPC2, EPC16, and EPC1441 configuration devices, which configure FLEX 10K devices via a serial data stream. Configuration data can also be downloaded from system RAM or from Altera's BitBlaster™ serial download cable or ByteBlasterMV™ parallel port download cable. After a FLEX 10K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 320 ms, real-time changes can be made during system operation.

FLEX 10K devices contain an optimized interface that permits microprocessors to configure FLEX 10K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat a FLEX 10K device as memory and configure the device by writing to a virtual memory location, making it very easy for the designer to reconfigure the device.

For more information, see the following documents:

- *Configuration Devices for APEX & FLEX Devices Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Application Note 116 (Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices)*

FLEX 10K devices are supported by Altera development systems; single, integrated packages that offer schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The Altera software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Altera software works easily with common gate array EDA tools for synthesis and simulation. For example, the Altera software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Altera software contains EDA libraries that use device-specific features such as carry chains which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Altera development systems include DesignWare functions that are optimized for the FLEX 10K architecture.

The Altera development systems run on Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations.

See the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* for more information.

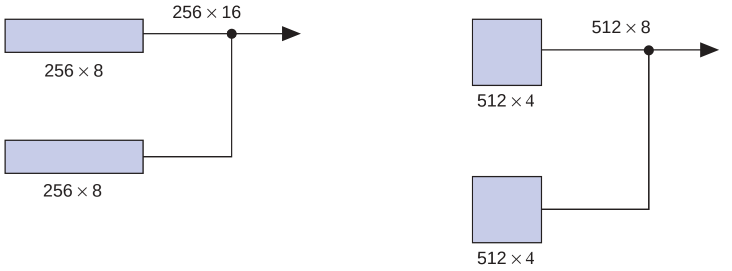
Functional Description

Each FLEX 10K device contains an embedded array to implement memory and specialized logic functions, and a logic array to implement general logic.

The embedded array consists of a series of EABs. When implementing memory functions, each EAB provides 2,048 bits, which can be used to create RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. When implementing logic, each EAB can contribute 100 to 600 gates towards complex logic functions, such as multipliers, microcontrollers, state machines, and DSP functions. EABs can be used independently, or multiple EABs can be combined to implement larger functions.

Larger blocks of RAM are created by combining multiple EABs. For example, two 256 × 8 RAM blocks can be combined to form a 256 × 16 RAM block; two 512 × 4 blocks of RAM can be combined to form a 512 × 8 RAM block. See Figure 3.

Figure 3. Examples of Combining EABs



If necessary, all EABs in a device can be cascaded to form a single RAM block. EABs can be cascaded to form RAM blocks of up to 2,048 words without impacting timing. Altera's software automatically combines EABs to meet a designer's RAM specifications.

EABs provide flexible options for driving and controlling clock signals. Different clocks can be used for the EAB inputs and outputs. Registers can be independently inserted on the data input, EAB output, or the address and `WE` inputs. The global signals and the EAB local interconnect can drive the `WE` signal. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control the `WE` signal or the EAB clock signals.

Each EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs. See Figure 4.

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks; the other two can be used for clear/preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I/O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I/O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

Logic Element

The LE, the smallest unit of logic in the FLEX 10K architecture, has a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect. See Figure 6.

Figure 6. FLEX 10K Logic Element

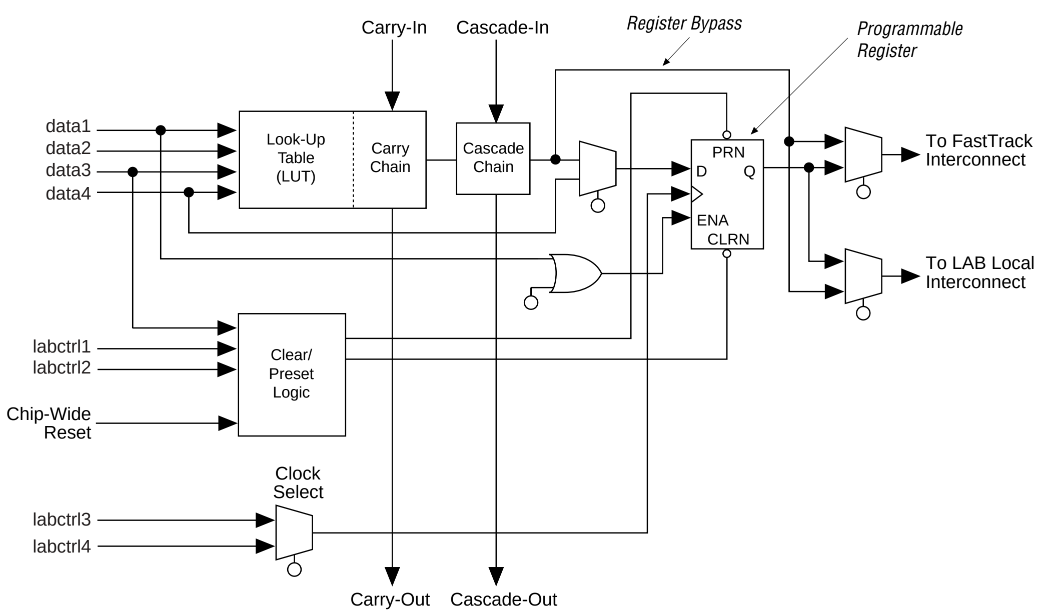
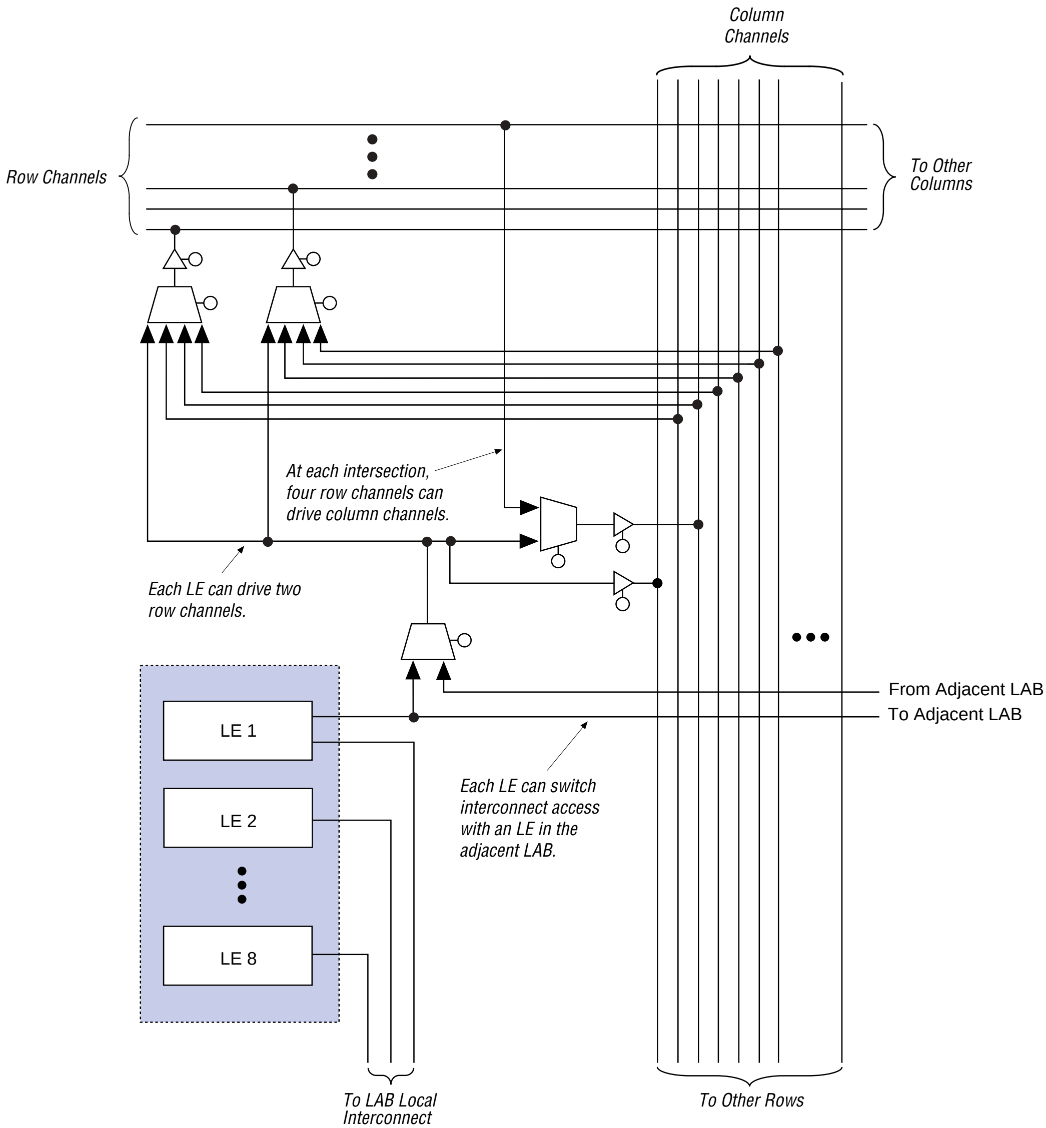


Figure 11. LAB Connections to Row & Column Interconnect



For improved routing, the row interconnect is comprised of a combination of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in half of the row. The EAB can be driven by the half-length channels in the left half of the row and by the full-length channels. The EAB drives out to the full-length channels. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-row channel, thereby saving the other half of the channel for the other half of the row.

Table 7 summarizes the FastTrack Interconnect resources available in each FLEX 10K device.

Table 7. FLEX 10K FastTrack Interconnect Resources

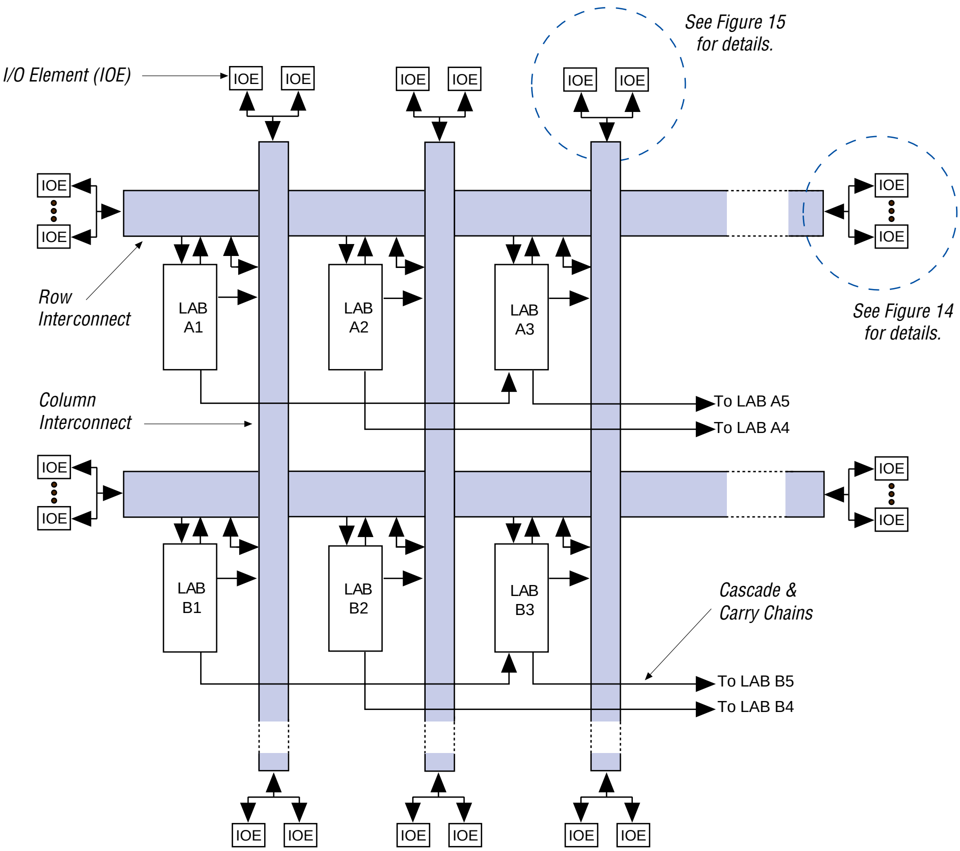
Device	Rows	Channels per Row	Columns	Channels per Column
EPF10K10 EPF10K10A	3	144	24	24
EPF10K20	6	144	24	24
EPF10K30 EPF10K30A	6	216	36	24
EPF10K40	8	216	36	24
EPF10K50 EPF10K50V	10	216	36	24
EPF10K70	9	312	52	24
EPF10K100 EPF10K100A	12	312	52	24
EPF10K130V	16	312	52	32
EPF10K250A	20	456	76	40

In addition to general-purpose I/O pins, FLEX 10K devices have six dedicated input pins that provide low-skew signal distribution across the device. These six inputs can be used for global clock, clear, preset, and peripheral output enable and clock enable control signals. These signals are available as control signals for all LABs and IOEs in the device.

The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device. However, the use of dedicated inputs as data inputs can introduce additional delay into the control signal network.

Figure 12 shows the interconnection of adjacent LABs and EABs with row, column, and local interconnects, as well as the associated cascade and carry chains. Each LAB is labeled according to its location: a letter represents the row and a number represents the column. For example, LAB B3 is in row B, column 3.

Figure 12. Interconnect Resources



Signals on the peripheral control bus can also drive the four global signals, referred to as GLOBAL0 through GLOBAL3 in Tables 8 and 9. The internally generated signal can drive the global signal, providing the same low-skew, low-delay characteristics for an internally generated signal as for a signal driven by an input. This feature is ideal for internally generated clear or clock signals with high fan-out. When a global signal is driven by internal logic, the dedicated input pin that drives that global signal cannot be used. The dedicated input pin should be driven to a known logic state (such as ground) and not be allowed to float.

When the chip-wide output enable pin is held low, it will tri-state all pins on the device. This option can be set in the Global Project Device Options menu. Additionally, the registers in the IOE can be reset by holding the chip-wide reset pin low.

Row-to-IOE Connections

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Up to eight IOEs connect to each side of each row channel. See Figure 14.

Figure 14. FLEX 10K Row-to-IOE Connections

The values for m and n are provided in Table 10.

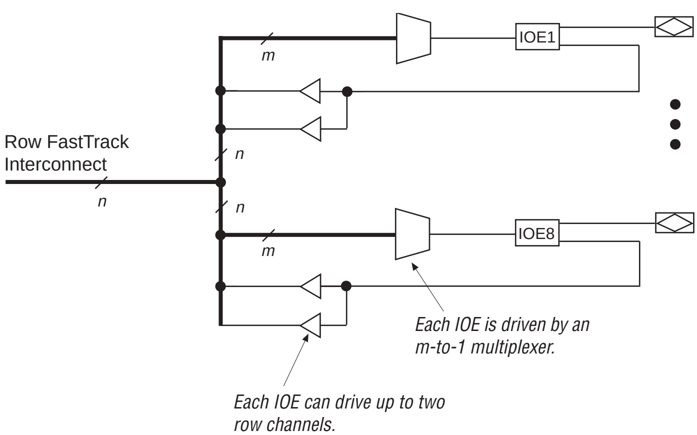


Table 10 lists the FLEX 10K row-to-IOE interconnect resources.

Table 10. FLEX 10K Row-to-IOE Interconnect Resources

Device	Channels per Row (*n*)	Row Channels per Pin (*m*)
EPF10K10 EPF10K10A	144	18
EPF10K20	144	18
EPF10K30 EPF10K30A	216	27
EPF10K40	216	27
EPF10K50 EPF10K50V	216	27
EPF10K70	312	39
EPF10K100 EPF10K100A	312	39
EPF10K130V	312	39
EPF10K250A	456	57

Column-to-IOE Connections

When an IOE is used as an input, it can drive up to two separate column channels. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the column channels. Two IOEs connect to each side of the column channels. Each IOE can be driven by column channels via a multiplexer. The set of column channels that each IOE can access is different for each IOE. See Figure 15.

ClockLock & ClockBoost Features

To support high-speed designs, selected FLEX 10K devices offer optional ClockLock and ClockBoost circuitry containing a phase-locked loop (PLL) that is used to increase design speed and reduce resource usage. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost feature allows the designer to distribute a low-speed clock and multiply that clock on-device. Combined, the ClockLock and ClockBoost features provide significant improvements in system performance and bandwidth.

The ClockLock and ClockBoost features in FLEX 10K devices are enabled through the Altera software. External devices are not required to use these features. The output of the ClockLock and ClockBoost circuits is not available at any of the device pins.

The ClockLock and ClockBoost circuitry locks onto the rising edge of the incoming clock. The circuit output can only drive the clock inputs of registers; the generated clock cannot be gated or inverted.

The dedicated clock pin (`GCLK1`) supplies the clock to the ClockLock and ClockBoost circuitry. When the dedicated clock pin is driving the ClockLock or ClockBoost circuitry, it cannot drive elsewhere in the device.

In designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to `GCLK1`. With the Altera software, `GCLK1` can feed both the ClockLock and ClockBoost circuitry in the FLEX 10K device. However, when both circuits are used, the other clock pin (`GCLK0`) cannot be used. Figure 17 shows a block diagram of how to enable both the ClockLock and ClockBoost circuits in the Altera software. The example shown is a schematic, but a similar approach applies for designs created in AHDL, VHDL, and Verilog HDL. When the ClockLock and ClockBoost circuits are used simultaneously, the input frequency parameter must be the same for both circuits. In Figure 17, the input frequency must meet the requirements specified when the ClockBoost multiplication factor is two.

Table 12 describes the FLEX 10K device supply voltages and MultiVolt I/O support levels.

Table 12. Supply Voltages & MultiVolt I/O Support Levels

Devices	Supply Voltage (V)		MultiVolt I/O Support Levels (V)	
	V_{CCINT}	V_{CCIO}	Input	Output
FLEX 10K *(1)*	5.0	5.0	3.3 or 5.0	5.0
	5.0	3.3	3.3 or 5.0	3.3 or 5.0
EPF10K50V *(1)*	3.3	3.3	3.3 or 5.0	3.3 or 5.0
EPF10K130V	3.3	3.3	3.3 or 5.0	3.3 or 5.0
FLEX 10KA *(1)*	3.3	3.3	2.5, 3.3, or 5.0	3.3 or 5.0
	3.3	2.5	2.5, 3.3, or 5.0	2.5

Note

(1) 240-pin QFP packages do not support the MultiVolt I/O features, so they do not have separate V_{CCIO} pins.

Power Sequencing & Hot-Socketing

Because FLEX 10K devices can be used in a multi-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power supplies can be powered in any order.

Signals can be driven into FLEX 10KA devices before and during power up without damaging the device. Additionally, FLEX 10KA devices do not drive out during power up. Once operating conditions are reached, FLEX 10KA devices operate as specified by the user.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All FLEX 10K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. All FLEX 10K devices can also be configured using the JTAG pins through the BitBlaster serial download cable, or ByteBlasterMV parallel port download cable, or via hardware that uses the Jam™ programming and test language. JTAG BST can be performed before or after configuration, but not during configuration. FLEX 10K devices support the JTAG instructions shown in Table 13.

Figure 18 shows the timing requirements for the JTAG signals.

Figure 18. JTAG Waveforms

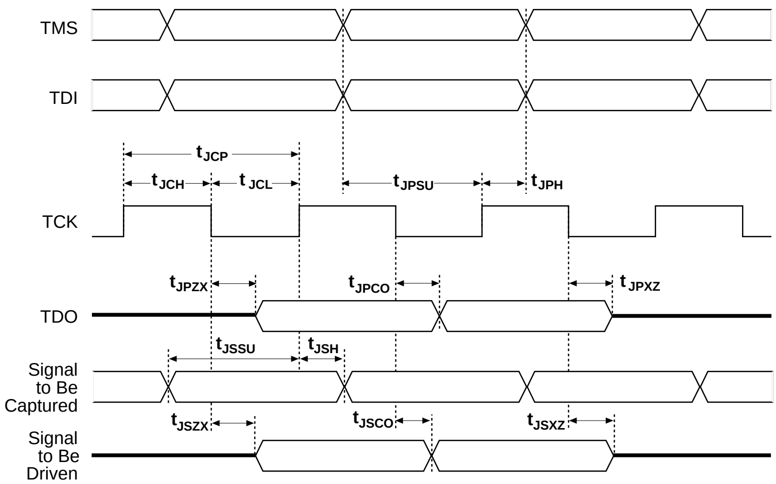


Table 16 shows the timing parameters and values for FLEX 10K devices.

Table 16. JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high-impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

Table 19. FLEX 10K 5.0-V Device DC Operating Conditions *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CCINT} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 4.75 V *(7)*	2.4			V
	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.00 V *(7)*	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(7)*	V_{CCIO} – 0.2			V
V_{OL}	5.0-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 4.75 V *(8)*			0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(8)*			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(8)*			0.2	V
I_I	Input pin leakage current	V_I = V_{CC} or ground *(9)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = V_{CC} or ground *(9)*	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load		0.5	10	mA

Table 20. 5.0-V Device Capacitance of EPF10K10, EPF10K20 & EPF10K30 Devices *Note (10)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Table 21. 5.0-V Device Capacitance of EPF10K40, EPF10K50, EPF10K70 & EPF10K100 Devices *Note (10)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Figures 25 through 27 show the delays that correspond to various paths and functions within the LE, IOE, and EAB timing models.

Figure 25. FLEX 10K Device LE Timing Model

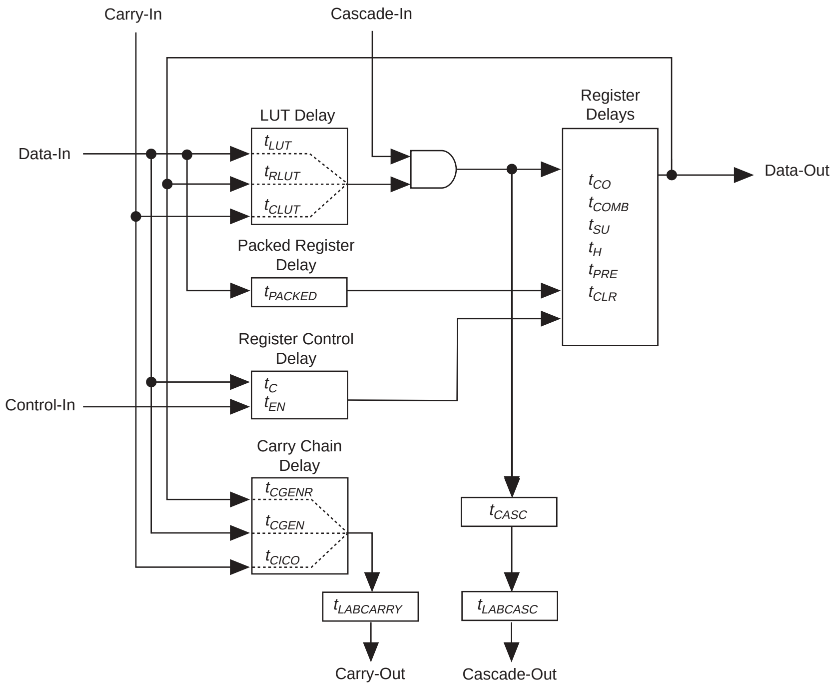


Table 66. EPF10K100 Device EAB Internal Microparameters *Note (1)*

Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.5		1.5		1.9	ns
$t_{EABDATA2}$		4.8		4.8		6.0	ns
t_{EABWE1}		1.0		1.0		1.2	ns
t_{EABWE2}		5.0		5.0		6.2	ns
t_{EABCLK}		1.0		1.0		2.2	ns
t_{EABCO}		0.5		0.5		0.6	ns
$t_{EABBYPASS}$		1.5		1.5		1.9	ns
t_{EABSU}	1.5		1.5		1.8		ns
t_{EABH}	2.0		2.0		2.5		ns
t_{AA}		8.7		8.7		10.7	ns
t_{WP}	5.8		5.8		7.2		ns
t_{WDSU}	1.6		1.6		2.0		ns
t_{WDH}	0.3		0.3		0.4		ns
t_{WASU}	0.5		0.5		0.6		ns
t_{WAH}	1.0		1.0		1.2		ns
t_{WO}		5.0		5.0		6.2	ns
t_{DD}		5.0		5.0		6.2	ns
t_{EABOUT}		0.5		0.5		0.6	ns
t_{EABCH}	4.0		4.0		4.0		ns
t_{EABCL}	5.8		5.8		7.2		ns

Table 75. EPF10K50V Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		4.7		6.0		7.1		8.2	ns
t_{DIN2LE}		2.5		2.6		3.1		3.9	ns
$t_{DIN2DATA}$		4.4		5.9		6.8		7.7	ns
$t_{DCLK2IOE}$		2.5		3.9		4.7		5.5	ns
$t_{DCLK2LE}$		2.5		2.6		3.1		3.9	ns
$t_{SAMELAB}$		0.2		0.2		0.3		0.3	ns
$t_{SAMEROW}$		2.8		3.0		3.2		3.4	ns
$t_{SAMECOLUMN}$		3.0		3.2		3.4		3.6	ns
$t_{DIFFROW}$		5.8		6.2		6.6		7.0	ns
$t_{TWOROWS}$		8.6		9.2		9.8		10.4	ns
$t_{LEPERIPH}$		4.5		5.5		6.1		7.0	ns
$t_{LABCARRY}$		0.3		0.4		0.5		0.7	ns
$t_{LABCASC}$		0.0		1.3		1.6		2.0	ns

Table 76. EPF10K50V Device External Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{DRR}		11.2		14.0		17.2		21.1	ns
t_{INSU} *(2), (3)*	5.5		4.2		5.2		6.9		ns
t_{INH} *(3)*	0.0		0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	5.9	2.0	7.8	2.0	9.5	2.0	11.1	ns

Table 77. EPF10K50V Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.0		2.8		3.5		4.1		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	5.9	2.0	7.8	2.0	9.5	2.0	11.1	ns
$t_{XZBIDIR}$		8.0		9.8		11.8		14.3	ns
$t_{ZXBIDIR}$		8.0		9.8		11.8		14.3	ns

Table 79. EPF10K130V Device IOE Timing Microparameters *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{IOD}		1.3		1.6		2.0	ns
t_{IOC}		0.4		0.5		0.7	ns
t_{IOCO}		0.3		0.4		0.5	ns
t_{IOCOMB}		0.0		0.0		0.0	ns
t_{IOSU}	2.6		3.3		3.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.7		2.2		2.7	ns
t_{OD1}		3.5		4.4		5.0	ns
t_{OD2}		–		–		–	ns
t_{OD3}		8.2		8.1		9.7	ns
t_{XZ}		4.9		6.3		7.4	ns
t_{ZX1}		4.9		6.3		7.4	ns
t_{ZX2}		–		–		–	ns
t_{ZX3}		9.6		10.0		12.1	ns
t_{INREG}		7.9		10.0		12.6	ns
t_{IOFD}		6.2		7.9		9.9	ns
t_{INCOMB}		6.2		7.9		9.9	ns

Table 102. EPF10K100A Device EAB Internal Timing Macroparameters *Note (1)*							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		6.8		7.8		9.2	ns
$t_{EABRCCOMB}$	6.8		7.8		9.2		ns
$t_{EABRCREG}$	5.4		6.2		7.4		ns
t_{EABWP}	3.2		3.7		4.4		ns
$t_{EABWCCOMB}$	3.4		3.9		4.7		ns
$t_{EABWCREG}$	9.4		10.8		12.8		ns
t_{EABDD}		6.1		6.9		8.2	ns
$t_{EABDATACO}$		2.1		2.3		2.9	ns
$t_{EABDATASU}$	3.7		4.3		5.1		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	2.8		3.3		3.8		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	3.4		4.0		4.6		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	1.9		2.3		2.6		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		5.1		5.7		6.9	ns

Table 107. EPF10K250A Device IOE Timing Microparameters Note (1)							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		1.2		1.3		1.6	ns
t_{IOC}		0.4		0.4		0.5	ns
t_{IOCO}		0.8		0.9		1.1	ns
t_{IOCOMB}		0.7		0.7		0.8	ns
t_{IOSU}	2.7		3.1		3.6		ns
t_{IOH}	0.2		0.3		0.3		ns
t_{IOCLR}		1.2		1.3		1.6	ns
t_{OD1}		3.2		3.6		4.2	ns
t_{OD2}		5.9		6.7		7.8	ns
t_{OD3}		8.7		9.8		11.5	ns
t_{XZ}		3.8		4.3		5.0	ns
t_{ZX1}		3.8		4.3		5.0	ns
t_{ZX2}		6.5		7.4		8.6	ns
t_{ZX3}		9.3		10.5		12.3	ns
t_{INREG}		8.2		9.3		10.9	ns
t_{IOFD}		9.0		10.2		12.0	ns
t_{INCOMB}		9.0		10.2		12.0	ns