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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

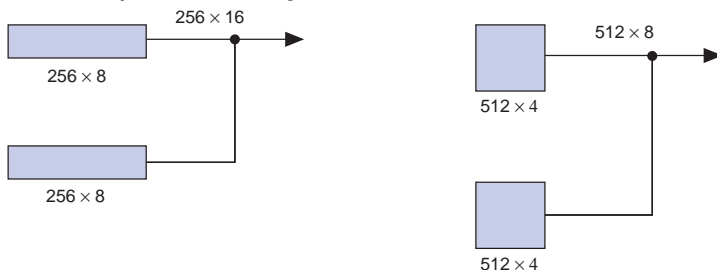
#### Details

Product Status	Obsolete
Number of LABs/CLBs	216
Number of Logic Elements/Cells	1728
Total RAM Bits	12288
Number of I/O	246
Number of Gates	69000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	356-LBGA
Supplier Device Package	356-BGA (35x35)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epf10k30bc356-3">https://www.e-xfl.com/product-detail/intel/epf10k30bc356-3</a>

- Flexible interconnect
  - FastTrack® Interconnect continuous routing structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Tri-state emulation that implements internal tri-state buses
  - Up to six global clock signals and four global clear signals
- Powerful I/O pins
  - Individual tri-state output enable control for each pin
  - Open-drain option on each I/O pin
  - Programmable output slew-rate control to reduce switching noise
  - FLEX 10KA devices support hot-socketing
- Peripheral register for fast setup and clock-to-output delay
- Flexible package options
  - Available in a variety of packages with 84 to 600 pins (see [Tables 4 and 5](#))
  - Pin-compatibility with other FLEX 10K devices in the same package
  - FineLine BGA™ packages maximize board space efficiency
- Software design support and automatic place-and-route provided by Altera development systems for Windows-based PCs and Sun SPARCstation, HP 9000 Series 700/800 workstations
- Additional design entry and simulation support provided by EDIF 2.0 and 3.0 netlist files, library of parameterized modules (LPM), DesignWare components, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, VeriBest, and Viewlogic

Larger blocks of RAM are created by combining multiple EABs. For example, two  $256 \times 8$  RAM blocks can be combined to form a  $256 \times 16$  RAM block; two  $512 \times 4$  blocks of RAM can be combined to form a  $512 \times 8$  RAM block. See [Figure 3](#).

**Figure 3. Examples of Combining EABs**



If necessary, all EABs in a device can be cascaded to form a single RAM block. EABs can be cascaded to form RAM blocks of up to 2,048 words without impacting timing. Altera's software automatically combines EABs to meet a designer's RAM specifications.

EABs provide flexible options for driving and controlling clock signals. Different clocks can be used for the EAB inputs and outputs. Registers can be independently inserted on the data input, EAB output, or the address and  $\overline{WE}$  inputs. The global signals and the EAB local interconnect can drive the  $\overline{WE}$  signal. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control the  $\overline{WE}$  signal or the EAB clock signals.

Each EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs. See [Figure 4](#).

### Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. Either the register or the LUT can be used to drive both the local interconnect and the FastTrack Interconnect at the same time.

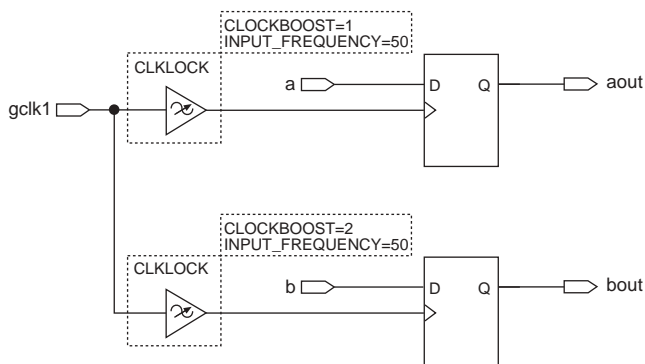
The LUT and the register in the LE can be used independently; this feature is known as register packing. To support register packing, the LE has two outputs; one drives the local interconnect and the other drives the FastTrack Interconnect. The DATA4 signal can drive the register directly, allowing the LUT to compute a function that is independent of the registered signal; a three-input function can be computed in the LUT, and a fourth independent signal can be registered. Alternatively, a four-input function can be generated, and one of the inputs to this function can be used to drive the register. The register in a packed LE can still use the clock enable, clear, and preset signals in the LE. In a packed LE, the register can drive the FastTrack Interconnect while the LUT drives the local interconnect, or vice versa.

### Arithmetic Mode

The arithmetic mode offers 2 three-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT computes a three-input function, and the other generates a carry output. As shown in [Figure 9](#) on page 19, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three signals: a, b, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

## I/O Element

An I/O element (IOE) contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. In some cases, using an LE register for an input register will result in a faster setup time than using an IOE register. IOEs can be used as input, output, or bidirectional pins. For bidirectional registered I/O implementation, the output register should be in the IOE and, the data input and output enable register should be LE registers placed adjacent to the bidirectional pin. The Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. [Figure 13](#) shows the bidirectional I/O registers.

**Figure 17. Enabling ClockLock & ClockBoost in the Same Design**

To use both the ClockLock and ClockBoost circuits in the same design, designers must use Revision C EPF10K100GC503-3DX devices and MAX+PLUS II software versions 7.2 or higher. The die revision is indicated by the third digit of the nine-digit code on the top side of the device.

## Output Configuration

This section discusses the peripheral component interconnect (PCI) pull-up clamping diode option, slew-rate control, open-drain output option, MultiVolt I/O interface, and power sequencing for FLEX 10K devices. The PCI pull-up clamping diode, slew-rate control, and open-drain output options are controlled pin-by-pin via Altera logic options. The MultiVolt I/O interface is controlled by connecting  $V_{CCIO}$  to a different voltage than  $V_{CCINT}$ . Its effect can be simulated in the Altera software via the **Global Project Device Options** dialog box (Assign menu).

### PCI Clamping Diodes

The EPF10K10A and EPF10K30A devices have a pull-up clamping diode on every I/O, dedicated input, and dedicated clock pin. PCI clamping diodes clamp the transient overshoot caused by reflected waves to the  $V_{CCIO}$  value and are required for 3.3-V PCI compliance. Clamping diodes can also be used to limit overshoot in other systems.

Clamping diodes are controlled on a pin-by-pin basis via a logic option in the Altera software. When  $V_{CCIO}$  is 3.3 V, a pin that has the clamping diode turned on can be driven by a 2.5-V or 3.3-V signal, but not a 5.0-V signal. When  $V_{CCIO}$  is 2.5 V, a pin that has the clamping diode turned on can be driven by a 2.5-V signal, but not a 3.3-V or 5.0-V signal. However, a clamping diode can be turned on for a subset of pins, which allows devices to bridge between a 3.3-V PCI bus and a 5.0-V device.

**Table 13. FLEX 10K JTAG Instructions**

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.
USERCODE	Selects the user electronic signature (USERCODE) register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	These instructions are used when configuring a FLEX 10K device via JTAG ports with a BitBlaster, or ByteBlasterMV or MasterBlaster download cable, or using a Jam File (.jam) or Jam Byte-Code File (.jbc) via an embedded processor.

The instruction register length of FLEX 10K devices is 10 bits. The USERCODE register length in FLEX 10K devices is 32 bits; 7 bits are determined by the user, and 25 bits are predetermined. [Tables 14 and 15](#) show the boundary-scan register length and device IDCODE information for FLEX 10K devices.

**Table 14. FLEX 10K Boundary-Scan Register Length**

Device	Boundary-Scan Register Length
EPF10K10, EPF10K10A	480
EPF10K20	624
EPF10K30, EPF10K30A	768
EPF10K40	864
EPF10K50, EPF10K50V	960
EPF10K70	1,104
EPF10K100, EPF10K100A	1,248
EPF10K130V	1,440
EPF10K250A	1,440

**Table 15. 32-Bit FLEX 10K Device IDCODE** *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)
EPF10K10, EPF10K10A	0000	0001 0000 0001 0000	00001101110	1
EPF10K20	0000	0001 0000 0010 0000	00001101110	1
EPF10K30, EPF10K30A	0000	0001 0000 0011 0000	00001101110	1
EPF10K40	0000	0001 0000 0100 0000	00001101110	1
EPF10K50, EPF10K50V	0000	0001 0000 0101 0000	00001101110	1
EPF10K70	0000	0001 0000 0111 0000	00001101110	1
EPF10K100, EPF10K100A	0000	0000 0001 0000 0000	00001101110	1
EPF10K130V	0000	0000 0001 0011 0000	00001101110	1
EPF10K250A	0000	0000 0010 0101 0000	00001101110	1

**Notes:**

- (1) The most significant bit (MSB) is on the left.  
 (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

FLEX 10K devices include weak pull-ups on JTAG pins.



For more information, see the following documents:

- *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Jam Programming & Test Language Specification*



Tables 22 through 25 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for EPF10K50V and EPF10K130V devices.

**Table 22. EPF10K50V & EPF10K130V Device Absolute Maximum Ratings** *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	Supply voltage	With respect to ground (2)	−0.5	4.6	V
$V_I$	DC input voltage		−2.0	5.75	V
$I_{OUT}$	DC output current, per pin		−25	25	mA
$T_{STG}$	Storage temperature	No bias	−65	150	° C
$T_{AMB}$	Ambient temperature	Under bias	−65	135	° C
$T_J$	Junction temperature	Ceramic packages, under bias		150	° C
		RQFP and BGA packages, under bias		135	° C

**Table 23. EPF10K50V & EPF10K130V Device Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage for internal logic and input buffers	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
$V_{CCIO}$	Supply voltage for output buffers	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
$V_I$	Input voltage	(5)	−0.5	5.75	V
$V_O$	Output voltage		0	$V_{CCIO}$	V
$T_A$	Ambient temperature	For commercial use	0	70	° C
		For industrial use	−40	85	° C
$T_J$	Operating temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
$t_R$	Input rise time			40	ns
$t_F$	Input fall time			40	ns

**Table 35. EAB Timing Macroparameters** *Notes (1), (6)*

Symbol	Parameter	Conditions
$t_{EABAA}$	EAB address access delay	
$t_{EABRCCOMB}$	EAB asynchronous read cycle time	
$t_{EABRCREG}$	EAB synchronous read cycle time	
$t_{EABWP}$	EAB write pulse width	
$t_{EABWCCOMB}$	EAB asynchronous write cycle time	
$t_{EABWCREG}$	EAB synchronous write cycle time	
$t_{EABDD}$	EAB data-in to data-out valid delay	
$t_{EABDATACO}$	EAB clock-to-output delay when using output registers	
$t_{EABDATASU}$	EAB data/address setup time before clock when using input register	
$t_{EABDATAH}$	EAB data/address hold time after clock when using input register	
$t_{EABWESU}$	EAB $\overline{WE}$ setup time before clock when using input register	
$t_{EABWEH}$	EAB $\overline{WE}$ hold time after clock when using input register	
$t_{EABWDSU}$	EAB data setup time before falling edge of write pulse when not using input registers	
$t_{EABWDH}$	EAB data hold time after falling edge of write pulse when not using input registers	
$t_{EABWASU}$	EAB address setup time before rising edge of write pulse when not using input registers	
$t_{EABWAH}$	EAB address hold time after falling edge of write pulse when not using input registers	
$t_{EABWO}$	EAB write enable to data output valid delay	

**Table 36. Interconnect Timing Microparameters** *Note (1)*

Symbol	Parameter	Conditions
$t_{DIN2IOE}$	Delay from dedicated input pin to IOE control input	(7)
$t_{DCLK2LE}$	Delay from dedicated clock pin to LE or EAB clock	(7)
$t_{DIN2DATA}$	Delay from dedicated input or clock to LE or EAB data	(7)
$t_{DCLK2IOE}$	Delay from dedicated clock pin to IOE clock	(7)
$t_{DIN2LE}$	Delay from dedicated input pin to LE or EAB control input	(7)
$t_{SAMELAB}$	Routing delay for an LE driving another LE in the same LAB	
$t_{SAMEROW}$	Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row	(7)
$t_{SAMECOLUMN}$	Routing delay for an LE driving an IOE in the same column	(7)
$t_{DIFFROW}$	Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row	(7)
$t_{TROWROWS}$	Routing delay for a row IOE or EAB driving an LE or EAB in a different row	(7)
$t_{LEPERIPH}$	Routing delay for an LE driving a control signal of an IOE via the peripheral control bus	(7)
$t_{LABCARRY}$	Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	

**Table 37. External Timing Parameters** *Notes (8), (10)*

Symbol	Parameter	Conditions
$t_{DRR}$	Register-to-register delay via four LEs, three row interconnects, and four local interconnects	(9)
$t_{INSU}$	Setup time with global clock at IOE register	
$t_{INH}$	Hold time with global clock at IOE register	
$t_{OUTCO}$	Clock-to-output delay with global clock at IOE register	

**Table 38. External Bidirectional Timing Parameters** *Note (10)*

Symbol	Parameter	Condition
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at adjacent LE register	
$t_{INHBDIR}$	Hold time for bidirectional pins with global clock at adjacent LE register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	
$t_{XZBIDIR}$	Synchronous IOE output buffer disable delay	
$t_{ZXBIDIR}$	Synchronous IOE output buffer enable delay, slow slew rate = off	

**Table 59. EPF10K70 Device EAB Internal Microparameters** *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.3		1.5		1.9	ns
$t_{EABDATA2}$		4.3		4.8		6.0	ns
$t_{EABWE1}$		0.9		1.0		1.2	ns
$t_{EABWE2}$		4.5		5.0		6.2	ns
$t_{EABCLK}$		0.9		1.0		2.2	ns
$t_{EABCO}$		0.4		0.5		0.6	ns
$t_{EABYPASS}$		1.3		1.5		1.9	ns
$t_{EABSU}$	1.3		1.5		1.8		ns
$t_{EABH}$	1.8		2.0		2.5		ns
$t_{AA}$		7.8		8.7		10.7	ns
$t_{WP}$	5.2		5.8		7.2		ns
$t_{WDSU}$	1.4		1.6		2.0		ns
$t_{WDH}$	0.3		0.3		0.4		ns
$t_{WASU}$	0.4		0.5		0.6		ns
$t_{WAH}$	0.9		1.0		1.2		ns
$t_{WO}$		4.5		5.0		6.2	ns
$t_{DD}$		4.5		5.0		6.2	ns
$t_{EABOUT}$		0.4		0.5		0.6	ns
$t_{EABCH}$	4.0		4.0		4.0		ns
$t_{EABCL}$	5.2		5.8		7.2		ns

**Table 68. EPF10K100 Device Interconnect Timing Microparameters** *Note (1)*

Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		10.3		10.3		12.2	ns
$t_{DIN2LE}$		4.8		4.8		6.0	ns
$t_{DIN2DATA}$		7.3		7.3		11.0	ns
$t_{DCLK2IOE}$ without ClockLock or ClockBoost circuitry		6.2		6.2		7.7	ns
$t_{DCLK2IOE}$ with ClockLock or ClockBoost circuitry		2.3		–		–	ns
$t_{DCLK2LE}$ without ClockLock or ClockBoost circuitry		4.8		4.8		6.0	ns
$t_{DCLK2LE}$ with ClockLock or ClockBoost circuitry		2.3		–		–	ns
$t_{SAMELAB}$		0.4		0.4		0.5	ns
$t_{SAMEROW}$		4.9		4.9		5.5	ns
$t_{SAMECOLUMN}$		5.1		5.1		5.4	ns
$t_{DIFFROW}$		10.0		10.0		10.9	ns
$t_{TWOROWS}$		14.9		14.9		16.4	ns
$t_{LEPERIPH}$		6.9		6.9		8.1	ns
$t_{LABCARRY}$		0.9		0.9		1.1	ns
$t_{LABCASC}$		3.0		3.0		3.2	ns

**Table 69. EPF10K100 Device External Timing Parameters** *Note (1)*

Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{DDR}}$		19.1		19.1		24.2	ns
$t_{\text{INSU}}$ (2), (3), (4)	7.8		7.8		8.5		ns
$t_{\text{OUTCO}}$ (3), (4)	2.0	11.1	2.0	11.1	2.0	14.3	ns
$t_{\text{INH}}$ (3)	0.0		0.0		0.0		ns
$t_{\text{INSU}}$ (2), (3), (5)	6.2		–		–		ns
$t_{\text{OUTCO}}$ (3), (5)	2.0	6.7		–		–	ns

**Table 70. EPF10K100 Device External Bidirectional Timing Parameters** *Note (1)*

Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$ (4)	8.1		8.1		10.4		ns
$t_{\text{INHBIDIR}}$ (4)	0.0		0.0		0.0		ns
$t_{\text{OUTCOBIDIR}}$ (4)	2.0	11.1	2.0	11.1	2.0	14.3	ns
$t_{\text{XZBIDIR}}$ (4)		15.3		15.3		18.4	ns
$t_{\text{ZXBIDIR}}$ (4)		15.3		15.3		18.4	ns
$t_{\text{INSUBIDIR}}$ (5)	9.1		–		–		ns
$t_{\text{INHBIDIR}}$ (5)	0.0		–		–		ns
$t_{\text{OUTCOBIDIR}}$ (5)	2.0	7.2	–	–	–	–	ns
$t_{\text{XZBIDIR}}$ (5)		14.3		–		–	ns
$t_{\text{ZXBIDIR}}$ (5)		14.3		–		–	ns

**Notes to tables:**

- (1) All timing parameters are described in Tables 32 through 38 in this data sheet.
- (2) Using an LE to register the signal may provide a lower setup time.
- (3) This parameter is specified by characterization.
- (4) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
- (5) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

**Table 88. EPF10K10A Device EAB Internal Timing Macroparameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABAA}$		8.1		9.8		13.1	ns
$t_{EABRCCOMB}$	8.1		9.8		13.1		ns
$t_{EABRCREG}$	5.8		6.9		9.3		ns
$t_{EABWP}$	2.0		2.4		3.2		ns
$t_{EABWCCOMB}$	3.5		4.2		5.6		ns
$t_{EABWCREG}$	9.4		11.2		14.8		ns
$t_{EABDD}$		6.9		8.3		11.0	ns
$t_{EABDATA CO}$		1.3		1.5		2.0	ns
$t_{EABDATASU}$	2.4		3.0		3.9		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	4.1		4.9		6.5		ns
$t_{EABWEH}$	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.4		1.6		2.2		ns
$t_{EABWDH}$	0.0		0.0		0.0		ns
$t_{EABWASU}$	2.5		3.0		4.1		ns
$t_{EABWAH}$	0.0		0.0		0.0		ns
$t_{EABWO}$		6.2		7.5		9.9	ns

**Table 89. EPF10K10A Device Interconnect Timing Microparameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		4.2		5.0		6.5	ns
$t_{DIN2LE}$		2.2		2.6		3.4	ns
$t_{DIN2DATA}$		4.3		5.2		7.1	ns
$t_{DCLK2IOE}$		4.2		4.9		6.6	ns
$t_{DCLK2LE}$		2.2		2.6		3.4	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		2.2		2.4		2.9	ns
$t_{SAMECOLUMN}$		0.8		1.0		1.4	ns
$t_{DIFFROW}$		3.0		3.4		4.3	ns
$t_{TWOROWS}$		5.2		5.8		7.2	ns
$t_{LEPERIPH}$		1.8		2.2		2.8	ns
$t_{LABCARRY}$		0.5		0.5		0.7	ns
$t_{LABCASC}$		0.9		1.0		1.5	ns

**Table 90. EPF10K10A External Reference Timing Parameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DRR}$		10.0		12.0		16.0	ns
$t_{INSU}$ (2), (3)	1.6		2.1		2.8		ns
$t_{INH}$ (3)	0.0		0.0		0.0		ns
$t_{OUTCO}$ (3)	2.0	5.8	2.0	6.9	2.0	9.2	ns

**Table 91. EPF10K10A Device External Bidirectional Timing Parameters** *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.4		3.3		4.5		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	5.8	2.0	6.9	2.0	9.2	ns
$t_{XZBIDIR}$		6.3		7.5		9.9	ns
$t_{ZXBIDIR}$		6.3		7.5		9.9	ns



**Table 94. EPF10K30A Device EAB Internal Microparameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		5.5		6.5		8.5	ns
$t_{EABDATA2}$		1.1		1.3		1.8	ns
$t_{EABWE1}$		2.4		2.8		3.7	ns
$t_{EABWE2}$		2.1		2.5		3.2	ns
$t_{EABCLK}$		0.0		0.0		0.2	ns
$t_{EABCO}$		1.7		2.0		2.6	ns
$t_{EABYPASS}$		0.0		0.0		0.3	ns
$t_{EABSU}$	1.2		1.4		1.9		ns
$t_{EABH}$	0.1		0.1		0.3		ns
$t_{AA}$		4.2		5.0		6.5	ns
$t_{WP}$	3.8		4.5		5.9		ns
$t_{WDSU}$	0.1		0.1		0.2		ns
$t_{WDH}$	0.1		0.1		0.2		ns
$t_{WASU}$	0.1		0.1		0.2		ns
$t_{WAH}$	0.1		0.1		0.2		ns
$t_{WO}$		3.7		4.4		6.4	ns
$t_{DD}$		3.7		4.4		6.4	ns
$t_{EABOUT}$		0.0		0.1		0.6	ns
$t_{EABCH}$	3.0		3.5		4.0		ns
$t_{EABCL}$	3.8		4.5		5.9		ns

**Table 96. EPF10K30A Device Interconnect Timing Microparameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		3.9		4.4		5.1	ns
$t_{DIN2LE}$		1.2		1.5		1.9	ns
$t_{DIN2DATA}$		3.2		3.6		4.5	ns
$t_{DCLK2IOE}$		3.0		3.5		4.6	ns
$t_{DCLK2LE}$		1.2		1.5		1.9	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		2.3		2.4		2.7	ns
$t_{SAMECOLUMN}$		1.3		1.4		1.9	ns
$t_{DIFFROW}$		3.6		3.8		4.6	ns
$t_{TWOROWS}$		5.9		6.2		7.3	ns
$t_{LEPERIPH}$		3.5		3.8		4.1	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.9		1.1		1.4	ns

**Table 97. EPF10K30A External Reference Timing Parameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DRR}$		11.0		13.0		17.0	ns
$t_{INSU}$ (2), (3)	2.5		3.1		3.9		ns
$t_{INH}$ (3)	0.0		0.0		0.0		ns
$t_{OUTCO}$ (3)	2.0	5.4	2.0	6.2	2.0	8.3	ns

**Table 98. EPF10K30A Device External Bidirectional Timing Parameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	4.2		4.9		6.8		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	5.4	2.0	6.2	2.0	8.3	ns
$t_{XZBIDIR}$		6.2		7.5		9.8	ns
$t_{ZXBIDIR}$		6.2		7.5		9.8	ns

**Table 113. ClockLock & ClockBoost Parameters (Part 2 of 2)**

Symbol	Parameter	Min	Typ	Max	Unit
$f_{CLKDEV1}$	Input deviation from user specification in MAX+PLUS II (ClockBoost clock multiplication factor equals 1) (1)			±1	MHz
$f_{CLKDEV2}$	Input deviation from user specification in MAX+PLUS II (ClockBoost clock multiplication factor equals 2) (1)			±0.5	MHz
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)			100	ps
$t_{LOCK}$	Time required for ClockLock or ClockBoost to acquire lock (2)			10	μs
$t_{JITTER}$	Jitter on ClockLock or ClockBoost-generated clock (3)			1	ns
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock	40	50	60	%

**Notes:**

- (1) To implement the ClockLock and ClockBoost circuitry with the MAX+PLUS II software, designers must specify the input frequency. The MAX+PLUS II software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The  $f_{CLKDEV}$  parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.
- (2) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the  $t_{LOCK}$  value is less than the time required for configuration.
- (3) The  $t_{JITTER}$  specification is measured under long-term observation.

## Power Consumption

The supply power (P) for FLEX 10K devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

Typical  $I_{CCSTANDBY}$  values are shown as  $I_{CC0}$  in the FLEX 10K device DC operating conditions tables on pages 46, 49, and 52 of this data sheet. The  $I_{CCACTIVE}$  value depends on the switching frequency and the application logic. This value is calculated based on the amount of current that each LE typically consumes. The  $P_{IO}$  value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.



Compared to the rest of the device, the embedded array consumes a negligible amount of power. Therefore, the embedded array can be ignored when calculating supply current.

The  $I_{CCACTIVE}$  value is calculated with the following equation:

$$I_{CCACTIVE} = K \times f_{MAX} \times N \times \text{tog}_{LC} \times \frac{\mu A}{\text{MHz} \times LE}$$

The parameters in this equation are shown below:

SRAM configuration elements allow FLEX 10K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation.

The entire reconfiguration process may be completed in less than 320 ms using an EPF10K250A device with a DCLK frequency of 10 MHz. This process can be used to reconfigure an entire system dynamically. In-field upgrades can be performed by distributing new configuration files.



Refer to the configuration device data sheet to obtain the POR delay when using a configuration device method.

## Programming Files

Despite being function- and pin-compatible, FLEX 10KA and FLEX 10KE devices are not programming- or configuration-file compatible with FLEX 10K devices. A design should be recompiled before it is transferred from a FLEX 10K device to an equivalent FLEX 10KA or FLEX 10KE device. This recompilation should be performed to create a new programming or configuration file and to check design timing on the faster FLEX 10KA or FLEX 10KE device. The programming or configuration files for EPF10K50 devices can program or configure an EPF10K50V device. However, Altera recommends recompiling a design for the EPF10K50V device when transferring it from the EPF10K50 device.

## Configuration Schemes

The configuration data for a FLEX 10K device can be loaded with one of five configuration schemes (see [Table 116](#)), chosen on the basis of the target application. An EPC1, EPC2, EPC16, or EPC1441 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of a FLEX 10K device, allowing automatic configuration on system power-up.



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