



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	216
Number of Logic Elements/Cells	1728
Total RAM Bits	12288
Number of I/O	189
Number of Gates	69000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-RQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k30rc240-3

Notes to tables:

- (1) FLEX 10K and FLEX 10KA device package types include plastic J-lead chip carrier (PLCC), thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), ball-grid array (BGA), pin-grid array (PGA), and FineLine BGA™ packages.
- (2) This option is supported with a 256-pin FineLine BGA package. By using SameFrame pin migration, all FineLine BGA packages are pin compatible. For example, a board can be designed to support both 256-pin and 484-pin FineLine BGA packages. The Altera software automatically avoids conflicting pins when future migration is set.

General Description

Altera's FLEX 10K devices are the industry's first embedded PLDs. Based on reconfigurable CMOS SRAM elements, the Flexible Logic Element MatriX (FLEX) architecture incorporates all features necessary to implement common gate array megafunctions. With up to 250,000 gates, the FLEX 10K family provides the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device.

FLEX 10K devices are reconfigurable, which allows 100% testing prior to shipment. As a result, the designer is not required to generate test vectors for fault coverage purposes. Additionally, the designer does not need to manage inventories of different ASIC designs; FLEX 10K devices can be configured on the board for the specific functionality required.

Table 6 shows FLEX 10K performance for some common designs. All performance values were obtained with Synopsys DesignWare or LPM functions. No special design technique was required to implement the applications; the designer simply inferred or instantiated a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

Table 6. FLEX 10K & FLEX 10KA Performance

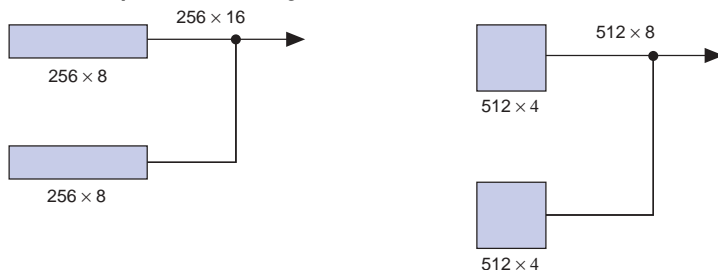
Application	Resources Used		Performance				Units
	LEs	EABs	-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	-4 Speed Grade	
16-bit loadable counter (1)	16	0	204	166	125	95	MHz
16-bit accumulator (1)	16	0	204	166	125	95	MHz
16-to-1 multiplexer (2)	10	0	4.2	5.8	6.0	7.0	ns
256 × 8 RAM read cycle speed (3)	0	1	172	145	108	84	MHz
256 × 8 RAM write cycle speed (3)	0	1	106	89	68	63	MHz

Notes:

- (1) The speed grade of this application is limited because of clock high and low specifications.
- (2) This application uses combinatorial inputs and outputs.
- (3) This application uses registered inputs and outputs.

Larger blocks of RAM are created by combining multiple EABs. For example, two 256×8 RAM blocks can be combined to form a 256×16 RAM block; two 512×4 blocks of RAM can be combined to form a 512×8 RAM block. See [Figure 3](#).

Figure 3. Examples of Combining EABs



If necessary, all EABs in a device can be cascaded to form a single RAM block. EABs can be cascaded to form RAM blocks of up to 2,048 words without impacting timing. Altera's software automatically combines EABs to meet a designer's RAM specifications.

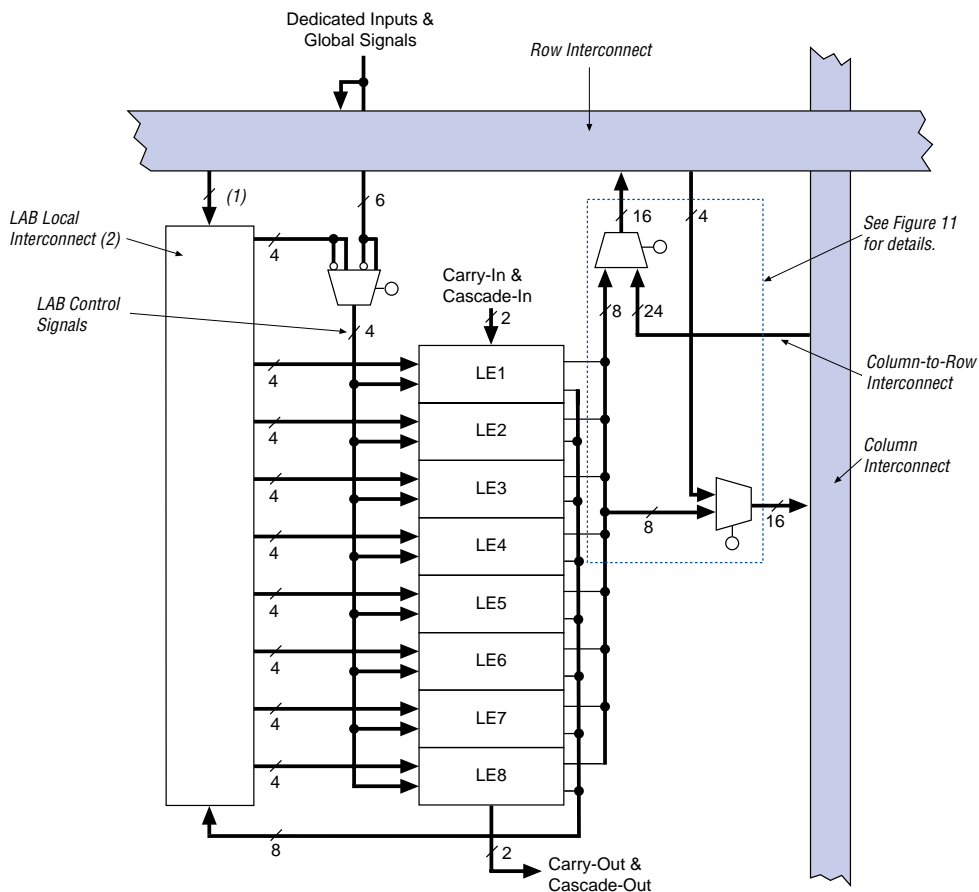
EABs provide flexible options for driving and controlling clock signals. Different clocks can be used for the EAB inputs and outputs. Registers can be independently inserted on the data input, EAB output, or the address and \overline{WE} inputs. The global signals and the EAB local interconnect can drive the \overline{WE} signal. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control the \overline{WE} signal or the EAB clock signals.

Each EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs. See [Figure 4](#).

Logic Array Block

Each LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the FLEX 10K architecture, facilitating efficient routing with optimum device utilization and high performance. See [Figure 5](#).

Figure 5. FLEX 10K LAB

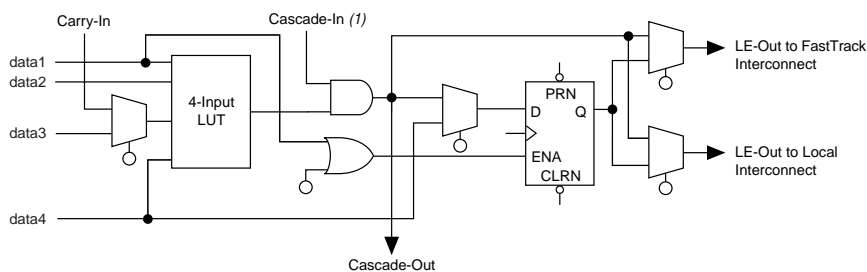


Notes:

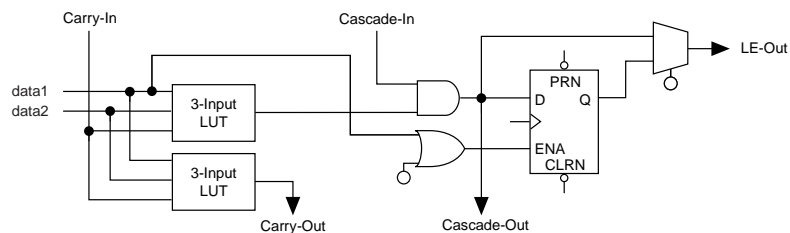
- (1) EPF10K10, EPF10K10A, EPF10K20, EPF10K30, EPF10K30A, EPF10K40, EPF10K50, and EPF10K50V devices have 22 inputs to the LAB local interconnect channel from the row; EPF10K70, EPF10K100, EPF10K100A, EPF10K130V, and EPF10K250A devices have 26.
- (2) EPF10K10, EPF10K10A, EPF10K20, EPF10K30, EPF10K30A, EPF10K40, EPF10K50, and EPF10K50V devices have 30 LAB local interconnect channels; EPF10K70, EPF10K100, EPF10K100A, EPF10K130V, and EPF10K250A devices have 34 LABs.

Figure 9. FLEX 10K LE Operating Modes

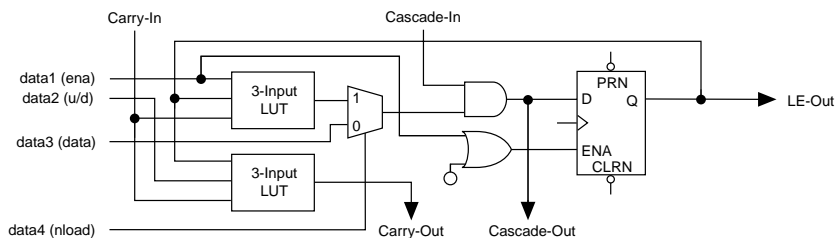
Normal Mode



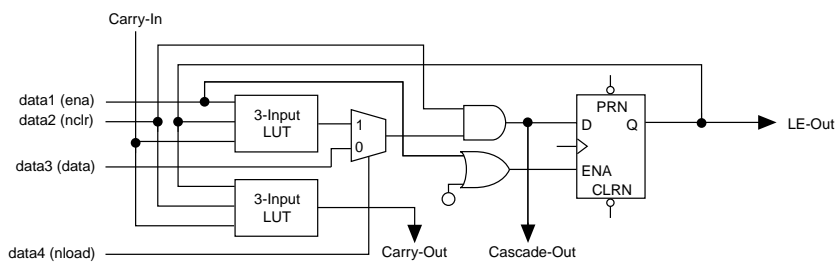
Arithmetic Mode



Up/Down Counter Mode



Clearable Counter Mode



Note:

(1) Packed registers cannot be used with the cascade chain.

Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. Either the register or the LUT can be used to drive both the local interconnect and the FastTrack Interconnect at the same time.

The LUT and the register in the LE can be used independently; this feature is known as register packing. To support register packing, the LE has two outputs; one drives the local interconnect and the other drives the FastTrack Interconnect. The DATA4 signal can drive the register directly, allowing the LUT to compute a function that is independent of the registered signal; a three-input function can be computed in the LUT, and a fourth independent signal can be registered. Alternatively, a four-input function can be generated, and one of the inputs to this function can be used to drive the register. The register in a packed LE can still use the clock enable, clear, and preset signals in the LE. In a packed LE, the register can drive the FastTrack Interconnect while the LUT drives the local interconnect, or vice versa.

Arithmetic Mode

The arithmetic mode offers 2 three-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT computes a three-input function, and the other generates a carry output. As shown in [Figure 9](#) on page 19, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three signals: a, b, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

Asynchronous Preset

An asynchronous preset is implemented as either an asynchronous load, or with an asynchronous clear. If DATA3 is tied to V_{CC} , asserting LABCTRL1 asynchronously loads a one into the register. Alternatively, the Altera software can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

Asynchronous Preset & Clear

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. DATA3 is tied to V_{CC} , therefore, asserting LABCTRL1 asynchronously loads a one into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

Asynchronous Load with Clear

When implementing an asynchronous load in conjunction with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear; LABCTRL2 does not have to feed the preset circuits.

Asynchronous Load with Preset

When implementing an asynchronous load in conjunction with preset, the Altera software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 presets the register, while asserting LABCTRL1 loads the register. The Altera software inverts the signal that drives DATA3 to account for the inversion of the register's output.

Asynchronous Load without Preset or Clear

When implementing an asynchronous load without preset or clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

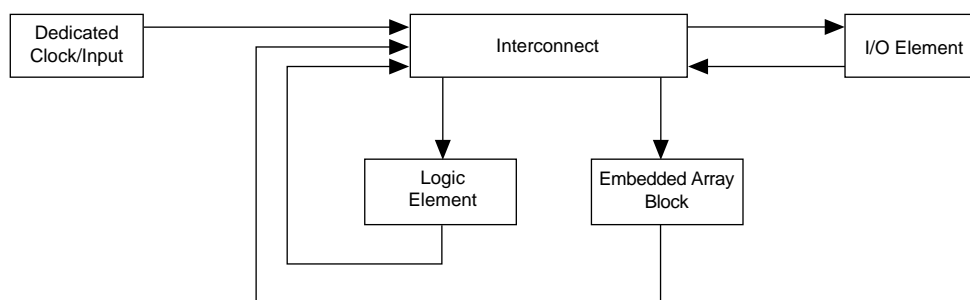
Table 28. FLEX 10KA 3.3-V Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		1.7 or $0.5 \times V_{CCINT}$, whichever is lower		5.75	V
V_{IL}	Low-level input voltage		-0.5		$0.3 \times V_{CCINT}$	V
V_{OH}	3.3-V high-level TTL output voltage	$I_{OH} = -11$ mA DC, $V_{CCIO} = 3.00$ V (8)	2.4			V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (8)	$V_{CCIO} - 0.2$			V
	3.3-V high-level PCI output voltage	$I_{OH} = -0.5$ mA DC, $V_{CCIO} = 3.00$ to 3.60 V (8)	$0.9 \times V_{CCIO}$			V
	2.5-V high-level output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 2.30$ V (8)	2.1			V
		$I_{OH} = -1$ mA DC, $V_{CCIO} = 2.30$ V (8)	2.0			V
		$I_{OH} = -2$ mA DC, $V_{CCIO} = 2.30$ V (8)	1.7			V
V_{OL}	3.3-V low-level TTL output voltage	$I_{OL} = 9$ mA DC, $V_{CCIO} = 3.00$ V (9)			0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.00$ V (9)			0.2	V
	3.3-V low-level PCI output voltage	$I_{OL} = 1.5$ mA DC, $V_{CCIO} = 3.00$ to 3.60 V (9)			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 2.30$ V (9)			0.2	V
		$I_{OL} = 1$ mA DC, $V_{CCIO} = 2.30$ V (9)			0.4	V
		$I_{OL} = 2$ mA DC, $V_{CCIO} = 2.30$ V (9)			0.7	V
I_I	Input pin leakage current	$V_I = 5.3$ V to -0.3 V (10)	-10		10	μ A
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = 5.3$ V to -0.3 V (10)	-10		10	μ A
I_{CC0}	V_{CC} supply current (standby)	$V_I =$ ground, no load		0.3	10	mA
		$V_I =$ ground, no load (11)		10		mA

Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Figure 24 shows the overall timing model, which maps the possible paths to and from the various elements of the FLEX 10K device.

Figure 24. FLEX 10K Device Timing Model



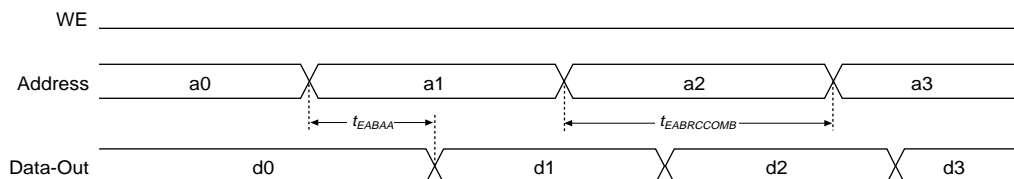
Notes to tables:

- (1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.
- (2) Operating conditions: $V_{CCIO} = 5.0 \text{ V} \pm 5\%$ for commercial use in FLEX 10K devices.
 $V_{CCIO} = 5.0 \text{ V} \pm 10\%$ for industrial use in FLEX 10K devices.
 $V_{CCIO} = 3.3 \text{ V} \pm 10\%$ for commercial or industrial use in FLEX 10KA devices.
- (3) Operating conditions: $V_{CCIO} = 3.3 \text{ V} \pm 10\%$ for commercial or industrial use in FLEX 10K devices.
 $V_{CCIO} = 2.5 \text{ V} \pm 0.2 \text{ V}$ for commercial or industrial use in FLEX 10KA devices.
- (4) Operating conditions: $V_{CCIO} = 2.5 \text{ V}, 3.3 \text{ V}, \text{ or } 5.0 \text{ V}$.
- (5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the \overline{WE} signal is registered.
- (6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.
- (7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
- (8) External reference timing parameters are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.
- (9) Contact Altera Applications for test circuit specifications and test conditions.
- (10) These timing parameters are sample-tested only.

Figures 29 and 30 show the asynchronous and synchronous timing waveforms, respectively, for the EAB macroparameters in Table 34.

Figure 29. EAB Asynchronous Timing Waveforms

EAB Asynchronous Read



EAB Asynchronous Write

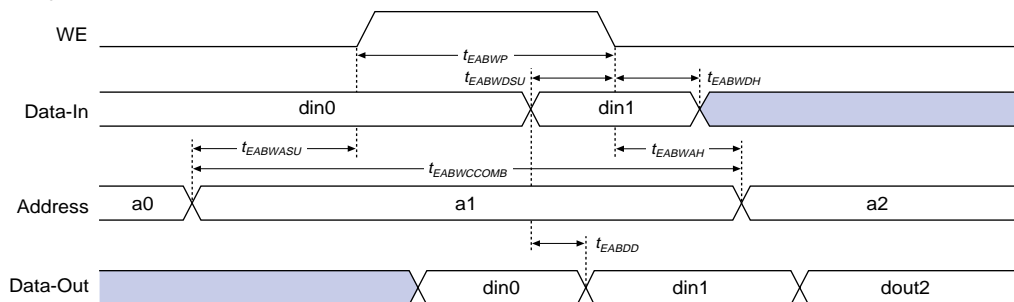


Table 42. EPF10K10 & EPF10K20 Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{EABAA}		13.7		17.0	ns
$t_{EABRCCOMB}$	13.7		17.0		ns
$t_{EABRCREG}$	9.7		11.9		ns
t_{EABWP}	5.8		7.2		ns
$t_{EABWCCOMB}$	7.3		9.0		ns
$t_{EABWCREG}$	13.0		16.0		ns
t_{EABDD}		10.0		12.5	ns
$t_{EABDATACO}$		2.0		3.4	ns
$t_{EABDATASU}$	5.3		5.6		ns
$t_{EABDATAH}$	0.0		0.0		ns
$t_{EABWESU}$	5.5		5.8		ns
t_{EABWEH}	0.0		0.0		ns
$t_{EABWDSU}$	5.5		5.8		ns
t_{EABWDH}	0.0		0.0		ns
$t_{EABWASU}$	2.1		2.7		ns
t_{EABWAH}	0.0		0.0		ns
t_{EABWO}		9.5		11.8	ns

Table 49. EPF10K30, EPF10K40 & EPF10K50 Device IOE Timing Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{IOD}		0.4		0.6	ns
t_{IOC}		0.5		0.9	ns
t_{IOCO}		0.4		0.5	ns
t_{IOCOMB}		0.0		0.0	ns
t_{IOSU}	3.1		3.5		ns
t_{IOH}	1.0		1.9		ns
t_{IOCLR}		1.0		1.2	ns
t_{OD1}		3.3		3.6	ns
t_{OD2}		5.6		6.5	ns
t_{OD3}		7.0		8.3	ns
t_{XZ}		5.2		5.5	ns
t_{ZX1}		5.2		5.5	ns
t_{ZX2}		7.5		8.4	ns
t_{ZX3}		8.9		10.2	ns
t_{INREG}		7.7		10.0	ns
t_{IOFD}		3.3		4.0	ns
t_{INCOMB}		3.3		4.0	ns

Notes to tables:

- (1) All timing parameters are described in Tables 32 through 38 in this data sheet.
- (2) Using an LE to register the signal may provide a lower setup time.
- (3) This parameter is specified by characterization.

Tables 57 through 63 show EPF10K70 device internal and external timing parameters.

Table 57. EPF10K70 Device LE Timing Microparameters *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		1.3		1.5		2.0	ns
t_{CLUT}		0.4		0.4		0.5	ns
t_{RLUT}		1.5		1.6		2.0	ns
t_{PACKED}		0.8		0.9		1.3	ns
t_{EN}		0.8		0.9		1.2	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		1.0		1.1		1.4	ns
t_{CGENR}		1.1		1.2		1.5	ns
t_{CASC}		1.0		1.1		1.3	ns
t_C		0.7		0.8		1.0	ns
t_{CO}		0.9		1.0		1.4	ns
t_{COMB}		0.4		0.5		0.7	ns
t_{SU}	1.9		2.1		2.6		ns
t_H	2.1		2.3		3.1		ns
t_{PRE}		0.9		1.0		1.4	ns
t_{CLR}		0.9		1.0		1.4	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns

Table 61. EPF10K70 Device Interconnect Timing Microparameters *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		6.6		7.3		8.8	ns
t_{DIN2LE}		4.2		4.8		6.0	ns
$t_{DIN2DATA}$		6.5		7.1		10.8	ns
$t_{DCLK2IOE}$		5.5		6.2		7.7	ns
$t_{DCLK2LE}$		4.2		4.8		6.0	ns
$t_{SAMELAB}$		0.4		0.4		0.5	ns
$t_{SAMEROW}$		4.8		4.9		5.5	ns
$t_{SAMECOLUMN}$		3.3		3.4		3.7	ns
$t_{DIFFROW}$		8.1		8.3		9.2	ns
$t_{TWOROWS}$		12.9		13.2		14.7	ns
$t_{LEPERIPH}$		5.5		5.7		6.5	ns
$t_{LABCARRY}$		0.8		0.9		1.1	ns
$t_{LABCASC}$		2.7		3.0		3.2	ns

Table 62. EPF10K70 Device External Timing Parameters *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		17.2		19.1		24.2	ns
t_{INSU} (2), (3)	6.6		7.3		8.0		ns
t_{INH} (3)	0.0		0.0		0.0		ns
t_{OUTCO} (3)	2.0	9.9	2.0	11.1	2.0	14.3	ns

Table 63. EPF10K70 Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	7.4		8.1		10.4		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	9.9	2.0	11.1	2.0	14.3	ns
$t_{XZBIDIR}$		13.7		15.4		18.5	ns
$t_{ZXBIDIR}$		13.7		15.4		18.5	ns

Notes to tables:

- (1) All timing parameters are described in Tables 32 through 38 in this data sheet.
- (2) Using an LE to register the signal may provide a lower setup time.
- (3) This parameter is specified by characterization.

Tables 64 through 70 show EPF10K100 device internal and external timing parameters.

Table 64. EPF10K100 Device LE Timing Microparameters <i>Note (1)</i>							
Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		1.5		1.5		2.0	ns
t_{CLUT}		0.4		0.4		0.5	ns
t_{RLUT}		1.6		1.6		2.0	ns
t_{PACKED}		0.9		0.9		1.3	ns
t_{EN}		0.9		0.9		1.2	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		1.1		1.1		1.4	ns
t_{CGENR}		1.2		1.2		1.5	ns
t_{CASC}		1.1		1.1		1.3	ns
t_C		0.8		0.8		1.0	ns
t_{CO}		1.0		1.0		1.4	ns
t_{COMB}		0.5		0.5		0.7	ns
t_{SU}	2.1		2.1		2.6		ns
t_H	2.3		2.3		3.1		ns
t_{PRE}		1.0		1.0		1.4	ns
t_{CLR}		1.0		1.0		1.4	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns

Table 80. EPF10K130V Device EAB Internal Microparameters *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.9		2.4		2.4	ns
$t_{EABDATA2}$		3.7		4.7		4.7	ns
t_{EABWE1}		1.9		2.4		2.4	ns
t_{EABWE2}		3.7		4.7		4.7	ns
t_{EABCLK}		0.7		0.9		0.9	ns
t_{EABCO}		0.5		0.6		0.6	ns
$t_{EABYPASS}$		0.6		0.8		0.8	ns
t_{EABSU}	1.4		1.8		1.8		ns
t_{EABH}	0.0		0.0		0.0		ns
t_{AA}		5.6		7.1		7.1	ns
t_{WP}	3.7		4.7		4.7		ns
t_{WDSU}	4.6		5.9		5.9		ns
t_{WDH}	0.0		0.0		0.0		ns
t_{WASU}	3.9		5.0		5.0		ns
t_{WAH}	0.0		0.0		0.0		ns
t_{WO}		5.6		7.1		7.1	ns
t_{DD}		5.6		7.1		7.1	ns
t_{EABOUT}		2.4		3.1		3.1	ns
t_{EABCH}	4.0		4.0		4.0		ns
t_{EABCL}	4.0		4.7		4.7		ns

Notes to tables:

- (1) All timing parameters are described in Tables 32 through 38 in this data sheet.
- (2) Using an LE to register the signal may provide a lower setup time.
- (3) This parameter is specified by characterization.

Tables 85 through 91 show EPF10K10A device internal and external timing parameters.

Table 85. EPF10K10A Device LE Timing Microparameters <i>Note (1)</i>							
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.9		1.2		1.6	ns
t_{CLUT}		1.2		1.4		1.9	ns
t_{RLUT}		1.9		2.3		3.0	ns
t_{PACKED}		0.6		0.7		0.9	ns
t_{EN}		0.5		0.6		0.8	ns
t_{CICO}		0.2		0.3		0.4	ns
t_{CGEN}		0.7		0.9		1.1	ns
t_{CGENR}		0.7		0.9		1.1	ns
t_{CASC}		1.0		1.2		1.7	ns
t_C		1.2		1.4		1.9	ns
t_{CO}		0.5		0.6		0.8	ns
t_{COMB}		0.5		0.6		0.8	ns
t_{SU}	1.1		1.3		1.7		ns
t_H	0.6		0.7		0.9		ns
t_{PRE}		0.5		0.6		0.9	ns
t_{CLR}		0.5		0.6		0.9	ns
t_{CH}	3.0		3.5		4.0		ns
t_{CL}	3.0		3.5		4.0		ns

Table 86. EPF10K10A Device IOE Timing Microparameters <i>Note (1) (Part 1 of 2)</i>							
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
		1.3		1.5		2.0	ns
t_{IOC}		0.2		0.3		0.3	ns
t_{IOCO}		0.2		0.3		0.4	ns
t_{IOCOMB}		0.6		0.7		0.9	ns
t_{IOSU}	0.8		1.0		1.3		ns

Table 101. EPF10K100A Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.8		2.1		2.4	ns
$t_{EABDATA2}$		3.2		3.7		4.4	ns
t_{EABWE1}		0.8		0.9		1.1	ns
t_{EABWE2}		2.3		2.7		3.1	ns
t_{EABCLK}		0.8		0.9		1.1	ns
t_{EABCO}		1.0		1.1		1.4	ns
$t_{EABYPASS}$		0.3		0.3		0.4	ns
t_{EABSU}	1.3		1.5		1.8		ns
t_{EABH}	0.4		0.5		0.5		ns
t_{AA}		4.1		4.8		5.6	ns
t_{WP}	3.2		3.7		4.4		ns
t_{WDSU}	2.4		2.8		3.3		ns
t_{WDH}	0.2		0.2		0.3		ns
t_{WASU}	0.2		0.2		0.3		ns
t_{WAH}	0.0		0.0		0.0		ns
t_{WO}		3.4		3.9		4.6	ns
t_{DD}		3.4		3.9		4.6	ns
t_{EABOUT}		0.3		0.3		0.4	ns
t_{EABCH}	2.5		3.5		4.0		ns
t_{EABCL}	3.2		3.7		4.4		ns

- f_{MAX} = Maximum operating frequency in MHz
 N = Total number of logic cells used in the device
 tog_{LC} = Average percent of logic cells toggling at each clock (typically 12.5%)
 K = Constant, shown in [Tables 114 and 115](#)

Table 114. FLEX 10K K Constant Values

Device	K Value
EPF10K10	82
EPF10K20	89
EPF10K30	88
EPF10K40	92
EPF10K50	95
EPF10K70	85
EPF10K100	88

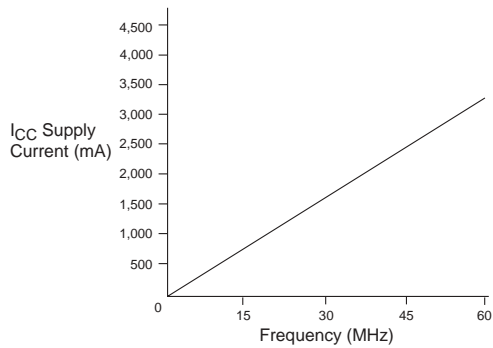
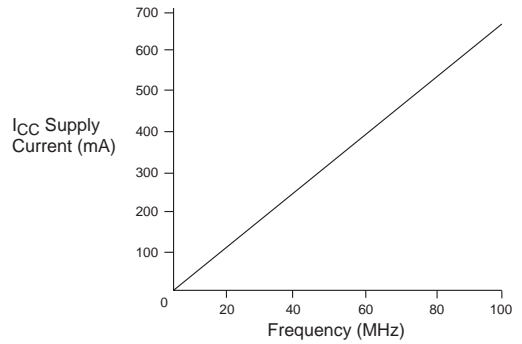
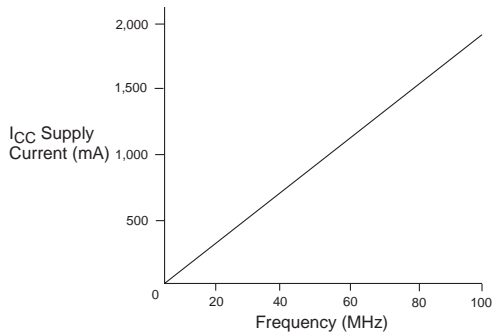
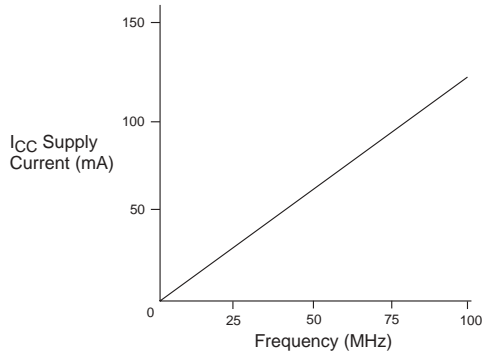
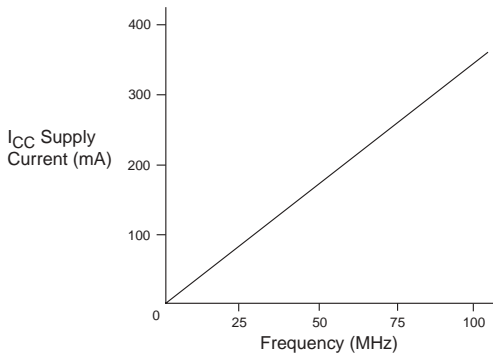
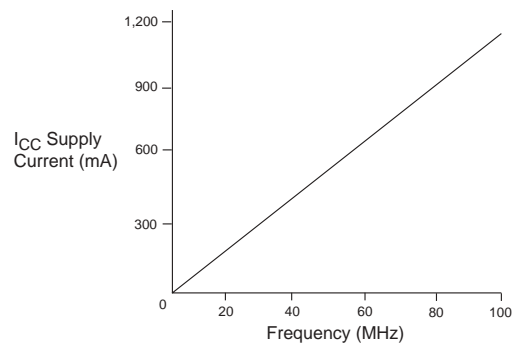
Table 115. FLEX 10KA K Constant Values

Device	K Value
EPF10K10A	17
EPF10K30A	17
EPF10K50V	19
EPF10K100A	19
EPF10K130V	22
EPF10K250A	23

This calculation provides an I_{CC} estimate based on typical conditions with no output load. The actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

To better reflect actual designs, the power model (and the constant K in the power calculation equations) for continuous interconnect FLEX devices assumes that logic cells drive FastTrack Interconnect channels. In contrast, the power model of segmented FPGAs assumes that all logic cells drive only one short interconnect segment. This assumption may lead to inaccurate results, compared to measured power consumption for an actual design in a segmented interconnect FPGA.

[Figure 32](#) shows the relationship between the current and operating frequency of FLEX 10K devices.

Figure 32. $I_{CCACTIVE}$ vs. Operating Frequency (Part 2 of 3)**EPF10K100****EPF10K50V****EPF10K130V****EPF10K10A****EPF10K30A****EPF10K100A**



Notes: