Intel - EPF10K30RC240-4N Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

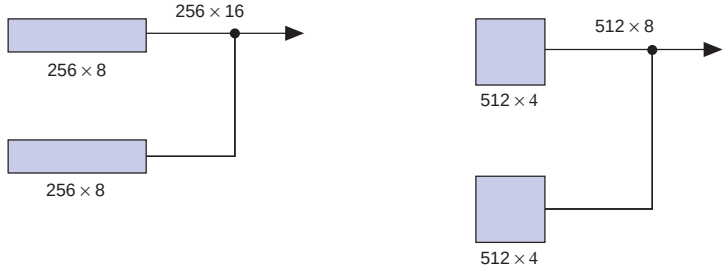
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	216
Number of Logic Elements/Cells	1728
Total RAM Bits	12288
Number of I/O	189
Number of Gates	69000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-RQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k30rc240-4n

Larger blocks of RAM are created by combining multiple EABs. For example, two 256 × 8 RAM blocks can be combined to form a 256 × 16 RAM block; two 512 × 4 blocks of RAM can be combined to form a 512 × 8 RAM block. See Figure 3.

Figure 3. Examples of Combining EABs

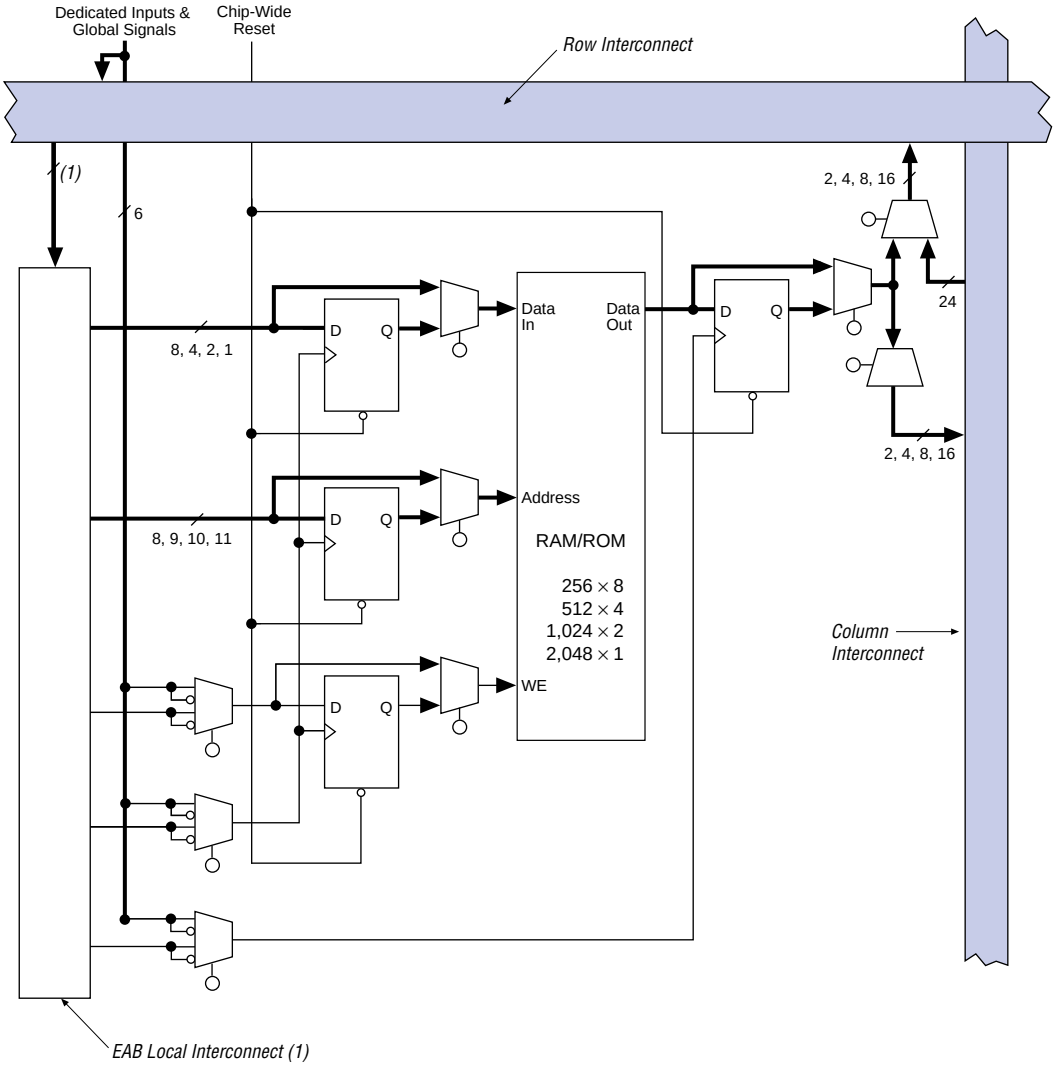


If necessary, all EABs in a device can be cascaded to form a single RAM block. EABs can be cascaded to form RAM blocks of up to 2,048 words without impacting timing. Altera's software automatically combines EABs to meet a designer's RAM specifications.

EABs provide flexible options for driving and controlling clock signals. Different clocks can be used for the EAB inputs and outputs. Registers can be independently inserted on the data input, EAB output, or the address and `WE` inputs. The global signals and the EAB local interconnect can drive the `WE` signal. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control the `WE` signal or the EAB clock signals.

Each EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs. See Figure 4.

Figure 4. FLEX 10K Embedded Array Block

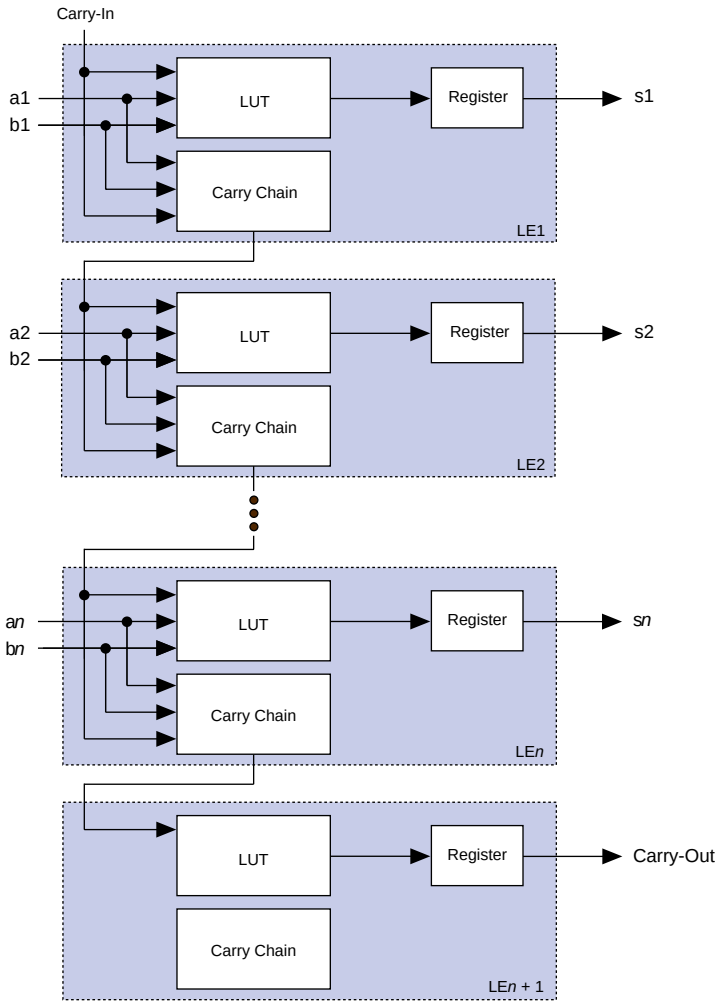


Note:

(1) EPF10K10, EPF10K10A, EPF10K20, EPF10K30, EPF10K30A, EPF10K40, EPF10K50, and EPF10K50V devices have 22 EAB local interconnect channels; EPF10K70, EPF10K100, EPF10K100A, EPF10K130V, and EPF10K250A devices have 26.

Figure 7 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can either be bypassed for simple adders or be used for an accumulator function. The carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal.

Figure 7. Carry Chain Operation (n-bit Full Adder)



Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across devices; it provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock enable or eight output enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by specific LEs. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, an LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal. The chip-wide reset signal will reset all IOE registers, overriding any other control signals.

Tables 8 and 9 list the sources for each peripheral control signal, and the rows that can drive global signals. These tables also show how the output enable, clock enable, clock, and clear signals share 12 peripheral control signals.

Signals on the peripheral control bus can also drive the four global signals, referred to as GLOBAL0 through GLOBAL3 in Tables 8 and 9. The internally generated signal can drive the global signal, providing the same low-skew, low-delay characteristics for an internally generated signal as for a signal driven by an input. This feature is ideal for internally generated clear or clock signals with high fan-out. When a global signal is driven by internal logic, the dedicated input pin that drives that global signal cannot be used. The dedicated input pin should be driven to a known logic state (such as ground) and not be allowed to float.

When the chip-wide output enable pin is held low, it will tri-state all pins on the device. This option can be set in the Global Project Device Options menu. Additionally, the registers in the IOE can be reset by holding the chip-wide reset pin low.

Row-to-IOE Connections

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Up to eight IOEs connect to each side of each row channel. See Figure 14.

Figure 14. FLEX 10K Row-to-IOE Connections

The values for m and n are provided in Table 10.

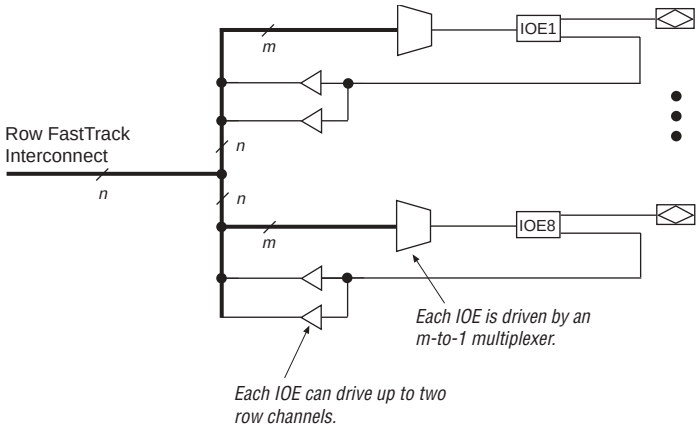


Table 15. 32-Bit FLEX 10K Device IDCODE *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) *(2)*
EPF10K10, EPF10K10A	0000	0001 0000 0001 0000	00001101110	1
EPF10K20	0000	0001 0000 0010 0000	00001101110	1
EPF10K30, EPF10K30A	0000	0001 0000 0011 0000	00001101110	1
EPF10K40	0000	0001 0000 0100 0000	00001101110	1
EPF10K50, EPF10K50V	0000	0001 0000 0101 0000	00001101110	1
EPF10K70	0000	0001 0000 0111 0000	00001101110	1
EPF10K100, EPF10K100A	0000	0000 0001 0000 0000	00001101110	1
EPF10K130V	0000	0000 0001 0011 0000	00001101110	1
EPF10K250A	0000	0000 0010 0101 0000	00001101110	1

Notes:
(1) The most significant bit (MSB) is on the left.
(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

FLEX 10K devices include weak pull-ups on JTAG pins.

For more information, see the following documents:

- *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Jam Programming & Test Language Specification*

Table 27. FLEX 10KA 3.3-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3)*, *(4)*	2.30 (2.30)	2.70 (2.70)	V
V_I	Input voltage	*(5)*	–0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 36. Interconnect Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
$t_{DIN2IOE}$	Delay from dedicated input pin to IOE control input	*(7)*
$t_{DCLK2LE}$	Delay from dedicated clock pin to LE or EAB clock	*(7)*
$t_{DIN2DATA}$	Delay from dedicated input or clock to LE or EAB data	*(7)*
$t_{DCLK2IOE}$	Delay from dedicated clock pin to IOE clock	*(7)*
t_{DIN2LE}	Delay from dedicated input pin to LE or EAB control input	*(7)*
$t_{SAMELAB}$	Routing delay for an LE driving another LE in the same LAB	
$t_{SAMEROW}$	Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row	*(7)*
$t_{SAMECOLUMN}$	Routing delay for an LE driving an IOE in the same column	*(7)*
$t_{DIFFROW}$	Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row	*(7)*
$t_{TWOROWS}$	Routing delay for a row IOE or EAB driving an LE or EAB in a different row	*(7)*
$t_{LEPERIPH}$	Routing delay for an LE driving a control signal of an IOE via the peripheral control bus	*(7)*
$t_{LABCARRY}$	Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	

Table 37. External Timing Parameters *Notes (8), (10)*

Symbol	Parameter	Conditions
t_{DRR}	Register-to-register delay via four LEs, three row interconnects, and four local interconnects	*(9)*
t_{INSU}	Setup time with global clock at IOE register	
t_{INH}	Hold time with global clock at IOE register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE register	

Table 38. External Bidirectional Timing Parameters *Note (10)*

Symbol	Parameter	Condition
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at adjacent LE register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at adjacent LE register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	
$t_{XZBIDIR}$	Synchronous IOE output buffer disable delay	
$t_{ZXBIDIR}$	Synchronous IOE output buffer enable delay, slow slew rate = off	

Table 45. EPF10K10 & EPF10K20 Device External Timing Parameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{DRR}		16.1		20.0	ns
t_{INSU} *(2)*, *(3)*	5.5		6.0		ns
t_{INH} *(3)*	0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	6.7	2.0	8.4	ns

Table 46. EPF10K10 Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{INSUBIDIR}$	4.5		5.6		ns
$t_{INHBIDIR}$	0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	6.7	2.0	8.4	ns
$t_{XZBIDIR}$		10.5		13.4	ns
$t_{ZXBIDIR}$		10.5		13.4	ns

Table 47. EPF10K20 Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{INSUBIDIR}$	4.6		5.7		ns
$t_{INHBIDIR}$	0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	6.7	2.0	8.4	ns
$t_{XZBIDIR}$		10.5		13.4	ns
$t_{ZXBIDIR}$		10.5		13.4	ns

Notes to tables:

(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Table 52. EPF10K30 Device Interconnect Timing Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{DIN2IOE}$		6.9		8.7	ns
t_{DIN2LE}		3.6		4.8	ns
$t_{DIN2DATA}$		5.5		7.2	ns
$t_{DCLK2IOE}$		4.6		6.2	ns
$t_{DCLK2LE}$		3.6		4.8	ns
$t_{SAMELAB}$		0.3		0.3	ns
$t_{SAMEROW}$		3.3		3.7	ns
$t_{SAMECOLUMN}$		2.5		2.7	ns
$t_{DIFFROW}$		5.8		6.4	ns
$t_{TWOROWS}$		9.1		10.1	ns
$t_{LEPERIPH}$		6.2		7.1	ns
$t_{LABCARRY}$		0.4		0.6	ns
$t_{LABCASC}$		2.4		3.0	ns

Table 53. EPF10K40 Device Interconnect Timing Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{DIN2IOE}$		7.6		9.4	ns
t_{DIN2LE}		3.6		4.8	ns
$t_{DIN2DATA}$		5.5		7.2	ns
$t_{DCLK2IOE}$		4.6		6.2	ns
$t_{DCLK2LE}$		3.6		4.8	ns
$t_{SAMELAB}$		0.3		0.3	ns
$t_{SAMEROW}$		3.3		3.7	ns
$t_{SAMECOLUMN}$		3.1		3.2	ns
$t_{DIFFROW}$		6.4		6.4	ns
$t_{TWOROWS}$		9.7		10.6	ns
$t_{LEPERIPH}$		6.4		7.1	ns
$t_{LABCARRY}$		0.4		0.6	ns
$t_{LABCASC}$		2.4		3.0	ns

Notes to tables:
(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Tables 64 through 70 show EPF10K100 device internal and external timing parameters.

Table 64. EPF10K100 Device LE Timing Microparameters *Note (1)*

Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		1.5		1.5		2.0	ns
t_{CLUT}		0.4		0.4		0.5	ns
t_{RLUT}		1.6		1.6		2.0	ns
t_{PACKED}		0.9		0.9		1.3	ns
t_{EN}		0.9		0.9		1.2	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		1.1		1.1		1.4	ns
t_{CGENR}		1.2		1.2		1.5	ns
t_{CASC}		1.1		1.1		1.3	ns
t_{C}		0.8		0.8		1.0	ns
t_{CO}		1.0		1.0		1.4	ns
t_{COMB}		0.5		0.5		0.7	ns
t_{SU}	2.1		2.1		2.6		ns
t_{H}	2.3		2.3		3.1		ns
t_{PRE}		1.0		1.0		1.4	ns
t_{CLR}		1.0		1.0		1.4	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns

Table 68. EPF10K100 Device Interconnect Timing Microparameters *Note (1)*

Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		10.3		10.3		12.2	ns
t_{DIN2LE}		4.8		4.8		6.0	ns
$t_{DIN2DATA}$		7.3		7.3		11.0	ns
$t_{DCLK2IOE}$ without ClockLock or ClockBoost circuitry		6.2		6.2		7.7	ns
$t_{DCLK2IOE}$ with ClockLock or ClockBoost circuitry		2.3		–		–	ns
$t_{DCLK2LE}$ without ClockLock or ClockBoost circuitry		4.8		4.8		6.0	ns
$t_{DCLK2LE}$ with ClockLock or ClockBoost circuitry		2.3		–		–	ns
$t_{SAMELAB}$		0.4		0.4		0.5	ns
$t_{SAMEROW}$		4.9		4.9		5.5	ns
$t_{SAMECOLUMN}$		5.1		5.1		5.4	ns
$t_{DIFFROW}$		10.0		10.0		10.9	ns
$t_{TWOROWS}$		14.9		14.9		16.4	ns
$t_{LEPERIPH}$		6.9		6.9		8.1	ns
$t_{LABCARRY}$		0.9		0.9		1.1	ns
$t_{LABCASC}$		3.0		3.0		3.2	ns

Table 69. EPF10K100 Device External Timing Parameters *Note (1)*

Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		19.1		19.1		24.2	ns
t_{INSU} *(2)*, *(3)*, *(4)*	7.8		7.8		8.5		ns
t_{OUTCO} *(3)*, *(4)*	2.0	11.1	2.0	11.1	2.0	14.3	ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{INSU} *(2)*, *(3)*, *(5)*	6.2		–		–		ns
t_{OUTCO} *(3)*, *(5)*	2.0	6.7		–		–	ns

Table 70. EPF10K100 Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ *(4)*	8.1		8.1		10.4		ns
$t_{INHBIDIR}$ *(4)*	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ *(4)*	2.0	11.1	2.0	11.1	2.0	14.3	ns
$t_{XZBIDIR}$ *(4)*		15.3		15.3		18.4	ns
$t_{ZXBIDIR}$ *(4)*		15.3		15.3		18.4	ns
$t_{INSUBIDIR}$ *(5)*	9.1		–		–		ns
$t_{INHBIDIR}$ *(5)*	0.0		–		–		ns
$t_{OUTCOBIDIR}$ *(5)*	2.0	7.2	–	–	–	–	ns
$t_{XZBIDIR}$ *(5)*		14.3		–		–	ns
$t_{ZXBIDIR}$ *(5)*		14.3		–		–	ns

Notes to tables:

(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.
(4) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(5) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Table 72. EPF10K50V Device IOE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{IOD}		1.2		1.6		1.9		2.1	ns
t_{IOC}		0.3		0.4		0.5		0.5	ns
t_{IOCO}		0.3		0.3		0.4		0.4	ns
t_{IOCOMB}		0.0		0.0		0.0		0.0	ns
t_{IOSU}	2.8		2.8		3.4		3.9		ns
t_{IOH}	0.7		0.8		1.0		1.4		ns
t_{IOCLR}		0.5		0.6		0.7		0.7	ns
t_{OD1}		2.8		3.2		3.9		4.7	ns
t_{OD2}		–		–		–		–	ns
t_{OD3}		6.5		6.9		7.6		8.4	ns
t_{XZ}		2.8		3.1		3.8		4.6	ns
t_{ZX1}		2.8		3.1		3.8		4.6	ns
t_{ZX2}		–		–		–		–	ns
t_{ZX3}		6.5		6.8		7.5		8.3	ns
t_{INREG}		5.0		5.7		7.0		9.0	ns
t_{IOFD}		1.5		1.9		2.3		2.7	ns
t_{INCOMB}		1.5		1.9		2.3		2.7	ns

Table 75. EPF10K50V Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		4.7		6.0		7.1		8.2	ns
t_{DIN2LE}		2.5		2.6		3.1		3.9	ns
$t_{DIN2DATA}$		4.4		5.9		6.8		7.7	ns
$t_{DCLK2IOE}$		2.5		3.9		4.7		5.5	ns
$t_{DCLK2LE}$		2.5		2.6		3.1		3.9	ns
$t_{SAMELAB}$		0.2		0.2		0.3		0.3	ns
$t_{SAMEROW}$		2.8		3.0		3.2		3.4	ns
$t_{SAMECOLUMN}$		3.0		3.2		3.4		3.6	ns
$t_{DIFFROW}$		5.8		6.2		6.6		7.0	ns
$t_{TWOROWS}$		8.6		9.2		9.8		10.4	ns
$t_{LEPERIPH}$		4.5		5.5		6.1		7.0	ns
$t_{LABCARRY}$		0.3		0.4		0.5		0.7	ns
$t_{LABCASC}$		0.0		1.3		1.6		2.0	ns

Table 76. EPF10K50V Device External Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{DRR}		11.2		14.0		17.2		21.1	ns
t_{INSU} *(2), (3)*	5.5		4.2		5.2		6.9		ns
t_{INH} *(3)*	0.0		0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	5.9	2.0	7.8	2.0	9.5	2.0	11.1	ns

Table 77. EPF10K50V Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.0		2.8		3.5		4.1		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	5.9	2.0	7.8	2.0	9.5	2.0	11.1	ns
$t_{XZBIDIR}$		8.0		9.8		11.8		14.3	ns
$t_{ZXBIDIR}$		8.0		9.8		11.8		14.3	ns

Notes to tables:
(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Tables 99 through 105 show EPF10K100A device internal and external timing parameters.

Table 99. EPF10K100A Device LE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		1.0		1.2		1.4	ns
t_{CLUT}		0.8		0.9		1.1	ns
t_{RLUT}		1.4		1.6		1.9	ns
t_{PACKED}		0.4		0.5		0.5	ns
t_{EN}		0.6		0.7		0.8	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		0.4		0.4		0.6	ns
t_{CGENR}		0.6		0.7		0.8	ns
t_{CASC}		0.7		0.9		1.0	ns
t_{C}		0.9		1.0		1.2	ns
t_{CO}		0.2		0.3		0.3	ns
t_{COMB}		0.6		0.7		0.8	ns
t_{SU}	0.8		1.0		1.2		ns
t_{H}	0.3		0.5		0.5		ns
t_{PRE}		0.3		0.3		0.4	ns
t_{CLR}		0.3		0.3		0.4	ns
t_{CH}	2.5		3.5		4.0		ns
t_{CL}	2.5		3.5		4.0		ns

Table 110. EPF10K250A Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		7.8		8.5		9.4	ns
t_{DIN2LE}		2.7		3.1		3.5	ns
$t_{DIN2DATA}$		1.6		1.6		1.7	ns
$t_{DCLK2IOE}$		3.6		4.0		4.6	ns
$t_{DCLK2LE}$		2.7		3.1		3.5	ns
$t_{SAMELAB}$		0.2		0.3		0.3	ns
$t_{SAMEROW}$		6.7		7.3		8.2	ns
$t_{SAMECOLUMN}$		2.5		2.7		3.0	ns
$t_{DIFFROW}$		9.2		10.0		11.2	ns
$t_{TWOROWS}$		15.9		17.3		19.4	ns
$t_{LEPERIPH}$		7.5		8.1		8.9	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.4		0.4		0.5	ns

Table 111. EPF10K250A Device External Reference Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		15.0		17.0		20.0	ns
t_{INSU} *(2), (3)*	6.9		8.0		9.4		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	8.0	2.0	8.9	2.0	10.4	ns

Table 112. EPF10K250A Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	9.3		10.6		12.7		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	8.0	2.0	8.9	2.0	10.4	ns
$t_{XZBIDIR}$		10.8		12.2		14.2	ns
$t_{ZXBIDIR}$		10.8		12.2		14.2	ns

Notes to tables:
(1) All timing parameters are described in Tables 32 through 37 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. Figure 31 illustrates the incoming and generated clock specifications.

Figure 31. Specifications for the Incoming & Generated Clocks

The t_I parameter refers to the nominal input clock period; the t_O parameter refers to the nominal output clock period.

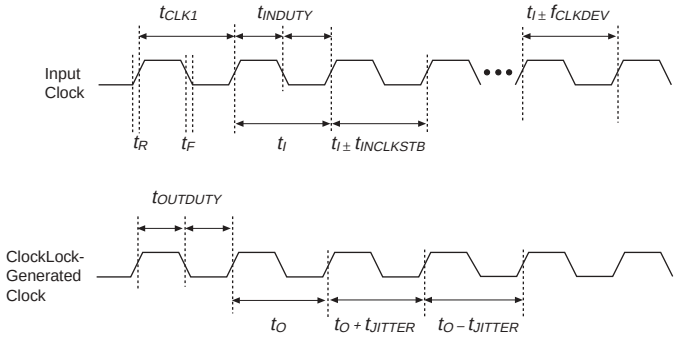


Table 113 summarizes the ClockLock and ClockBoost parameters.

Table 113. ClockLock & ClockBoost Parameters (Part 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
t_R	Input rise time			2	ns
t_F	Input fall time			2	ns
t_{INDUTY}	Input duty cycle	45		55	%
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)	30		80	MHz
t_{CLK1}	Input clock period (ClockBoost clock multiplication factor equals 1)	12.5		33.3	ns
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)	16		50	MHz
t_{CLK2}	Input clock period (ClockBoost clock multiplication factor equals 2)	20		62.5	ns

$\mathbf{f_{MAX}}$ = Maximum operating frequency in MHz
N = Total number of logic cells used in the device
$\mathbf{tog_{LC}}$ = Average percent of logic cells toggling at each clock (typically 12.5%)
K = Constant, shown in Tables 114 and 115

Table 114. FLEX 10K K Constant Values

Device	K Value
EPF10K10	82
EPF10K20	89
EPF10K30	88
EPF10K40	92
EPF10K50	95
EPF10K70	85
EPF10K100	88

Table 115. FLEX 10KA K Constant Values

Device	K Value
EPF10K10A	17
EPF10K30A	17
EPF10K50V	19
EPF10K100A	19
EPF10K130V	22
EPF10K250A	23

This calculation provides an I_{CC} estimate based on typical conditions with no output load. The actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

To better reflect actual designs, the power model (and the constant *K* in the power calculation equations) for continuous interconnect FLEX devices assumes that logic cells drive FastTrack Interconnect channels. In contrast, the power model of segmented FPGAs assumes that all logic cells drive only one short interconnect segment. This assumption may lead to inaccurate results, compared to measured power consumption for an actual design in a segmented interconnect FPGA.

Figure 32 shows the relationship between the current and operating frequency of FLEX 10K devices.

Multiple FLEX 10K devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 116. Data Sources for Configuration

Configuration Scheme	Data Source
Configuration device	EPC1, EPC2, EPC16, or EPC1441 configuration device
Passive serial (PS)	BitBlaster, MasterBlaster, or ByteBlasterMV download cable, or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	BitBlaster, MasterBlaster, or ByteBlasterMV download cable, or microprocessor with Jam STAPL file or Jam Byte-Code file

Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the Altera Digital Library for pin-out information.

Revision History

The information contained in the *FLEX 10K Embedded Programmable Logic Device Family Data Sheet* version 4.2 supersedes information published in previous versions.

Version 4.2 Changes

The following change was made to version 4.2 of the *FLEX 10K Embedded Programmable Logic Device Family Data Sheet*: updated Figure 13.

Version 4.1 Changes

The following changes were made to version 4.1 of the *FLEX 10K Embedded Programmable Logic Device Family Data Sheet*.

- Updated General Description section
- Updated I/O Element section
- Updated SameFrame Pin-Outs section
- Updated Figure 16
- Updated Tables 13 and 116
- Added Note 9 to Table 19
- Added Note 10 to Table 24
- Added Note 10 to Table 28