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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

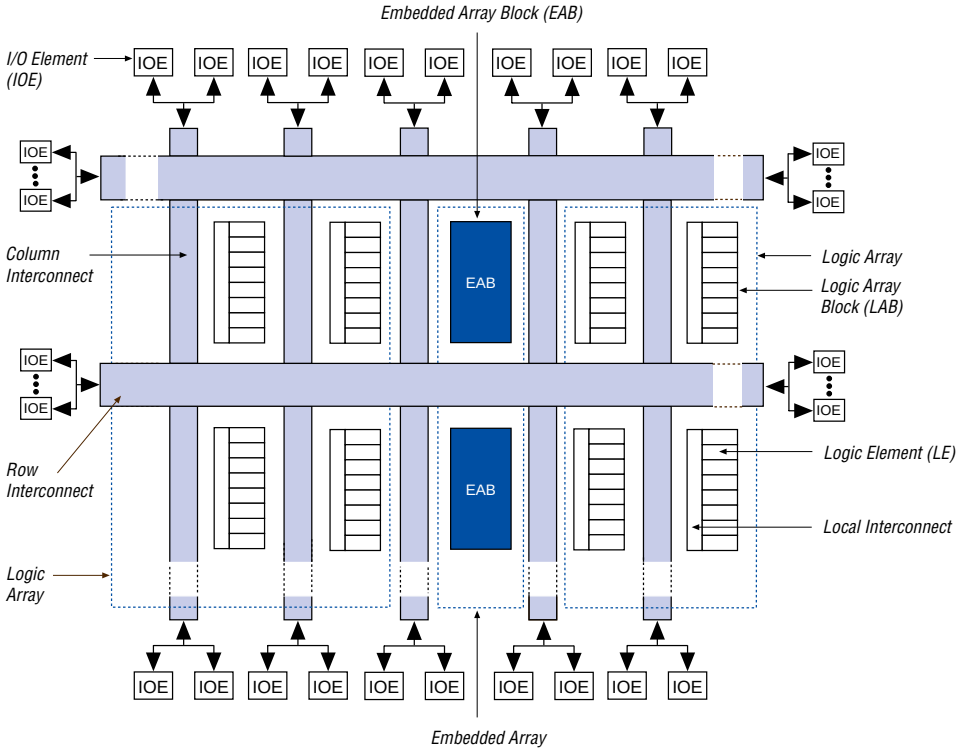
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 216 |
| Number of Logic Elements/Cells | 1728 |
| Total RAM Bits | 12288 |
| Number of I/O | 189 |
| Number of Gates | 69000 |
| Voltage - Supply | 4.5V ~ 5.5V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 240-BFQFP Exposed Pad |
| Supplier Device Package | 240-RQFP (32x32) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epf10k30ri240-4n |

*Figure 1. FLEX 10K Device Block Diagram*

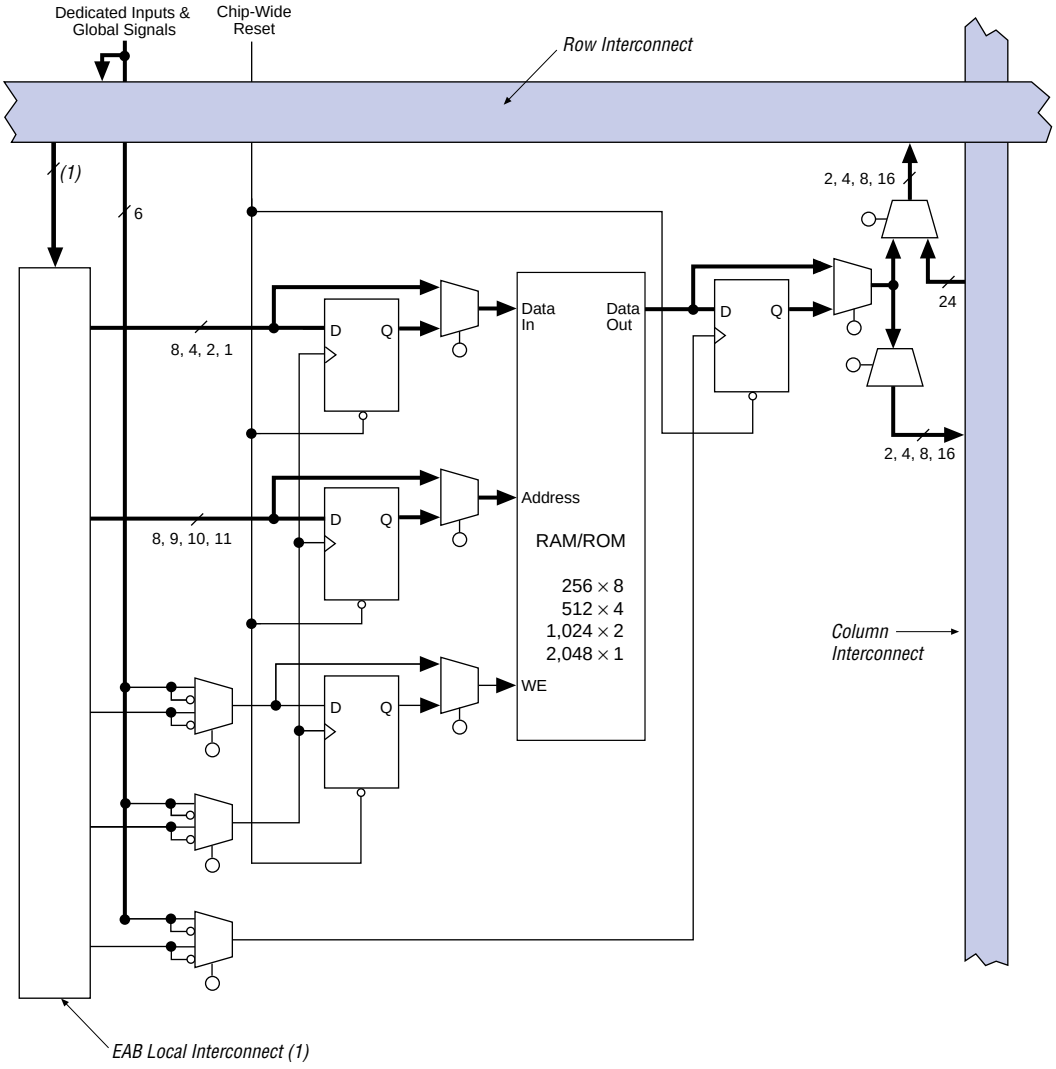



FLEX 10K devices provide six dedicated inputs that drive the flipflops' control inputs to ensure the efficient distribution of high-speed, low-skew (less than 1.5 ns) control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

## Embedded Array Block

The EAB is a flexible block of RAM with registers on the input and output ports, and is used to implement common gate array megafunctions. The EAB is also suitable for functions such as multipliers, vector scalars, and error correction circuits, because it is large and flexible. These functions can be combined in applications such as digital filters and microcontrollers.

*Figure 4. FLEX 10K Embedded Array Block*




*Note:*

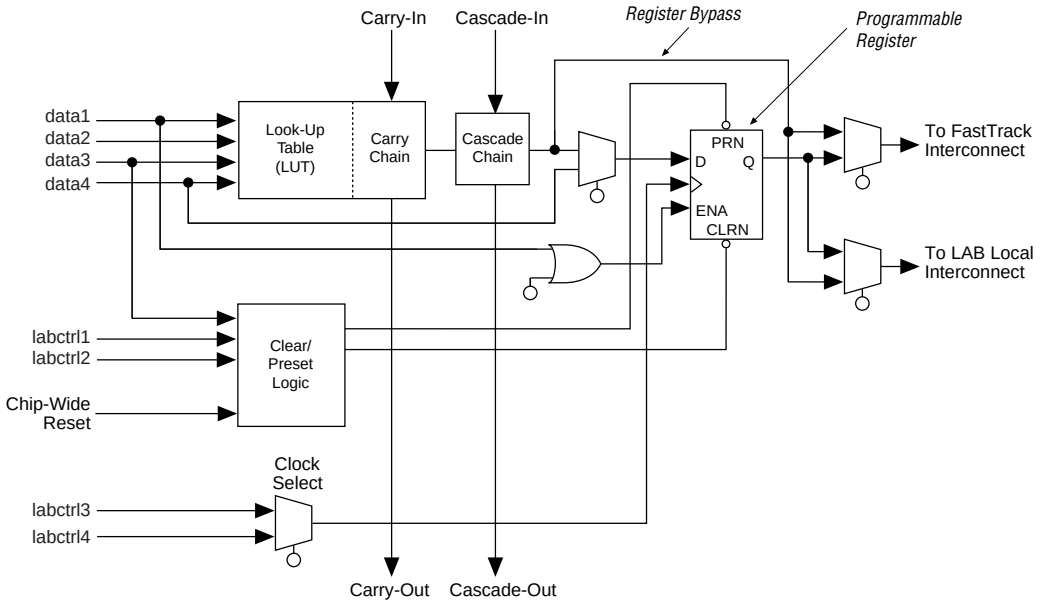
(1) EPF10K10, EPF10K10A, EPF10K20, EPF10K30, EPF10K30A, EPF10K40, EPF10K50, and EPF10K50V devices have 22 EAB local interconnect channels; EPF10K70, EPF10K100, EPF10K100A, EPF10K130V, and EPF10K250A devices have 26.

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks; the other two can be used for clear/preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I/O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I/O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

## Logic Element

The LE, the smallest unit of logic in the FLEX 10K architecture, has a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect. See Figure 6.

*Figure 6. FLEX 10K Logic Element*



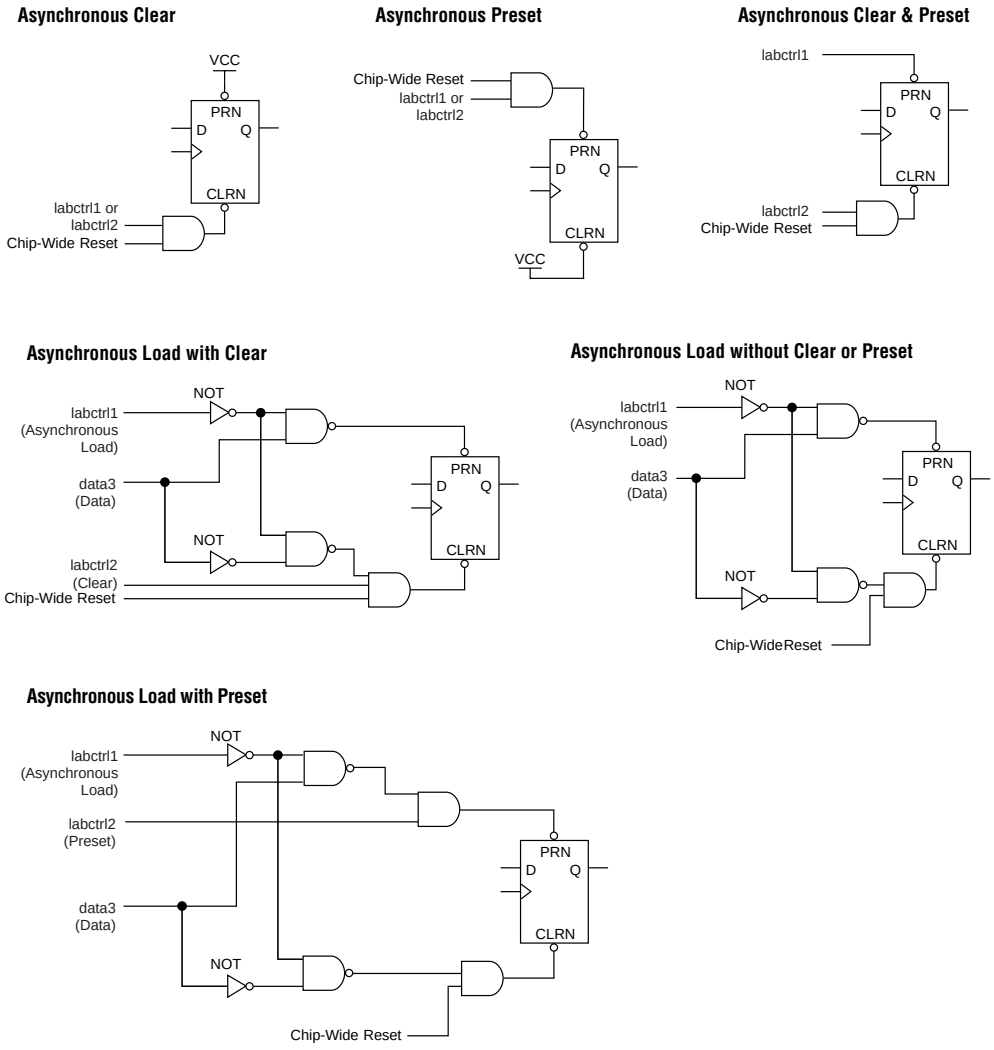
During compilation, the Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six modes chosen during design entry:

- Asynchronous clear
- Asynchronous preset
- Asynchronous clear and preset
- Asynchronous load with clear
- Asynchronous load with preset
- Asynchronous load without clear or preset

In addition to the six clear and preset modes, FLEX 10K devices provide a chip-wide reset pin that can reset all registers in the device. Use of this feature is set during design entry. In any of the clear and preset modes, the chip-wide reset overrides all other signals. Registers with asynchronous presets may be preset when the chip-wide reset is asserted. Inversion can be used to implement the asynchronous preset. Figure 10 shows examples of how to enter a section of a design for the desired functionality.

*Figure 10. LE Clear & Preset Modes*




### Asynchronous Clear

The flipflop can be cleared by either LABCTRL1 or LABCTRL2. In this mode, the preset signal is tied to $V_{CC}$ to deactivate it.

Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across devices; it provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock enable or eight output enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by specific LEs. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, an LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal. The chip-wide reset signal will reset all IOE registers, overriding any other control signals.

Tables 8 and 9 list the sources for each peripheral control signal, and the rows that can drive global signals. These tables also show how the output enable, clock enable, clock, and clear signals share 12 peripheral control signals.

## Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces system noise and adds a maximum delay of approximately 2.9 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a device-wide basis. The slow slew rate setting affects only the falling edge of the output.

## Open-Drain Output Option

FLEX 10K devices provide an optional open-drain (electrically equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane. Additionally, the Altera software can convert tri-state buffers with grounded data inputs to open-drain pins automatically.

Open-drain output pins on FLEX 10K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a $V_{IH}$ of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The $I_{OL}$ current specification should be considered when selecting a pull-up resistor.

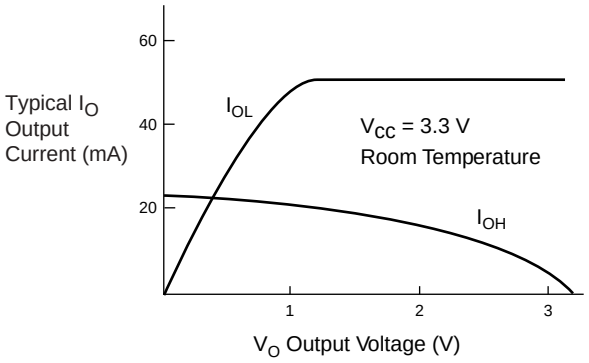
Output pins on 5.0-V FLEX 10K devices with $V_{CCIO}$ = 3.3 V or 5.0 V (with a pull-up resistor to the 5.0-V supply) can also drive 5.0-V CMOS input pins. In this case, the pull-up transistor will turn off when the pin voltage exceeds 3.3 V. Therefore, the pin does not have to be open-drain.

## MultiVolt I/O Interface

The FLEX 10K device architecture supports the MultiVolt I/O interface feature, which allows FLEX 10K devices to interface with systems of differing supply voltages. These devices have one set of $V_{CC}$ pins for internal operation and input buffers (VCCINT) and another set for I/O output drivers (VCCIO).

Figure 21 shows the typical output drive characteristics of EPF10K50V and EPF10K130V devices.

*Figure 21. Output Drive Characteristics of EPF10K50V & EPF10K130V Devices*




Tables 26 through 31 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 3.3-V FLEX 10K devices.

*Table 26. FLEX 10KA 3.3-V Device Absolute Maximum Ratings* *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to ground *(2)* | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –2.0 | 5.75 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | Ceramic packages, under bias | | 150 | ° C |
| | | PQFP, TQFP, RQFP, and BGA packages, under bias | | 135 | ° C |

*Table 27. FLEX 10KA 3.3-V Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(3)*, *(4)* | 2.30 (2.30) | 2.70 (2.70) | V |
| $V_I$ | Input voltage | *(5)* | –0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | For commercial use | 0 | 70 | ° C |
| | | For industrial use | –40 | 85 | ° C |
| $T_J$ | Operating temperature | For commercial use | 0 | 85 | ° C |
| | | For industrial use | –40 | 100 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Figure 24 shows the overall timing model, which maps the possible paths to and from the various elements of the FLEX 10K device.

*Figure 24. FLEX 10K Device Timing Model*

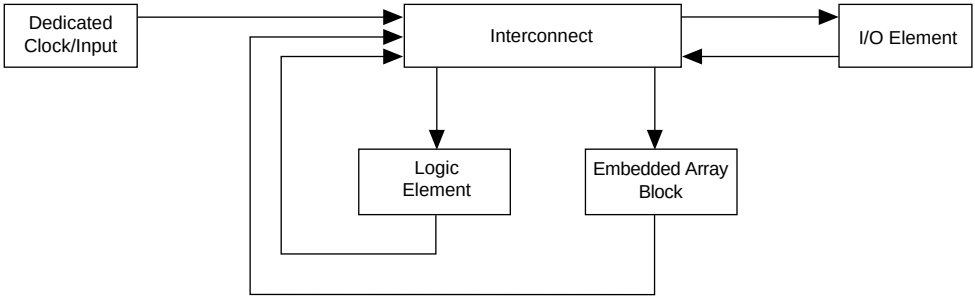


*Figure 26. FLEX 10K Device IOE Timing Model*

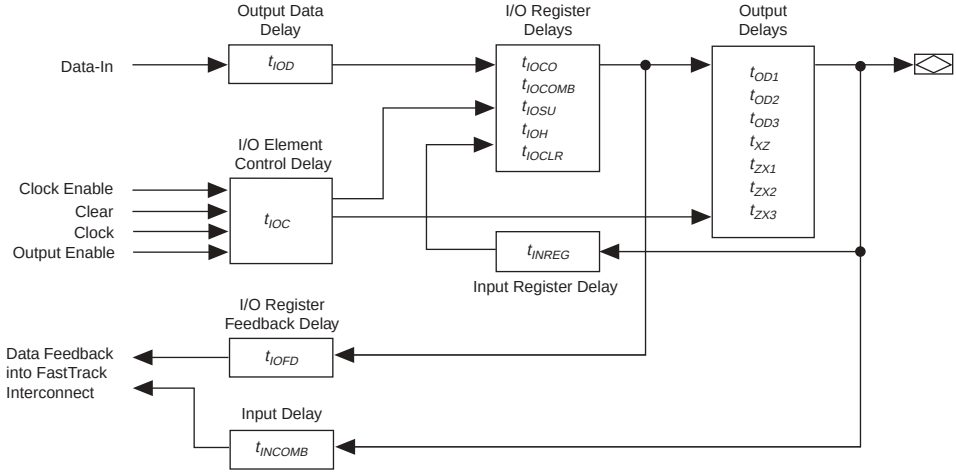
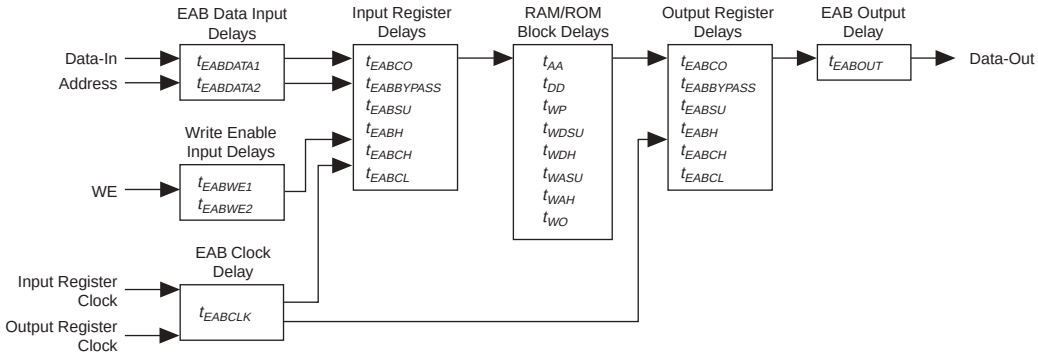



*Figure 27. FLEX 10K Device EAB Timing Model*




Figures 28 shows the timing model for bidirectional I/O pin timing.

**Table 32. LE Timing Microparameters (Part 2 of 2)** *Note (1)*

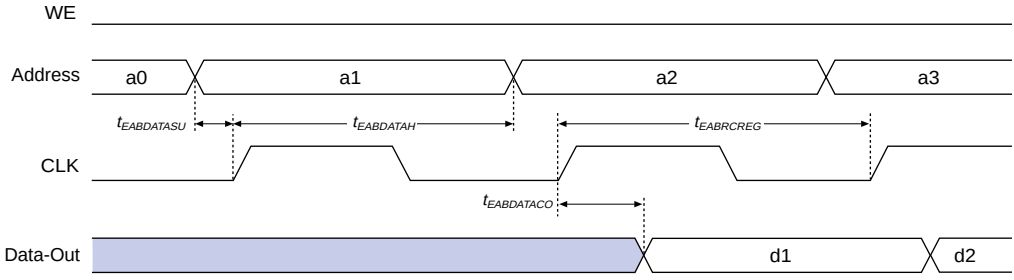
| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{SU}$ | LE register setup time for data and enable signals before clock; LE register recovery time after asynchronous clear, preset, or load | |
| $t_{H}$ | LE register hold time for data and enable signals after clock | |
| $t_{PRE}$ | LE register preset delay | |
| $t_{CLR}$ | LE register clear delay | |
| $t_{CH}$ | Minimum clock high time from clock pin | |
| $t_{CL}$ | Minimum clock low time from clock pin | |

**Table 33. IOE Timing Microparameters** *Note (1)*

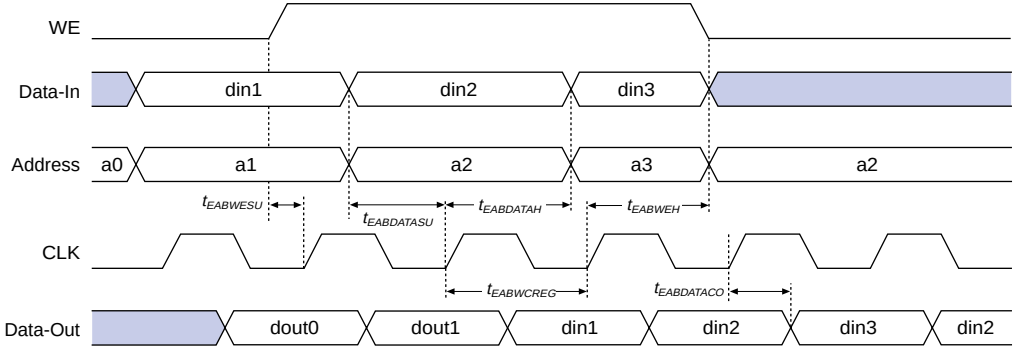
| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{IOD}$ | IOE data delay | |
| $t_{IOC}$ | IOE register control signal delay | |
| $t_{IOCO}$ | IOE register clock-to-output delay | |
| $t_{IOCOMB}$ | IOE combinatorial delay | |
| $t_{IOSU}$ | IOE register setup time for data and enable signals before clock; IOE register recovery time after asynchronous clear | |
| $t_{IOH}$ | IOE register hold time for data and enable signals after clock | |
| $t_{IOCLR}$ | IOE register clear time | |
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$ | C1 = 35 pF *(2)* |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off, $V_{CCIO}$ = low voltage | C1 = 35 pF *(3)* |
| $t_{OD3}$ | Output buffer and pad delay, slow slew rate = on | C1 = 35 pF *(4)* |
| $t_{XZ}$ | IOE output buffer disable delay | |
| $t_{ZX1}$ | IOE output buffer enable delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$ | C1 = 35 pF *(2)* |
| $t_{ZX2}$ | IOE output buffer enable delay, slow slew rate = off, $V_{CCIO}$ = low voltage | C1 = 35 pF *(3)* |
| $t_{ZX3}$ | IOE output buffer enable delay, slow slew rate = on | C1 = 35 pF *(4)* |
| $t_{INREG}$ | IOE input pad and buffer to IOE register delay | |
| $t_{IOFD}$ | IOE register feedback delay | |
| $t_{INCOMB}$ | IOE input pad and buffer to FastTrack Interconnect delay | |

*Figure 30. EAB Synchronous Timing Waveforms*

**EAB Synchronous Read**




**EAB Synchronous Write (EAB Output Registers Used)**



*Notes to tables:*
(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Tables 57 through 63 show EPF10K70 device internal and external timing parameters.

**Table 57. EPF10K70 Device LE Timing Microparameters** *Note (1)*

| Symbol | -2 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 1.3 | | 1.5 | | 2.0 | ns |
| $t_{CLUT}$ | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{RLUT}$ | | 1.5 | | 1.6 | | 2.0 | ns |
| $t_{PACKED}$ | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{EN}$ | | 0.8 | | 0.9 | | 1.2 | ns |
| $t_{CICO}$ | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{CGEN}$ | | 1.0 | | 1.1 | | 1.4 | ns |
| $t_{CGENR}$ | | 1.1 | | 1.2 | | 1.5 | ns |
| $t_{CASC}$ | | 1.0 | | 1.1 | | 1.3 | ns |
| $t_{C}$ | | 0.7 | | 0.8 | | 1.0 | ns |
| $t_{CO}$ | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{SU}$ | 1.9 | | 2.1 | | 2.6 | | ns |
| $t_{H}$ | 2.1 | | 2.3 | | 3.1 | | ns |
| $t_{PRE}$ | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{CLR}$ | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{CH}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | 4.0 | | 4.0 | | 4.0 | | ns |

*Table 59. EPF10K70 Device EAB Internal Microparameters* *Note (1)*

| Symbol | -2 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.3 | | 1.5 | | 1.9 | ns |
| $t_{EABDATA2}$ | | 4.3 | | 4.8 | | 6.0 | ns |
| $t_{EABWE1}$ | | 0.9 | | 1.0 | | 1.2 | ns |
| $t_{EABWE2}$ | | 4.5 | | 5.0 | | 6.2 | ns |
| $t_{EABCLK}$ | | 0.9 | | 1.0 | | 2.2 | ns |
| $t_{EABCO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{EABBYPASS}$ | | 1.3 | | 1.5 | | 1.9 | ns |
| $t_{EABSU}$ | 1.3 | | 1.5 | | 1.8 | | ns |
| $t_{EABH}$ | 1.8 | | 2.0 | | 2.5 | | ns |
| $t_{AA}$ | | 7.8 | | 8.7 | | 10.7 | ns |
| $t_{WP}$ | 5.2 | | 5.8 | | 7.2 | | ns |
| $t_{WDSU}$ | 1.4 | | 1.6 | | 2.0 | | ns |
| $t_{WDH}$ | 0.3 | | 0.3 | | 0.4 | | ns |
| $t_{WASU}$ | 0.4 | | 0.5 | | 0.6 | | ns |
| $t_{WAH}$ | 0.9 | | 1.0 | | 1.2 | | ns |
| $t_{WO}$ | | 4.5 | | 5.0 | | 6.2 | ns |
| $t_{DD}$ | | 4.5 | | 5.0 | | 6.2 | ns |
| $t_{EABOUT}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{EABCH}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{EABCL}$ | 5.2 | | 5.8 | | 7.2 | | ns |

*Table 74. EPF10K50V Device EAB Internal Timing Macroparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{EABAA}$ | | 9.5 | | 13.6 | | 16.5 | | 20.8 | ns |
| $t_{EABRCCOMB}$ | 9.5 | | 13.6 | | 16.5 | | 20.8 | | ns |
| $t_{EABRCREG}$ | 6.1 | | 8.8 | | 10.8 | | 13.4 | | ns |
| $t_{EABWP}$ | 6.0 | | 4.9 | | 6.0 | | 7.4 | | ns |
| $t_{EABWCCOMB}$ | 6.2 | | 6.1 | | 7.5 | | 9.2 | | ns |
| $t_{EABWCREG}$ | 12.0 | | 11.6 | | 14.2 | | 17.4 | | ns |
| $t_{EABDD}$ | | 6.8 | | 9.7 | | 11.8 | | 14.9 | ns |
| $t_{EABDATACO}$ | | 1.0 | | 1.4 | | 1.8 | | 2.2 | ns |
| $t_{EABDATASU}$ | 5.3 | | 4.6 | | 5.6 | | 6.9 | | ns |
| $t_{EABDATAH}$ | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWESU}$ | 4.4 | | 4.8 | | 5.8 | | 7.2 | | ns |
| $t_{EABWEH}$ | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWDSU}$ | 1.8 | | 1.1 | | 1.4 | | 2.1 | | ns |
| $t_{EABWDH}$ | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWASU}$ | 4.5 | | 4.6 | | 5.6 | | 7.4 | | ns |
| $t_{EABWAH}$ | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWO}$ | | 5.1 | | 9.4 | | 11.4 | | 14.0 | ns |

| *Table 81. EPF10K130V Device EAB Internal Timing Macroparameters* *Note (1)* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **-2 Speed Grade** | | **-3 Speed Grade** | | **-4 Speed Grade** | | **Unit** |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{EABAA}$ | | 11.2 | | 14.2 | | 14.2 | ns |
| $t_{EABRCCOMB}$ | 11.1 | | 14.2 | | 14.2 | | ns |
| $t_{EABRCREG}$ | 8.5 | | 10.8 | | 10.8 | | ns |
| $t_{EABWP}$ | 3.7 | | 4.7 | | 4.7 | | ns |
| $t_{EABWCCOMB}$ | 7.6 | | 9.7 | | 9.7 | | ns |
| $t_{EABWCREG}$ | 14.0 | | 17.8 | | 17.8 | | ns |
| $t_{EABDD}$ | | 11.1 | | 14.2 | | 14.2 | ns |
| $t_{EABDATACO}$ | | 3.6 | | 4.6 | | 4.6 | ns |
| $t_{EABDATASU}$ | 4.4 | | 5.6 | | 5.6 | | ns |
| $t_{EABDATAH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWESU}$ | 4.4 | | 5.6 | | 5.6 | | ns |
| $t_{EABWEH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWDSU}$ | 4.6 | | 5.9 | | 5.9 | | ns |
| $t_{EABWDH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWASU}$ | 3.9 | | 5.0 | | 5.0 | | ns |
| $t_{EABWAH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWO}$ | | 11.1 | | 14.2 | | 14.2 | ns |

*Notes to tables:*
(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Tables 92 through 98 show EPF10K30A device internal and external timing parameters.

**Table 92. EPF10K30A Device LE Timing Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.8 | | 1.1 | | 1.5 | ns |
| $t_{CLUT}$ | | 0.6 | | 0.7 | | 1.0 | ns |
| $t_{RLUT}$ | | 1.2 | | 1.5 | | 2.0 | ns |
| $t_{PACKED}$ | | 0.6 | | 0.6 | | 1.0 | ns |
| $t_{EN}$ | | 1.3 | | 1.5 | | 2.0 | ns |
| $t_{CICO}$ | | 0.2 | | 0.3 | | 0.4 | ns |
| $t_{CGEN}$ | | 0.8 | | 1.0 | | 1.3 | ns |
| $t_{CGENR}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{CASC}$ | | 0.9 | | 1.1 | | 1.4 | ns |
| $t_{C}$ | | 1.1 | | 1.3 | | 1.7 | ns |
| $t_{CO}$ | | 0.4 | | 0.6 | | 0.7 | ns |
| $t_{COMB}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{SU}$ | 0.9 | | 0.9 | | 1.4 | | ns |
| $t_{H}$ | 1.1 | | 1.3 | | 1.7 | | ns |
| $t_{PRE}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{CLR}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{CH}$ | 3.0 | | 3.5 | | 4.0 | | ns |
| $t_{CL}$ | 3.0 | | 3.5 | | 4.0 | | ns |

**Table 93. EPF10K30A Device IOE Timing Microparameters** *Note (1)* **(Part 1 of 2)**

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 2.2 | | 2.6 | | 3.4 | ns |
| $t_{IOC}$ | | 0.3 | | 0.3 | | 0.5 | ns |
| $t_{IOCO}$ | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{IOCOMB}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{IOSU}$ | 1.4 | | 1.7 | | 2.2 | | ns |

*Table 96. EPF10K30A Device Interconnect Timing Microparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 3.9 | | 4.4 | | 5.1 | ns |
| $t_{DIN2LE}$ | | 1.2 | | 1.5 | | 1.9 | ns |
| $t_{DIN2DATA}$ | | 3.2 | | 3.6 | | 4.5 | ns |
| $t_{DCLK2IOE}$ | | 3.0 | | 3.5 | | 4.6 | ns |
| $t_{DCLK2LE}$ | | 1.2 | | 1.5 | | 1.9 | ns |
| $t_{SAMELAB}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{SAMEROW}$ | | 2.3 | | 2.4 | | 2.7 | ns |
| $t_{SAMECOLUMN}$ | | 1.3 | | 1.4 | | 1.9 | ns |
| $t_{DIFFROW}$ | | 3.6 | | 3.8 | | 4.6 | ns |
| $t_{TWOROWS}$ | | 5.9 | | 6.2 | | 7.3 | ns |
| $t_{LEPERIPH}$ | | 3.5 | | 3.8 | | 4.1 | ns |
| $t_{LABCARRY}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{LABCASC}$ | | 0.9 | | 1.1 | | 1.4 | ns |

*Table 97. EPF10K30A External Reference Timing Parameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 11.0 | | 13.0 | | 17.0 | ns |
| $t_{INSU}$ *(2)*, *(3)* | 2.5 | | 3.1 | | 3.9 | | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(3)* | 2.0 | 5.4 | 2.0 | 6.2 | 2.0 | 8.3 | ns |

*Table 98. EPF10K30A Device External Bidirectional Timing Parameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 4.2 | | 4.9 | | 6.8 | | ns |
| $t_{INHBIDIR}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ | 2.0 | 5.4 | 2.0 | 6.2 | 2.0 | 8.3 | ns |
| $t_{XZBIDIR}$ | | 6.2 | | 7.5 | | 9.8 | ns |
| $t_{ZXBIDIR}$ | | 6.2 | | 7.5 | | 9.8 | ns |

*Table 107. EPF10K250A Device IOE Timing Microparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 1.2 | | 1.3 | | 1.6 | ns |
| $t_{IOC}$ | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{IOCO}$ | | 0.8 | | 0.9 | | 1.1 | ns |
| $t_{IOCOMB}$ | | 0.7 | | 0.7 | | 0.8 | ns |
| $t_{IOSU}$ | 2.7 | | 3.1 | | 3.6 | | ns |
| $t_{IOH}$ | 0.2 | | 0.3 | | 0.3 | | ns |
| $t_{IOCLR}$ | | 1.2 | | 1.3 | | 1.6 | ns |
| $t_{OD1}$ | | 3.2 | | 3.6 | | 4.2 | ns |
| $t_{OD2}$ | | 5.9 | | 6.7 | | 7.8 | ns |
| $t_{OD3}$ | | 8.7 | | 9.8 | | 11.5 | ns |
| $t_{XZ}$ | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{ZX1}$ | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{ZX2}$ | | 6.5 | | 7.4 | | 8.6 | ns |
| $t_{ZX3}$ | | 9.3 | | 10.5 | | 12.3 | ns |
| $t_{INREG}$ | | 8.2 | | 9.3 | | 10.9 | ns |
| $t_{IOFD}$ | | 9.0 | | 10.2 | | 12.0 | ns |
| $t_{INCOMB}$ | | 9.0 | | 10.2 | | 12.0 | ns |