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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 360 |
| Number of Logic Elements/Cells | 2880 |
| Total RAM Bits | 20480 |
| Number of I/O | 189 |
| Number of Gates | 116000 |
| Voltage - Supply | 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 240-BFQFP Exposed Pad |
| Supplier Device Package | 240-RQFP (32x32) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epf10k50rc240-4n |

The logic array consists of logic array blocks (LABs). Each LAB contains eight LEs and a local interconnect. An LE consists of a 4-input look-up table (LUT), a programmable flipflop, and dedicated signal paths for carry and cascade functions. The eight LEs can be used to create medium-sized blocks of logic—8-bit counters, address decoders, or state machines—or combined across LABs to create larger logic blocks. Each LAB represents about 96 usable gates of logic.

Signal interconnections within FLEX 10K devices and to and from device pins are provided by the FastTrack Interconnect, a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an output or input register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. As inputs, they provide setup times as low as 1.6 ns and hold times of 0 ns; as outputs, these registers provide clock-to-output times as low as 5.3 ns. IOEs provide a variety of features, such as JTAG BST support, slew-rate control, tri-state buffers, and open-drain outputs.

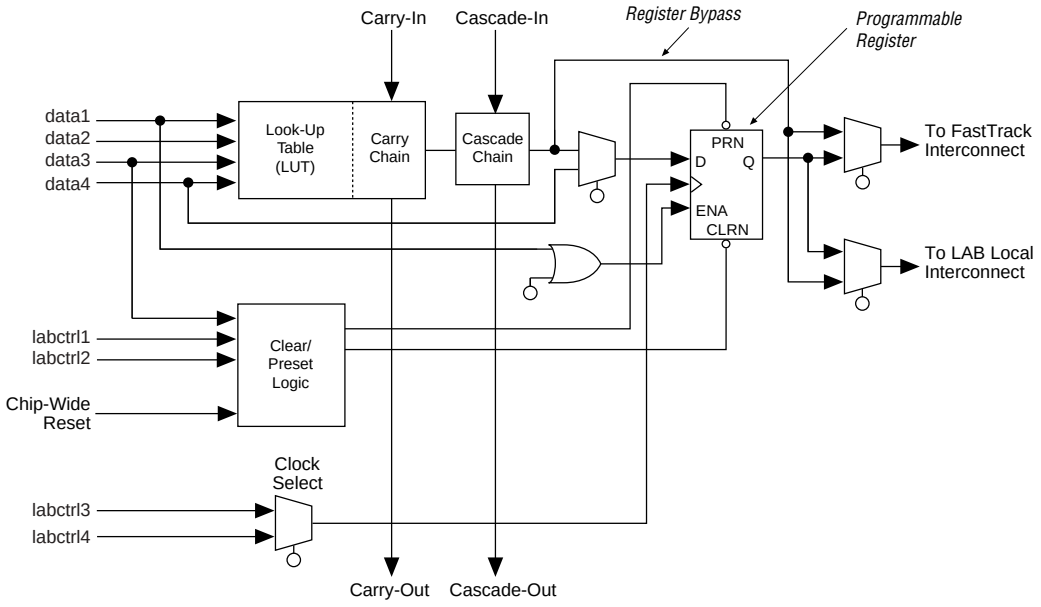
Figure 1 shows a block diagram of the FLEX 10K architecture. Each group of LEs is combined into an LAB; LABs are arranged into rows and columns. Each row also contains a single EAB. The LABs and EABs are interconnected by the FastTrack Interconnect. IOEs are located at the end of each row and column of the FastTrack Interconnect.

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks; the other two can be used for clear/preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I/O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I/O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

## Logic Element

The LE, the smallest unit of logic in the FLEX 10K architecture, has a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect. See Figure 6.

*Figure 6. FLEX 10K Logic Element*



The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the flipflop is bypassed and the output of the LUT drives the output of the LE.

The LE has two outputs that drive the interconnect; one drives the local interconnect and the other drives either the row or column FastTrack Interconnect. The two outputs can be controlled independently. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, can improve LE utilization because the register and the LUT can be used for unrelated functions.

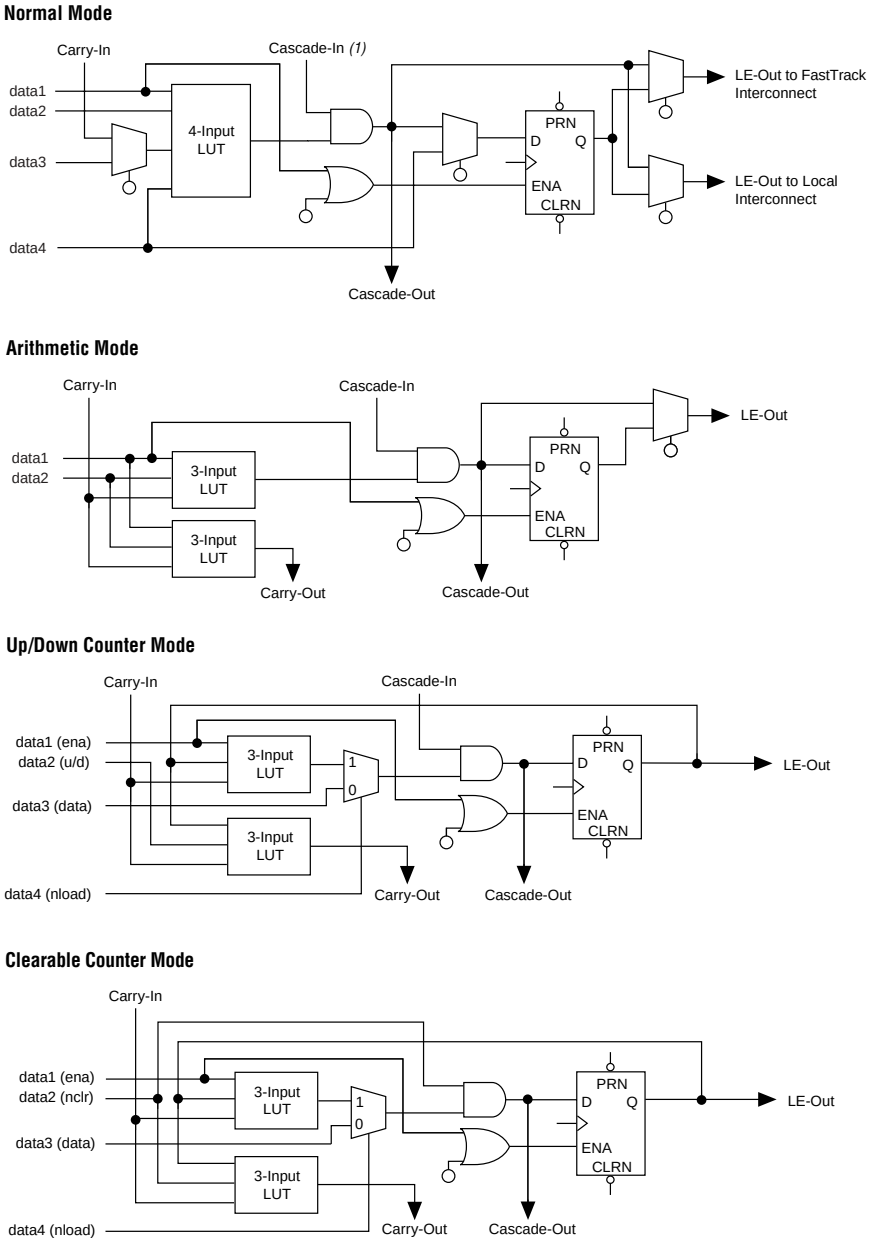
The FLEX 10K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. The carry chain supports high-speed counters and adders; the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in an LAB and all LABs in the same row. Intensive use of carry and cascade chains can reduce routing flexibility. Therefore, the use of these chains should be limited to speed-critical portions of a design.

### *Carry Chain*

The carry chain provides a very fast (as low as 0.2 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 10K architecture to implement high-speed counters, adders, and comparators of arbitrary width efficiently. Carry chain logic can be created automatically by the Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of carry chains.

Carry chains longer than eight LEs are automatically implemented by linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a row. A carry chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB. For example, the last LE of the first LAB in a row carries to the first LE of the third LAB in the row. The carry chain does not cross the EAB at the middle of the row. For instance, in the EPF10K50 device, the carry chain stops at the eighteenth LAB and a new one begins at the nineteenth LAB.

*Figure 9. FLEX 10K LE Operating Modes*




*Note:*
(1) Packed registers cannot be used with the cascade chain.

## I/O Element

An I/O element (IOE) contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. In some cases, using an LE register for an input register will result in a faster setup time than using an IOE register. IOEs can be used as input, output, or bidirectional pins. For bidirectional registered I/O implementation, the output register should be in the IOE and, the data input and output enable register should be LE registers placed adjacent to the bidirectional pin. The Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Figure 13 shows the bidirectional I/O registers.

*Table 8. EPF10K10, EPF10K20, EPF10K30, EPF10K40 & EPF10K50 Peripheral Bus Sources*

| Peripheral Control Signal | EPF10K10 EPF10K10A | EPF10K20 | EPF10K30 EPF10K30A | EPF10K40 | EPF10K50 EPF10K50V |
|---|---|---|---|---|---|
| OE0 | Row A | Row A | Row A | Row A | Row A |
| OE1 | Row A | Row B | Row B | Row C | Row B |
| OE2 | Row B | Row C | Row C | Row D | Row D |
| OE3 | Row B | Row D | Row D | Row E | Row F |
| OE4 | Row C | Row E | Row E | Row F | Row H |
| OE5 | Row C | Row F | Row F | Row G | Row J |
| CLKENA0/CLK0/GLOBAL0 | Row A | Row A | Row A | Row B | Row A |
| CLKENA1/OE6/GLOBAL1 | Row A | Row B | Row B | Row C | Row C |
| CLKENA2/CLR0 | Row B | Row C | Row C | Row D | Row E |
| CLKENA3/OE7/GLOBAL2 | Row B | Row D | Row D | Row E | Row G |
| CLKENA4/CLR1 | Row C | Row E | Row E | Row F | Row I |
| CLKENA5/CLK1/GLOBAL3 | Row C | Row F | Row F | Row H | Row J |

*Table 9. EPF10K70, EPF10K100, EPF10K130V & EPF10K250A Peripheral Bus Sources*

| Peripheral Control Signal | EPF10K70 | EPF10K100 EPF10K100A | EPF10K130V | EPF10K250A |
|---|---|---|---|---|
| OE0 | Row A | Row A | Row C | Row E |
| OE1 | Row B | Row C | Row E | Row G |
| OE2 | Row D | Row E | Row G | Row I |
| OE3 | Row I | Row L | Row N | Row P |
| OE4 | Row G | Row I | Row K | Row M |
| OE5 | Row H | Row K | Row M | Row O |
| CLKENA0/CLK0/GLOBAL0 | Row E | Row F | Row H | Row J |
| CLKENA1/OE6/GLOBAL1 | Row C | Row D | Row F | Row H |
| CLKENA2/CLR0 | Row B | Row B | Row D | Row F |
| CLKENA3/OE7/GLOBAL2 | Row F | Row H | Row J | Row L |
| CLKENA4/CLR1 | Row H | Row J | Row L | Row N |
| CLKENA5/CLK1/GLOBAL3 | Row E | Row G | Row I | Row K |

**Table 24. EPF10K50V & EPF10K130V Device DC Operating Conditions** *Notes (6), (7)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2.0 | | 5.75 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.8 | V |
| $V_{OH}$ | 3.3-V high-level TTL output voltage | $I_{OH}$ = –8 mA DC *(8)* | 2.4 | | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC *(8)* | $V_{CCIO}$ – 0.2 | | | V |
| $V_{OL}$ | 3.3-V low-level TTL output voltage | $I_{OL}$ = 8 mA DC *(9)* | | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC *(9)* | | | 0.2 | V |
| $I_I$ | Input pin leakage current | $V_I$ = 5.3 V to –0.3 V *(10)* | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O$ = 5.3 V to –0.3 V *(10)* | –10 | | 10 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) | $V_I$ = ground, no load | | 0.3 | 10 | mA |
| | | $V_I$ = ground, no load *(11)* | | 10 | | mA |

**Table 25. EPF10K50V & EPF10K130V Device Capacitance** *(12)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 10 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 15 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 10 | pF |

***Notes to tables:***

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum $V_{CC}$ rise time is 100 ms. $V_{CC}$ must rise monotonically.
(5) EPF10K50V and EPF10K130V device inputs may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.
(6) Typical values are for $T_A$ = 25° C and $V_{CC}$ = 3.3 V.
(7) These values are specified under the EPF10K50V and EPF10K130V device Recommended Operating Conditions in Table 23 on page 48.
(8) The $I_{OH}$ parameter refers to high-level TTL or CMOS output current.
(9) The $I_{OL}$ parameter refers to low-level TTL or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(10) This value is specified for normal device operation. The value may vary during power-up.
(11) This parameter applies to -1 speed grade EPF10K50V devices, -2 speed grade EPF10K50V industrial temperature devices, and -2 speed grade EPF10K130V devices.
(12) Capacitance is sample-tested only.

*Table 27. FLEX 10KA 3.3-V Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(3)*, *(4)* | 2.30 (2.30) | 2.70 (2.70) | V |
| $V_I$ | Input voltage | *(5)* | –0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | For commercial use | 0 | 70 | ° C |
| | | For industrial use | –40 | 85 | ° C |
| $T_J$ | Operating temperature | For commercial use | 0 | 85 | ° C |
| | | For industrial use | –40 | 100 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

**Table 34. EAB Timing Microparameters** *Note (1)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{EABDATA1}$ | Data or address delay to EAB for combinatorial input | |
| $t_{EABDATA2}$ | Data or address delay to EAB for registered input | |
| $t_{EABWE1}$ | Write enable delay to EAB for combinatorial input | |
| $t_{EABWE2}$ | Write enable delay to EAB for registered input | |
| $t_{EABCLK}$ | EAB register clock delay | |
| $t_{EABCO}$ | EAB register clock-to-output delay | |
| $t_{EABBYPASS}$ | Bypass register delay | |
| $t_{EABSU}$ | EAB register setup time before clock | |
| $t_{EABH}$ | EAB register hold time after clock | |
| $t_{AA}$ | Address access delay | |
| $t_{WP}$ | Write pulse width | |
| $t_{WDSU}$ | Data setup time before falling edge of write pulse | *(5)* |
| $t_{WDH}$ | Data hold time after falling edge of write pulse | *(5)* |
| $t_{WASU}$ | Address setup time before rising edge of write pulse | *(5)* |
| $t_{WAH}$ | Address hold time after falling edge of write pulse | *(5)* |
| $t_{WO}$ | Write enable to data output valid delay | |
| $t_{DD}$ | Data-in to data-out valid delay | |
| $t_{EABOUT}$ | Data-out delay | |
| $t_{EABCH}$ | Clock high time | |
| $t_{EABCL}$ | Clock low time | |

Tables 39 through 47 show EPF10K10 and EPF10K20 device internal and external timing parameters.

*Table 39. EPF10K10 & EPF10K20 Device LE Timing Microparameters* *Note (1)*

| Symbol | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| $t_{LUT}$ | | 1.4 | | 1.7 | ns |
| $t_{CLUT}$ | | 0.6 | | 0.7 | ns |
| $t_{RLUT}$ | | 1.5 | | 1.9 | ns |
| $t_{PACKED}$ | | 0.6 | | 0.9 | ns |
| $t_{EN}$ | | 1.0 | | 1.2 | ns |
| $t_{CICO}$ | | 0.2 | | 0.3 | ns |
| $t_{CGEN}$ | | 0.9 | | 1.2 | ns |
| $t_{CGENR}$ | | 0.9 | | 1.2 | ns |
| $t_{CASC}$ | | 0.8 | | 0.9 | ns |
| $t_{C}$ | | 1.3 | | 1.5 | ns |
| $t_{CO}$ | | 0.9 | | 1.1 | ns |
| $t_{COMB}$ | | 0.5 | | 0.6 | ns |
| $t_{SU}$ | 1.3 | | 2.5 | | ns |
| $t_{H}$ | 1.4 | | 1.6 | | ns |
| $t_{PRE}$ | | 1.0 | | 1.2 | ns |
| $t_{CLR}$ | | 1.0 | | 1.2 | ns |
| $t_{CH}$ | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | 4.0 | | 4.0 | | ns |

*Table 41. EPF10K10 & EPF10K20 Device EAB Internal Microparameters* *Note (1)*

| Symbol | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.5 | | 1.9 | ns |
| $t_{EABDATA2}$ | | 4.8 | | 6.0 | ns |
| $t_{EABWE1}$ | | 1.0 | | 1.2 | ns |
| $t_{EABWE2}$ | | 5.0 | | 6.2 | ns |
| $t_{EABCLK}$ | | 1.0 | | 2.2 | ns |
| $t_{EABCO}$ | | 0.5 | | 0.6 | ns |
| $t_{EABBYPASS}$ | | 1.5 | | 1.9 | ns |
| $t_{EABSU}$ | 1.5 | | 1.8 | | ns |
| $t_{EABH}$ | 2.0 | | 2.5 | | ns |
| $t_{AA}$ | | 8.7 | | 10.7 | ns |
| $t_{WP}$ | 5.8 | | 7.2 | | ns |
| $t_{WDSU}$ | 1.6 | | 2.0 | | ns |
| $t_{WDH}$ | 0.3 | | 0.4 | | ns |
| $t_{WASU}$ | 0.5 | | 0.6 | | ns |
| $t_{WAH}$ | 1.0 | | 1.2 | | ns |
| $t_{WO}$ | | 5.0 | | 6.2 | ns |
| $t_{DD}$ | | 5.0 | | 6.2 | ns |
| $t_{EABOUT}$ | | 0.5 | | 0.6 | ns |
| $t_{EABCH}$ | 4.0 | | 4.0 | | ns |
| $t_{EABCL}$ | 5.8 | | 7.2 | | ns |

**Table 45. EPF10K10 & EPF10K20 Device External Timing Parameters** *Note (1)*

| Symbol | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| $t_{DRR}$ | | 16.1 | | 20.0 | ns |
| $t_{INSU}$ *(2)*, *(3)* | 5.5 | | 6.0 | | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(3)* | 2.0 | 6.7 | 2.0 | 8.4 | ns |

**Table 46. EPF10K10 Device External Bidirectional Timing Parameters** *Note (1)*

| Symbol | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 4.5 | | 5.6 | | ns |
| $t_{INHBIDIR}$ | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ | 2.0 | 6.7 | 2.0 | 8.4 | ns |
| $t_{XZBIDIR}$ | | 10.5 | | 13.4 | ns |
| $t_{ZXBIDIR}$ | | 10.5 | | 13.4 | ns |

**Table 47. EPF10K20 Device External Bidirectional Timing Parameters** *Note (1)*

| Symbol | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 4.6 | | 5.7 | | ns |
| $t_{INHBIDIR}$ | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ | 2.0 | 6.7 | 2.0 | 8.4 | ns |
| $t_{XZBIDIR}$ | | 10.5 | | 13.4 | ns |
| $t_{ZXBIDIR}$ | | 10.5 | | 13.4 | ns |

*Notes to tables:*

(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

*Table 54. EPF10K50 Device Interconnect Timing Microparameters* *Note (1)*

| Symbol | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 8.4 | | 10.2 | ns |
| $t_{DIN2LE}$ | | 3.6 | | 4.8 | ns |
| $t_{DIN2DATA}$ | | 5.5 | | 7.2 | ns |
| $t_{DCLK2IOE}$ | | 4.6 | | 6.2 | ns |
| $t_{DCLK2LE}$ | | 3.6 | | 4.8 | ns |
| $t_{SAMELAB}$ | | 0.3 | | 0.3 | ns |
| $t_{SAMEROW}$ | | 3.3 | | 3.7 | ns |
| $t_{SAMECOLUMN}$ | | 3.9 | | 4.1 | ns |
| $t_{DIFFROW}$ | | 7.2 | | 7.8 | ns |
| $t_{TWOROWS}$ | | 10.5 | | 11.5 | ns |
| $t_{LEPERIPH}$ | | 7.5 | | 8.2 | ns |
| $t_{LABCARRY}$ | | 0.4 | | 0.6 | ns |
| $t_{LABCASC}$ | | 2.4 | | 3.0 | ns |

*Table 55. EPF10K30, EPF10K40 & EPF10K50 Device External Timing Parameters* *Note (1)*

| Symbol | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| $t_{DRR}$ | | 17.2 | | 21.1 | ns |
| $t_{INSU}$ *(2)*, *(3)* | 5.7 | | 6.4 | | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(3)* | 2.0 | 8.8 | 2.0 | 11.2 | ns |

*Table 56. EPF10K30, EPF10K40 & EPF10K50 Device External Bidirectional Timing Parameters* *Note (1)*

| Symbol | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 4.1 | | 4.6 | | ns |
| $t_{INHBIDIR}$ | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ | 2.0 | 8.8 | 2.0 | 11.2 | ns |
| $t_{XZBIDIR}$ | | 12.3 | | 15.0 | ns |
| $t_{ZXBIDIR}$ | | 12.3 | | 15.0 | ns |

*Table 65. EPF10K100 Device IOE Timing Microparameters* *Note (1)*

| Symbol | -3DX Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOC}$ | | 0.5 | | 0.5 | | 0.7 | ns |
| $t_{IOCO}$ | | 0.4 | | 0.4 | | 0.9 | ns |
| $t_{IOCOMB}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOSU}$ | 5.5 | | 5.5 | | 6.7 | | ns |
| $t_{IOH}$ | 0.5 | | 0.5 | | 0.7 | | ns |
| $t_{IOCLR}$ | | 0.7 | | 0.7 | | 1.6 | ns |
| $t_{OD1}$ | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{OD2}$ | | 6.3 | | 6.3 | | 7.3 | ns |
| $t_{OD3}$ | | 7.7 | | 7.7 | | 8.7 | ns |
| $t_{XZ}$ | | 6.2 | | 6.2 | | 6.8 | ns |
| $t_{ZX1}$ | | 6.2 | | 6.2 | | 6.8 | ns |
| $t_{ZX2}$ | | 8.5 | | 8.5 | | 9.1 | ns |
| $t_{ZX3}$ | | 9.9 | | 9.9 | | 10.5 | ns |
| $t_{INREG}$ without ClockLock or ClockBoost circuitry | | 9.0 | | 9.0 | | 10.5 | ns |
| $t_{INREG}$ with ClockLock or ClockBoost circuitry | | 3.0 | | – | | – | ns |
| $t_{IOFD}$ | | 8.1 | | 8.1 | | 10.3 | ns |
| $t_{INCOMB}$ | | 8.1 | | 8.1 | | 10.3 | ns |

*Table 72. EPF10K50V Device IOE Timing Microparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 1.2 | | 1.6 | | 1.9 | | 2.1 | ns |
| $t_{IOC}$ | | 0.3 | | 0.4 | | 0.5 | | 0.5 | ns |
| $t_{IOCO}$ | | 0.3 | | 0.3 | | 0.4 | | 0.4 | ns |
| $t_{IOCOMB}$ | | 0.0 | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOSU}$ | 2.8 | | 2.8 | | 3.4 | | 3.9 | | ns |
| $t_{IOH}$ | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{IOCLR}$ | | 0.5 | | 0.6 | | 0.7 | | 0.7 | ns |
| $t_{OD1}$ | | 2.8 | | 3.2 | | 3.9 | | 4.7 | ns |
| $t_{OD2}$ | | – | | – | | – | | – | ns |
| $t_{OD3}$ | | 6.5 | | 6.9 | | 7.6 | | 8.4 | ns |
| $t_{XZ}$ | | 2.8 | | 3.1 | | 3.8 | | 4.6 | ns |
| $t_{ZX1}$ | | 2.8 | | 3.1 | | 3.8 | | 4.6 | ns |
| $t_{ZX2}$ | | – | | – | | – | | – | ns |
| $t_{ZX3}$ | | 6.5 | | 6.8 | | 7.5 | | 8.3 | ns |
| $t_{INREG}$ | | 5.0 | | 5.7 | | 7.0 | | 9.0 | ns |
| $t_{IOFD}$ | | 1.5 | | 1.9 | | 2.3 | | 2.7 | ns |
| $t_{INCOMB}$ | | 1.5 | | 1.9 | | 2.3 | | 2.7 | ns |

*Table 73. EPF10K50V Device EAB Internal Microparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.7 | | 2.8 | | 3.4 | | 4.6 | ns |
| $t_{EABDATA2}$ | | 4.9 | | 3.9 | | 4.8 | | 5.9 | ns |
| $t_{EABWE1}$ | | 0.0 | | 2.5 | | 3.0 | | 3.7 | ns |
| $t_{EABWE2}$ | | 4.0 | | 4.1 | | 5.0 | | 6.2 | ns |
| $t_{EABCLK}$ | | 0.4 | | 0.8 | | 1.0 | | 1.2 | ns |
| $t_{EABCO}$ | | 0.1 | | 0.2 | | 0.3 | | 0.4 | ns |
| $t_{EABBYPASS}$ | | 0.9 | | 1.1 | | 1.3 | | 1.6 | ns |
| $t_{EABSU}$ | 0.8 | | 1.5 | | 1.8 | | 2.2 | | ns |
| $t_{EABH}$ | 0.8 | | 1.6 | | 2.0 | | 2.5 | | ns |
| $t_{AA}$ | | 5.5 | | 8.2 | | 10.0 | | 12.4 | ns |
| $t_{WP}$ | 6.0 | | 4.9 | | 6.0 | | 7.4 | | ns |
| $t_{WDSU}$ | 0.1 | | 0.8 | | 1.0 | | 1.2 | | ns |
| $t_{WDH}$ | 0.1 | | 0.2 | | 0.3 | | 0.4 | | ns |
| $t_{WASU}$ | 0.1 | | 0.4 | | 0.5 | | 0.6 | | ns |
| $t_{WAH}$ | 0.1 | | 0.8 | | 1.0 | | 1.2 | | ns |
| $t_{WO}$ | | 2.8 | | 4.3 | | 5.3 | | 6.5 | ns |
| $t_{DD}$ | | 2.8 | | 4.3 | | 5.3 | | 6.5 | ns |
| $t_{EABOUT}$ | | 0.5 | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{EABCH}$ | 2.0 | | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{EABCL}$ | 6.0 | | 4.9 | | 6.0 | | 7.4 | | ns |

*Table 86. EPF10K10A Device IOE Timing Microparameters* *Note (1)* *(Part 2 of 2)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOH}$ | 0.8 | | 1.0 | | 1.3 | | ns |
| $t_{IOCLR}$ | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{OD1}$ | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{OD2}$ | | 2.9 | | 3.5 | | 4.7 | ns |
| $t_{OD3}$ | | 6.6 | | 7.8 | | 10.5 | ns |
| $t_{XZ}$ | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{ZX1}$ | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{ZX2}$ | | 2.9 | | 3.5 | | 4.7 | ns |
| $t_{ZX3}$ | | 6.6 | | 7.8 | | 10.5 | ns |
| $t_{INREG}$ | | 5.2 | | 6.3 | | 8.4 | ns |
| $t_{IOFD}$ | | 3.1 | | 3.8 | | 5.0 | ns |
| $t_{INCOMB}$ | | 3.1 | | 3.8 | | 5.0 | ns |

*Table 110. EPF10K250A Device Interconnect Timing Microparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 7.8 | | 8.5 | | 9.4 | ns |
| $t_{DIN2LE}$ | | 2.7 | | 3.1 | | 3.5 | ns |
| $t_{DIN2DATA}$ | | 1.6 | | 1.6 | | 1.7 | ns |
| $t_{DCLK2IOE}$ | | 3.6 | | 4.0 | | 4.6 | ns |
| $t_{DCLK2LE}$ | | 2.7 | | 3.1 | | 3.5 | ns |
| $t_{SAMELAB}$ | | 0.2 | | 0.3 | | 0.3 | ns |
| $t_{SAMEROW}$ | | 6.7 | | 7.3 | | 8.2 | ns |
| $t_{SAMECOLUMN}$ | | 2.5 | | 2.7 | | 3.0 | ns |
| $t_{DIFFROW}$ | | 9.2 | | 10.0 | | 11.2 | ns |
| $t_{TWOROWS}$ | | 15.9 | | 17.3 | | 19.4 | ns |
| $t_{LEPERIPH}$ | | 7.5 | | 8.1 | | 8.9 | ns |
| $t_{LABCARRY}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{LABCASC}$ | | 0.4 | | 0.4 | | 0.5 | ns |

*Table 111. EPF10K250A Device External Reference Timing Parameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 15.0 | | 17.0 | | 20.0 | ns |
| $t_{INSU}$ *(2), (3)* | 6.9 | | 8.0 | | 9.4 | | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(3)* | 2.0 | 8.0 | 2.0 | 8.9 | 2.0 | 10.4 | ns |

*Table 112. EPF10K250A Device External Bidirectional Timing Parameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 9.3 | | 10.6 | | 12.7 | | ns |
| $t_{INHBIDIR}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ | 2.0 | 8.0 | 2.0 | 8.9 | 2.0 | 10.4 | ns |
| $t_{XZBIDIR}$ | | 10.8 | | 12.2 | | 14.2 | ns |
| $t_{ZXBIDIR}$ | | 10.8 | | 12.2 | | 14.2 | ns |

*Table 113. ClockLock & ClockBoost Parameters (Part 2 of 2)*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{CLKDEV1}$ | Input deviation from user specification in MAX+PLUS II (ClockBoost clock multiplication factor equals 1) *(1)* | | | ±1 | MHz |
| $f_{CLKDEV2}$ | Input deviation from user specification in MAX+PLUS II (ClockBoost clock multiplication factor equals 2) *(1)* | | | ±0.5 | MHz |
| $t_{INCLKSTB}$ | Input clock stability (measured between adjacent clocks) | | | 100 | ps |
| $t_{LOCK}$ | Time required for ClockLock or ClockBoost to acquire lock *(2)* | | | 10 | µs |
| $t_{JITTER}$ | Jitter on ClockLock or ClockBoost-generated clock *(3)* | | | 1 | ns |
| $t_{OUTDUTY}$ | Duty cycle for ClockLock or ClockBoost-generated clock | 40 | 50 | 60 | % |

*Notes:*

(1) To implement the ClockLock and ClockBoost circuitry with the MAX+PLUS II software, designers must specify the input frequency. The MAX+PLUS II software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The $f_{CLKDEV}$ parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.

(2) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the $t_{LOCK}$ value is less than the time required for configuration.

(3) The $t_{JITTER}$ specification is measured under long-term observation.

## Power Consumption

The supply power (P) for FLEX 10K devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

Typical $I_{CCSTANDBY}$ values are shown as $I_{CC0}$ in the FLEX 10K device DC operating conditions tables on pages 46, 49, and 52 of this data sheet. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value is calculated based on the amount of current that each LE typically consumes. The $P_{IO}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

Compared to the rest of the device, the embedded array consumes a negligible amount of power. Therefore, the embedded array can be ignored when calculating supply current.

The $I_{CCACTIVE}$ value is calculated with the following equation:

$$I_{CCACTIVE} = K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}} \times \frac{\mu A}{MHz \times LE}$$

The parameters in this equation are shown below:

$\mathbf{f_{MAX}}$ = Maximum operating frequency in MHz
$N$ = Total number of logic cells used in the device
$\mathbf{tog_{LC}}$ = Average percent of logic cells toggling at each clock (typically 12.5%)
$K$ = Constant, shown in Tables 114 and 115

*Table 114. FLEX 10K K Constant Values*

| Device | K Value |
|---|---|
| EPF10K10 | 82 |
| EPF10K20 | 89 |
| EPF10K30 | 88 |
| EPF10K40 | 92 |
| EPF10K50 | 95 |
| EPF10K70 | 85 |
| EPF10K100 | 88 |

*Table 115. FLEX 10KA K Constant Values*

| Device | K Value |
|---|---|
| EPF10K10A | 17 |
| EPF10K30A | 17 |
| EPF10K50V | 19 |
| EPF10K100A | 19 |
| EPF10K130V | 22 |
| EPF10K250A | 23 |

This calculation provides an $I_{CC}$ estimate based on typical conditions with no output load. The actual $I_{CC}$ should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

To better reflect actual designs, the power model (and the constant *K* in the power calculation equations) for continuous interconnect FLEX devices assumes that logic cells drive FastTrack Interconnect channels. In contrast, the power model of segmented FPGAs assumes that all logic cells drive only one short interconnect segment. This assumption may lead to inaccurate results, compared to measured power consumption for an actual design in a segmented interconnect FPGA.

Figure 32 shows the relationship between the current and operating frequency of FLEX 10K devices.