E·XFL

# Intel - EPF10K50RI240-4 Datasheet


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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 360 |
| Number of Logic Elements/Cells | 2880 |
| Total RAM Bits | 20480 |
| Number of I/O | 189 |
| Number of Gates | 116000 |
| Voltage - Supply | 4.5V ~ 5.5V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 240-BFQFP Exposed Pad |
| Supplier Device Package | 240-RQFP (32x32) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epf10k50ri240-4 |

- Flexible interconnect
  - FastTrack® Interconnect continuous routing structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Tri-state emulation that implements internal tri-state buses
  - Up to six global clock signals and four global clear signals
- Powerful I/O pins
  - Individual tri-state output enable control for each pin
  - Open-drain option on each I/O pin
  - Programmable output slew-rate control to reduce switching noise
  - FLEX 10KA devices support hot-socketing
- Peripheral register for fast setup and clock-to-output delay
- Flexible package options
  - Available in a variety of packages with 84 to 600 pins (see Tables 4 and 5)
  - Pin-compatibility with other FLEX 10K devices in the same package
  - FineLine BGA™ packages maximize board space efficiency
- Software design support and automatic place-and-route provided by Altera development systems for Windows-based PCs and Sun SPARCstation, HP 9000 Series 700/800 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), DesignWare components, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, VeriBest, and Viewlogic

The FLEX 10K architecture is similar to that of embedded gate arrays, the fastest-growing segment of the gate array market. As with standard gate arrays, embedded gate arrays implement general logic in a conventional “sea-of-gates” architecture. In addition, embedded gate arrays have dedicated die areas for implementing large, specialized functions. By embedding functions in silicon, embedded gate arrays provide reduced die area and increased speed compared to standard gate arrays. However, embedded megafunctions typically cannot be customized, limiting the designer’s options. In contrast, FLEX 10K devices are programmable, providing the designer with full control over embedded megafunctions and general logic while facilitating iterative design changes during debugging.

Each FLEX 10K device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), microcontroller, wide-data-path manipulation, and data-transformation functions. The logic array performs the same function as the sea-of-gates in the gate array: it is used to implement general logic, such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

FLEX 10K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers the EPC1, EPC2, EPC16, and EPC1441 configuration devices, which configure FLEX 10K devices via a serial data stream. Configuration data can also be downloaded from system RAM or from Altera’s BitBlaster™ serial download cable or ByteBlasterMV™ parallel port download cable. After a FLEX 10K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 320 ms, real-time changes can be made during system operation.

FLEX 10K devices contain an optimized interface that permits microprocessors to configure FLEX 10K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat a FLEX 10K device as memory and configure the device by writing to a virtual memory location, making it very easy for the designer to reconfigure the device.

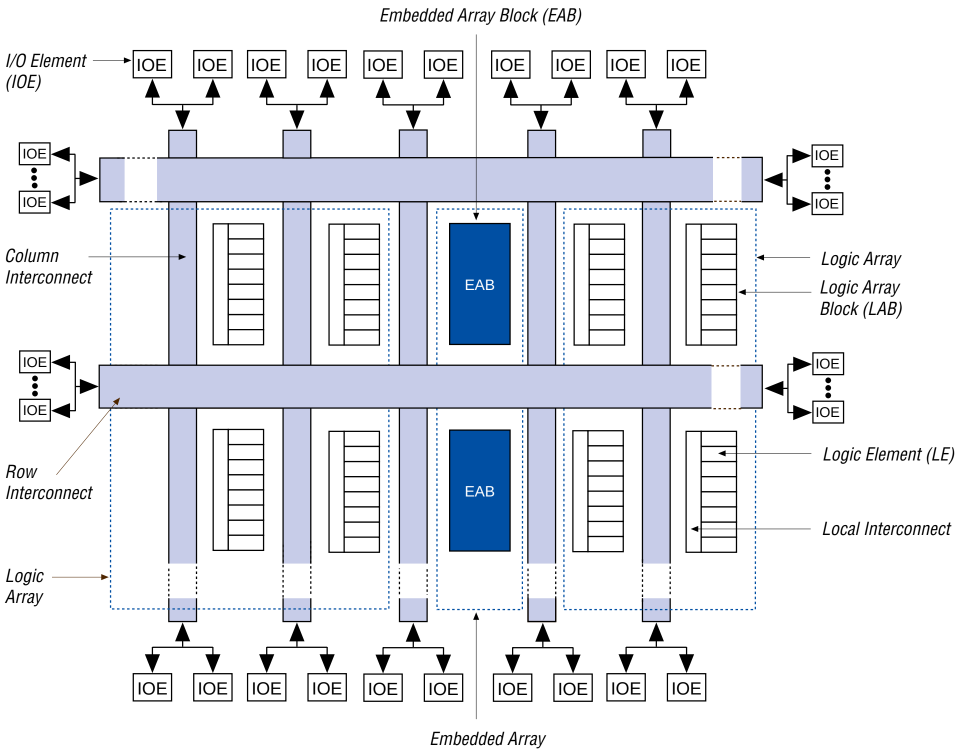
The logic array consists of logic array blocks (LABs). Each LAB contains eight LEs and a local interconnect. An LE consists of a 4-input look-up table (LUT), a programmable flipflop, and dedicated signal paths for carry and cascade functions. The eight LEs can be used to create medium-sized blocks of logic—8-bit counters, address decoders, or state machines—or combined across LABs to create larger logic blocks. Each LAB represents about 96 usable gates of logic.

Signal interconnections within FLEX 10K devices and to and from device pins are provided by the FastTrack Interconnect, a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an output or input register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. As inputs, they provide setup times as low as 1.6 ns and hold times of 0 ns; as outputs, these registers provide clock-to-output times as low as 5.3 ns. IOEs provide a variety of features, such as JTAG BST support, slew-rate control, tri-state buffers, and open-drain outputs.

Figure 1 shows a block diagram of the FLEX 10K architecture. Each group of LEs is combined into an LAB; LABs are arranged into rows and columns. Each row also contains a single EAB. The LABs and EABs are interconnected by the FastTrack Interconnect. IOEs are located at the end of each row and column of the FastTrack Interconnect.

*Figure 1. FLEX 10K Device Block Diagram*



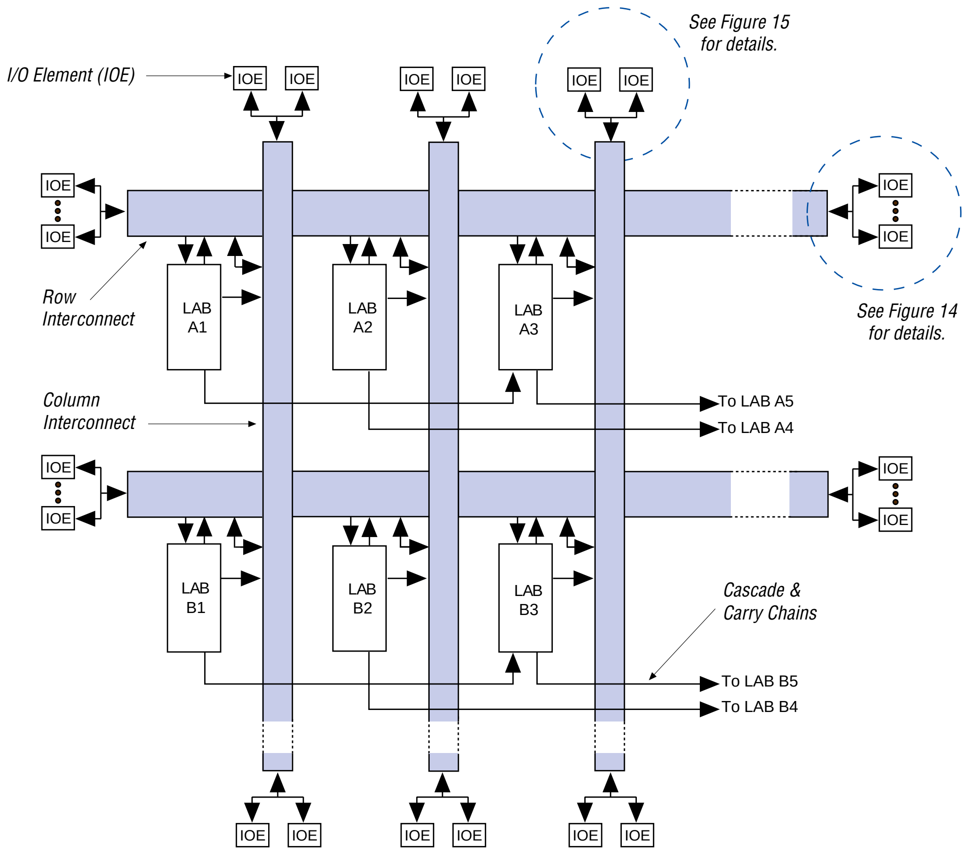

FLEX 10K devices provide six dedicated inputs that drive the flipflops' control inputs to ensure the efficient distribution of high-speed, low-skew (less than 1.5 ns) control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

## Embedded Array Block

The EAB is a flexible block of RAM with registers on the input and output ports, and is used to implement common gate array megafunctions. The EAB is also suitable for functions such as multipliers, vector scalars, and error correction circuits, because it is large and flexible. These functions can be combined in applications such as digital filters and microcontrollers.

Figure 12 shows the interconnection of adjacent LABs and EABs with row, column, and local interconnects, as well as the associated cascade and carry chains. Each LAB is labeled according to its location: a letter represents the row and a number represents the column. For example, LAB B3 is in row B, column 3.

***Figure 12. Interconnect Resources***



## ClockLock & ClockBoost Features

To support high-speed designs, selected FLEX 10K devices offer optional ClockLock and ClockBoost circuitry containing a phase-locked loop (PLL) that is used to increase design speed and reduce resource usage. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost feature allows the designer to distribute a low-speed clock and multiply that clock on-device. Combined, the ClockLock and ClockBoost features provide significant improvements in system performance and bandwidth.

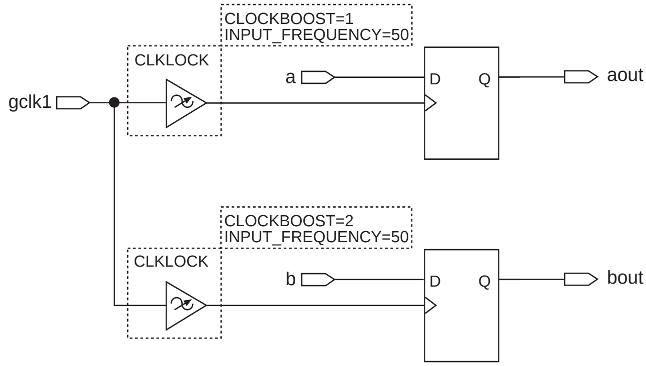
The ClockLock and ClockBoost features in FLEX 10K devices are enabled through the Altera software. External devices are not required to use these features. The output of the ClockLock and ClockBoost circuits is not available at any of the device pins.

The ClockLock and ClockBoost circuitry locks onto the rising edge of the incoming clock. The circuit output can only drive the clock inputs of registers; the generated clock cannot be gated or inverted.

The dedicated clock pin (`GCLK1`) supplies the clock to the ClockLock and ClockBoost circuitry. When the dedicated clock pin is driving the ClockLock or ClockBoost circuitry, it cannot drive elsewhere in the device.

In designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to `GCLK1`. With the Altera software, `GCLK1` can feed both the ClockLock and ClockBoost circuitry in the FLEX 10K device. However, when both circuits are used, the other clock pin (`GCLK0`) cannot be used. Figure 17 shows a block diagram of how to enable both the ClockLock and ClockBoost circuits in the Altera software. The example shown is a schematic, but a similar approach applies for designs created in AHDL, VHDL, and Verilog HDL. When the ClockLock and ClockBoost circuits are used simultaneously, the input frequency parameter must be the same for both circuits. In Figure 17, the input frequency must meet the requirements specified when the ClockBoost multiplication factor is two.

*Figure 17. Enabling ClockLock & ClockBoost in the Same Design*




To use both the ClockLock and ClockBoost circuits in the same design, designers must use Revision C EPF10K100GC503-3DX devices and MAX+PLUS II software versions 7.2 or higher. The die revision is indicated by the third digit of the nine-digit code on the top side of the device.

## Output Configuration

This section discusses the peripheral component interconnect (PCI) pull-up clamping diode option, slew-rate control, open-drain output option, MultiVolt I/O interface, and power sequencing for FLEX 10K devices. The PCI pull-up clamping diode, slew-rate control, and open-drain output options are controlled pin-by-pin via Altera logic options. The MultiVolt I/O interface is controlled by connecting $V_{CCIO}$ to a different voltage than $V_{CCINT}$. Its effect can be simulated in the Altera software via the **Global Project Device Options** dialog box (Assign menu).

### PCI Clamping Diodes

The EPF10K10A and EPF10K30A devices have a pull-up clamping diode on every I/O, dedicated input, and dedicated clock pin. PCI clamping diodes clamp the transient overshoot caused by reflected waves to the $V_{CCIO}$ value and are required for 3.3-V PCI compliance. Clamping diodes can also be used to limit overshoot in other systems.

Clamping diodes are controlled on a pin-by-pin basis via a logic option in the Altera software. When $V_{CCIO}$ is 3.3 V, a pin that has the clamping diode turned on can be driven by a 2.5-V or 3.3-V signal, but not a 5.0-V signal. When $V_{CCIO}$ is 2.5 V, a pin that has the clamping diode turned on can be driven by a 2.5-V signal, but not a 3.3-V or 5.0-V signal. However, a clamping diode can be turned on for a subset of pins, which allows devices to bridge between a 3.3-V PCI bus and a 5.0-V device.

## Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces system noise and adds a maximum delay of approximately 2.9 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a device-wide basis. The slow slew rate setting affects only the falling edge of the output.

## Open-Drain Output Option

FLEX 10K devices provide an optional open-drain (electrically equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane. Additionally, the Altera software can convert tri-state buffers with grounded data inputs to open-drain pins automatically.

Open-drain output pins on FLEX 10K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a $V_{IH}$ of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The $I_{OL}$ current specification should be considered when selecting a pull-up resistor.

Output pins on 5.0-V FLEX 10K devices with $V_{CCIO}$ = 3.3 V or 5.0 V (with a pull-up resistor to the 5.0-V supply) can also drive 5.0-V CMOS input pins. In this case, the pull-up transistor will turn off when the pin voltage exceeds 3.3 V. Therefore, the pin does not have to be open-drain.

## MultiVolt I/O Interface

The FLEX 10K device architecture supports the MultiVolt I/O interface feature, which allows FLEX 10K devices to interface with systems of differing supply voltages. These devices have one set of $V_{CC}$ pins for internal operation and input buffers (VCCINT) and another set for I/O output drivers (VCCIO).

Figure 18 shows the timing requirements for the JTAG signals.

*Figure 18. JTAG Waveforms*

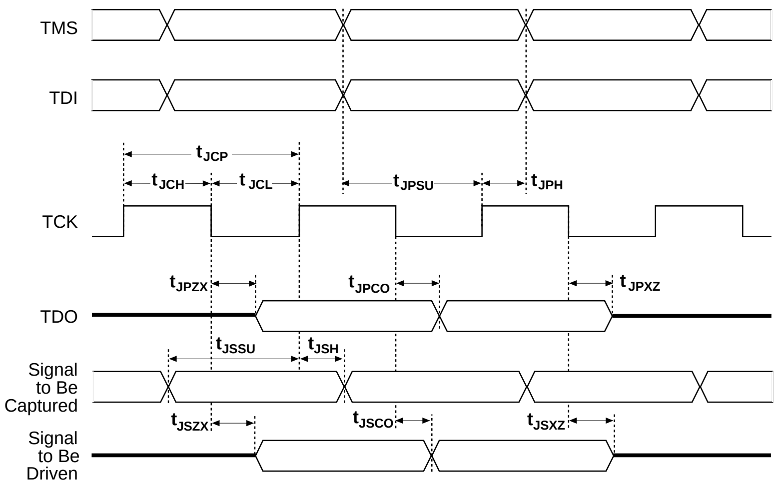
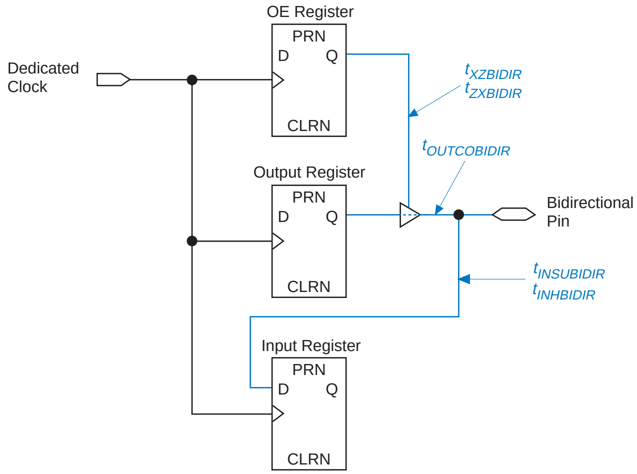



Table 16 shows the timing parameters and values for FLEX 10K devices.

*Table 16. JTAG Timing Parameters & Values*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 100 | | ns |
| $t_{JCH}$ | TCK clock high time | 50 | | ns |
| $t_{JCL}$ | TCK clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 35 | ns |
| $t_{JSZX}$ | Update register high-impedance to valid output | | 35 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 35 | ns |

*Figure 28. Synchronous Bidirectional Pin External Timing Model*




Tables 32 through 36 describe the FLEX 10K device internal timing parameters. These internal timing parameters are expressed as worst-case values. Using hand calculations, these parameters can be used to estimate design performance. However, before committing designs to silicon, actual worst-case performance should be modeled using timing simulation and analysis. Tables 37 through 38 describe FLEX 10K external timing parameters.

*Table 32. LE Timing Microparameters (Part 1 of 2)* Note (1)

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{LUT}$ | LUT delay for data-in | |
| $t_{CLUT}$ | LUT delay for carry-in | |
| $t_{RLUT}$ | LUT delay for LE register feedback | |
| $t_{PACKED}$ | Data-in to packed register delay | |
| $t_{EN}$ | LE register enable delay | |
| $t_{CICO}$ | Carry-in to carry-out delay | |
| $t_{CGEN}$ | Data-in to carry-out delay | |
| $t_{CGENR}$ | LE register feedback to carry-out delay | |
| $t_{CASC}$ | Cascade-in to cascade-out delay | |
| $t_{C}$ | LE register control signal delay | |
| $t_{CO}$ | LE register clock-to-output delay | |
| $t_{COMB}$ | Combinatorial delay | |

**Table 36. Interconnect Timing Microparameters** *Note (1)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{DIN2IOE}$ | Delay from dedicated input pin to IOE control input | (7) |
| $t_{DCLK2LE}$ | Delay from dedicated clock pin to LE or EAB clock | (7) |
| $t_{DIN2DATA}$ | Delay from dedicated input or clock to LE or EAB data | (7) |
| $t_{DCLK2IOE}$ | Delay from dedicated clock pin to IOE clock | (7) |
| $t_{DIN2LE}$ | Delay from dedicated input pin to LE or EAB control input | (7) |
| $t_{SAMELAB}$ | Routing delay for an LE driving another LE in the same LAB | |
| $t_{SAMEROW}$ | Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row | (7) |
| $t_{SAMECOLUMN}$ | Routing delay for an LE driving an IOE in the same column | (7) |
| $t_{DIFFROW}$ | Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row | (7) |
| $t_{TWOROWS}$ | Routing delay for a row IOE or EAB driving an LE or EAB in a different row | (7) |
| $t_{LEPERIPH}$ | Routing delay for an LE driving a control signal of an IOE via the peripheral control bus | (7) |
| $t_{LABCARRY}$ | Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB | |
| $t_{LABCASC}$ | Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB | |

**Table 37. External Timing Parameters** *Notes (8), (10)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{DRR}$ | Register-to-register delay via four LEs, three row interconnects, and four local interconnects | (9) |
| $t_{INSU}$ | Setup time with global clock at IOE register | |
| $t_{INH}$ | Hold time with global clock at IOE register | |
| $t_{OUTCO}$ | Clock-to-output delay with global clock at IOE register | |

**Table 38. External Bidirectional Timing Parameters** *Note (10)*

| Symbol | Parameter | Condition |
|---|---|---|
| $t_{INSUBIDIR}$ | Setup time for bidirectional pins with global clock at adjacent LE register | |
| $t_{INHBIDIR}$ | Hold time for bidirectional pins with global clock at adjacent LE register | |
| $t_{OUTCOBIDIR}$ | Clock-to-output delay for bidirectional pins with global clock at IOE register | |
| $t_{XZBIDIR}$ | Synchronous IOE output buffer disable delay | |
| $t_{ZXBIDIR}$ | Synchronous IOE output buffer enable delay, slow slew rate = off | |

*Notes to tables:*

(1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.

(2) Operating conditions: $V_{CCIO}$ = 5.0 V ± 5% for commercial use in FLEX 10K devices.
$V_{CCIO}$ = 5.0 V ± 10% for industrial use in FLEX 10K devices.
$V_{CCIO}$ = 3.3 V ± 10% for commercial or industrial use in FLEX 10KA devices.

(3) Operating conditions: $V_{CCIO}$ = 3.3 V ± 10% for commercial or industrial use in FLEX 10K devices.
$V_{CCIO}$ = 2.5 V ± 0.2 V for commercial or industrial use in FLEX 10KA devices.

(4) Operating conditions: $V_{CCIO}$ = 2.5 V, 3.3 V, or 5.0 V.

(5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the `WE` signal is registered.

(6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.

(7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.

(8) External reference timing parameters are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.

(9) Contact Altera Applications for test circuit specifications and test conditions.

(10) These timing parameters are sample-tested only.

Figures 29 and 30 show the asynchronous and synchronous timing waveforms, respectively, for the EAB macroparameters in Table 34.

*Figure 29. EAB Asynchronous Timing Waveforms*

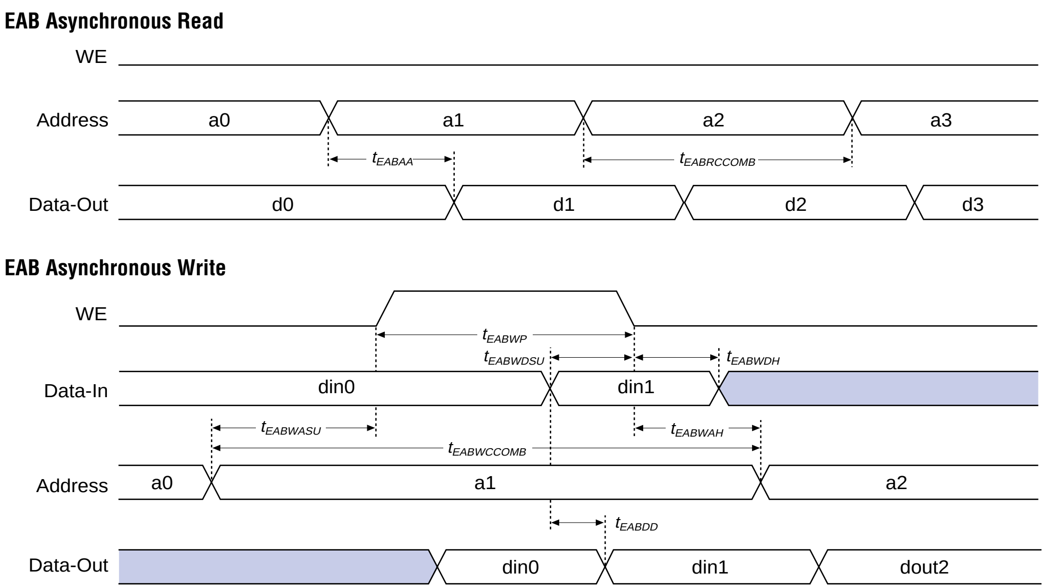


**Table 49. EPF10K30, EPF10K40 & EPF10K50 Device IOE Timing Microparameters** *Note (1)*

| Symbol | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| $t_{IOD}$ | | 0.4 | | 0.6 | ns |
| $t_{IOC}$ | | 0.5 | | 0.9 | ns |
| $t_{IOCO}$ | | 0.4 | | 0.5 | ns |
| $t_{IOCOMB}$ | | 0.0 | | 0.0 | ns |
| $t_{IOSU}$ | 3.1 | | 3.5 | | ns |
| $t_{IOH}$ | 1.0 | | 1.9 | | ns |
| $t_{IOCLR}$ | | 1.0 | | 1.2 | ns |
| $t_{OD1}$ | | 3.3 | | 3.6 | ns |
| $t_{OD2}$ | | 5.6 | | 6.5 | ns |
| $t_{OD3}$ | | 7.0 | | 8.3 | ns |
| $t_{XZ}$ | | 5.2 | | 5.5 | ns |
| $t_{ZX1}$ | | 5.2 | | 5.5 | ns |
| $t_{ZX2}$ | | 7.5 | | 8.4 | ns |
| $t_{ZX3}$ | | 8.9 | | 10.2 | ns |
| $t_{INREG}$ | | 7.7 | | 10.0 | ns |
| $t_{IOFD}$ | | 3.3 | | 4.0 | ns |
| $t_{INCOMB}$ | | 3.3 | | 4.0 | ns |

Tables 71 through 77 show EPF10K50V device internal and external timing parameters.

**Table 71. EPF10K50V Device LE Timing Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.9 | | 1.0 | | 1.3 | | 1.6 | ns |
| $t_{CLUT}$ | | 0.1 | | 0.5 | | 0.6 | | 0.6 | ns |
| $t_{RLUT}$ | | 0.5 | | 0.8 | | 0.9 | | 1.0 | ns |
| $t_{PACKED}$ | | 0.4 | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{EN}$ | | 0.7 | | 0.9 | | 1.1 | | 1.4 | ns |
| $t_{CICO}$ | | 0.2 | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{CGEN}$ | | 0.8 | | 0.7 | | 0.8 | | 1.2 | ns |
| $t_{CGENR}$ | | 0.4 | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{CASC}$ | | 0.7 | | 0.7 | | 0.8 | | 0.9 | ns |
| $t_{C}$ | | 0.3 | | 1.0 | | 1.3 | | 1.5 | ns |
| $t_{CO}$ | | 0.5 | | 0.7 | | 0.9 | | 1.0 | ns |
| $t_{COMB}$ | | 0.4 | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{SU}$ | 0.8 | | 1.6 | | 2.2 | | 2.5 | | ns |
| $t_{H}$ | 0.5 | | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{PRE}$ | | 0.8 | | 0.4 | | 0.5 | | 0.5 | ns |
| $t_{CLR}$ | | 0.8 | | 0.4 | | 0.5 | | 0.5 | ns |
| $t_{CH}$ | 2.0 | | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | 2.0 | | 4.0 | | 4.0 | | 4.0 | | ns |

| *Table 72. EPF10K50V Device IOE Timing Microparameters* Note (1) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 1.2 | | 1.6 | | 1.9 | | 2.1 | ns |
| $t_{IOC}$ | | 0.3 | | 0.4 | | 0.5 | | 0.5 | ns |
| $t_{IOCO}$ | | 0.3 | | 0.3 | | 0.4 | | 0.4 | ns |
| $t_{IOCOMB}$ | | 0.0 | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOSU}$ | 2.8 | | 2.8 | | 3.4 | | 3.9 | | ns |
| $t_{IOH}$ | 0.7 | | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{IOCLR}$ | | 0.5 | | 0.6 | | 0.7 | | 0.7 | ns |
| $t_{OD1}$ | | 2.8 | | 3.2 | | 3.9 | | 4.7 | ns |
| $t_{OD2}$ | | – | | – | | – | | – | ns |
| $t_{OD3}$ | | 6.5 | | 6.9 | | 7.6 | | 8.4 | ns |
| $t_{XZ}$ | | 2.8 | | 3.1 | | 3.8 | | 4.6 | ns |
| $t_{ZX1}$ | | 2.8 | | 3.1 | | 3.8 | | 4.6 | ns |
| $t_{ZX2}$ | | – | | – | | – | | – | ns |
| $t_{ZX3}$ | | 6.5 | | 6.8 | | 7.5 | | 8.3 | ns |
| $t_{INREG}$ | | 5.0 | | 5.7 | | 7.0 | | 9.0 | ns |
| $t_{IOFD}$ | | 1.5 | | 1.9 | | 2.3 | | 2.7 | ns |
| $t_{INCOMB}$ | | 1.5 | | 1.9 | | 2.3 | | 2.7 | ns |

*Notes to tables:*
(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Tables 85 through 91 show EPF10K10A device internal and external timing parameters.

**Table 85. EPF10K10A Device LE Timing Microparameters** Note (1)

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.9 | | 1.2 | | 1.6 | ns |
| $t_{CLUT}$ | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{RLUT}$ | | 1.9 | | 2.3 | | 3.0 | ns |
| $t_{PACKED}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{EN}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{CICO}$ | | 02 | | 0.3 | | 0.4 | ns |
| $t_{CGEN}$ | | 0.7 | | 0.9 | | 1.1 | ns |
| $t_{CGENR}$ | | 0.7 | | 0.9 | | 1.1 | ns |
| $t_{CASC}$ | | 1.0 | | 1.2 | | 1.7 | ns |
| $t_C$ | | 1.2 | | 1.4 | | 1.9 | ns |
| $t_{CO}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{COMB}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{SU}$ | 1.1 | | 1.3 | | 1.7 | | ns |
| $t_H$ | 0.6 | | 0.7 | | 0.9 | | ns |
| $t_{PRE}$ | | 0.5 | | 0.6 | | 0.9 | ns |
| $t_{CLR}$ | | 0.5 | | 0.6 | | 0.9 | ns |
| $t_{CH}$ | 3.0 | | 3.5 | | 4.0 | | ns |
| $t_{CL}$ | 3.0 | | 3.5 | | 4.0 | | ns |

**Table 86. EPF10K10A Device IOE Timing Microparameters** Note (1) **(Part 1 of 2)**

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| | | 1.3 | | 1.5 | | 2.0 | ns |
| $t_{IOC}$ | | 0.2 | | 0.3 | | 0.3 | ns |
| $t_{IOCO}$ | | 0.2 | | 0.3 | | 0.4 | ns |
| $t_{IOCOMB}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{IOSU}$ | 0.8 | | 1.0 | | 1.3 | | ns |

| *Table 94. EPF10K30A Device EAB Internal Microparameters* Note (1) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **-1 Speed Grade** | | **-2 Speed Grade** | | **-3 Speed Grade** | | **Unit** |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{EABDATA1}$ | | 5.5 | | 6.5 | | 8.5 | ns |
| $t_{EABDATA2}$ | | 1.1 | | 1.3 | | 1.8 | ns |
| $t_{EABWE1}$ | | 2.4 | | 2.8 | | 3.7 | ns |
| $t_{EABWE2}$ | | 2.1 | | 2.5 | | 3.2 | ns |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.2 | ns |
| $t_{EABCO}$ | | 1.7 | | 2.0 | | 2.6 | ns |
| $t_{EABBYPASS}$ | | 0.0 | | 0.0 | | 0.3 | ns |
| $t_{EABSU}$ | 1.2 | | 1.4 | | 1.9 | | ns |
| $t_{EABH}$ | 0.1 | | 0.1 | | 0.3 | | ns |
| $t_{AA}$ | | 4.2 | | 5.0 | | 6.5 | ns |
| $t_{WP}$ | 3.8 | | 4.5 | | 5.9 | | ns |
| $t_{WDSU}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{WDH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{WASU}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{WAH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{WO}$ | | 3.7 | | 4.4 | | 6.4 | ns |
| $t_{DD}$ | | 3.7 | | 4.4 | | 6.4 | ns |
| $t_{EABOUT}$ | | 0.0 | | 0.1 | | 0.6 | ns |
| $t_{EABCH}$ | 3.0 | | 3.5 | | 4.0 | | ns |
| $t_{EABCL}$ | 3.8 | | 4.5 | | 5.9 | | ns |

| *Table 107. EPF10K250A Device IOE Timing Microparameters* Note (1) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **-1 Speed Grade** | | **-2 Speed Grade** | | **-3 Speed Grade** | | **Unit** |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{IOD}$ | | 1.2 | | 1.3 | | 1.6 | ns |
| $t_{IOC}$ | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{IOCO}$ | | 0.8 | | 0.9 | | 1.1 | ns |
| $t_{IOCOMB}$ | | 0.7 | | 0.7 | | 0.8 | ns |
| $t_{IOSU}$ | 2.7 | | 3.1 | | 3.6 | | ns |
| $t_{IOH}$ | 0.2 | | 0.3 | | 0.3 | | ns |
| $t_{IOCLR}$ | | 1.2 | | 1.3 | | 1.6 | ns |
| $t_{OD1}$ | | 3.2 | | 3.6 | | 4.2 | ns |
| $t_{OD2}$ | | 5.9 | | 6.7 | | 7.8 | ns |
| $t_{OD3}$ | | 8.7 | | 9.8 | | 11.5 | ns |
| $t_{XZ}$ | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{ZX1}$ | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{ZX2}$ | | 6.5 | | 7.4 | | 8.6 | ns |
| $t_{ZX3}$ | | 9.3 | | 10.5 | | 12.3 | ns |
| $t_{INREG}$ | | 8.2 | | 9.3 | | 10.9 | ns |
| $t_{IOFD}$ | | 9.0 | | 10.2 | | 12.0 | ns |
| $t_{INCOMB}$ | | 9.0 | | 10.2 | | 12.0 | ns |

Multiple FLEX 10K devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

*Table 116. Data Sources for Configuration*

| Configuration Scheme | Data Source |
|---|---|
| Configuration device | EPC1, EPC2, EPC16, or EPC1441 configuration device |
| Passive serial (PS) | BitBlaster, MasterBlaster, or ByteBlasterMV download cable, or serial data source |
| Passive parallel asynchronous (PPA) | Parallel data source |
| Passive parallel synchronous (PPS) | Parallel data source |
| JTAG | BitBlaster, MasterBlaster, or ByteBlasterMV download cable, or microprocessor with Jam STAPL file or Jam Byte-Code file |

## Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the Altera Digital Library for pin-out information.

## Revision History

The information contained in the *FLEX 10K Embedded Programmable Logic Device Family Data Sheet* version 4.2 supersedes information published in previous versions.

### Version 4.2 Changes

The following change was made to version 4.2 of the *FLEX 10K Embedded Programmable Logic Device Family Data Sheet*: updated Figure 13.

### Version 4.1 Changes

The following changes were made to version 4.1 of the *FLEX 10K Embedded Programmable Logic Device Family Data Sheet*.

- Updated General Description section
- Updated I/O Element section
- Updated SameFrame Pin-Outs section
- Updated Figure 16
- Updated Tables 13 and 116
- Added Note 9 to Table 19
- Added Note 10 to Table 24
- Added Note 10 to Table 28

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