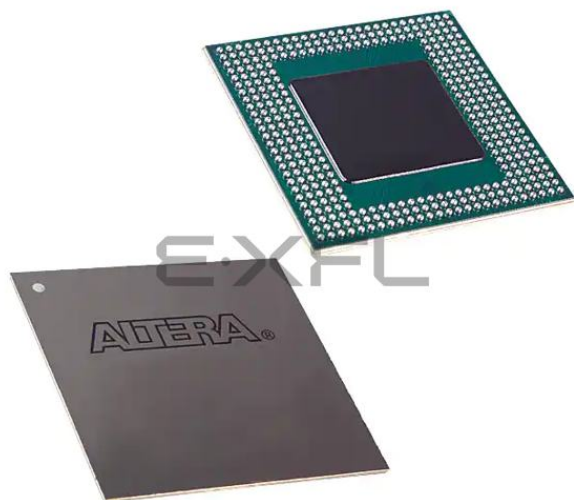




Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                       |
|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                              |
| Number of LABs/CLBs            | 360                                                                                                                                   |
| Number of Logic Elements/Cells | 2880                                                                                                                                  |
| Total RAM Bits                 | 20480                                                                                                                                 |
| Number of I/O                  | 274                                                                                                                                   |
| Number of Gates                | 116000                                                                                                                                |
| Voltage - Supply               | 3V ~ 3.6V                                                                                                                             |
| Mounting Type                  | Surface Mount                                                                                                                         |
| Operating Temperature          | 0°C ~ 70°C (TA)                                                                                                                       |
| Package / Case                 | 356-LBGA                                                                                                                              |
| Supplier Device Package        | 356-BGA (35x35)                                                                                                                       |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/intel/epf10k50vbc356-1">https://www.e-xfl.com/product-detail/intel/epf10k50vbc356-1</a> |

The logic array consists of logic array blocks (LABs). Each LAB contains eight LEs and a local interconnect. An LE consists of a 4-input look-up table (LUT), a programmable flipflop, and dedicated signal paths for carry and cascade functions. The eight LEs can be used to create medium-sized blocks of logic—8-bit counters, address decoders, or state machines—or combined across LABs to create larger logic blocks. Each LAB represents about 96 usable gates of logic.

Signal interconnections within FLEX 10K devices and to and from device pins are provided by the FastTrack Interconnect, a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an output or input register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. As inputs, they provide setup times as low as 1.6 ns and hold times of 0 ns; as outputs, these registers provide clock-to-output times as low as 5.3 ns. IOEs provide a variety of features, such as JTAG BST support, slew-rate control, tri-state buffers, and open-drain outputs.

**Figure 1** shows a block diagram of the FLEX 10K architecture. Each group of LEs is combined into an LAB; LABs are arranged into rows and columns. Each row also contains a single EAB. The LABs and EABs are interconnected by the FastTrack Interconnect. IOEs are located at the end of each row and column of the FastTrack Interconnect.

The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the flipflop is bypassed and the output of the LUT drives the output of the LE.

The LE has two outputs that drive the interconnect; one drives the local interconnect and the other drives either the row or column FastTrack Interconnect. The two outputs can be controlled independently. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, can improve LE utilization because the register and the LUT can be used for unrelated functions.

The FLEX 10K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. The carry chain supports high-speed counters and adders; the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in an LAB and all LABs in the same row. Intensive use of carry and cascade chains can reduce routing flexibility. Therefore, the use of these chains should be limited to speed-critical portions of a design.

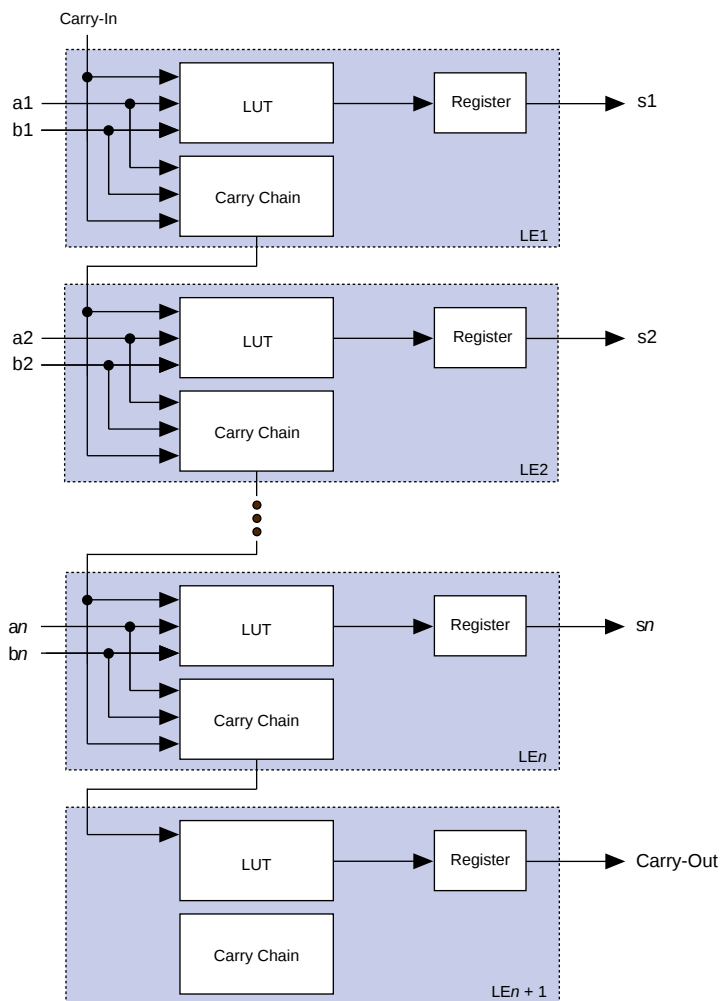
### *Carry Chain*

The carry chain provides a very fast (as low as 0.2 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 10K architecture to implement high-speed counters, adders, and comparators of arbitrary width efficiently. Carry chain logic can be created automatically by the Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of carry chains.

Carry chains longer than eight LEs are automatically implemented by linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a row. A carry chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB. For example, the last LE of the first LAB in a row carries to the first LE of the third LAB in the row. The carry chain does not cross the EAB at the middle of the row. For instance, in the EPF10K50 device, the carry chain stops at the eighteenth LAB and a new one begins at the nineteenth LAB.

Figure 7 shows how an  $n$ -bit full adder can be implemented in  $n + 1$  LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can either be bypassed for simple adders or be used for an accumulator function. The carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal.

**Figure 7. Carry Chain Operation ( $n$ -bit Full Adder)**



### **Up/Down Counter Mode**

The up/down counter mode offers counter enable, clock enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. The Up/down counter mode uses 2 three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the clear and preset register control signals, without using the LUT resources.

### **Clearable Counter Mode**

The clearable counter mode is similar to the up/down counter mode, but supports a synchronous clear instead of the up/down control. The clear function is substituted for the cascade-in signal in the up/down counter mode. Clearable counter mode uses 2 three-input LUTs: one generates the counter data, and the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer. The output of this multiplexer is ANDed with a synchronous clear signal.

### *Internal Tri-State Emulation*

Internal tri-state emulation provides internal tri-stating without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The Altera software automatically implements tri-state bus functionality with a multiplexer.

### *Clear & Preset Logic Control*

Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE asynchronously loads signals into a register. Either LABCTRL1 or LABCTRL2 can control the asynchronous clear. Alternatively, the register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

### **Asynchronous Preset**

An asynchronous preset is implemented as either an asynchronous load, or with an asynchronous clear. If DATA3 is tied to  $V_{CC}$ , asserting LABCTRL1 asynchronously loads a one into the register. Alternatively, the Altera software can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

### **Asynchronous Preset & Clear**

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. DATA3 is tied to  $V_{CC}$ , therefore, asserting LABCTRL1 asynchronously loads a one into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

### **Asynchronous Load with Clear**

When implementing an asynchronous load in conjunction with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear; LABCTRL2 does not have to feed the preset circuits.

### **Asynchronous Load with Preset**

When implementing an asynchronous load in conjunction with preset, the Altera software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 presets the register, while asserting LABCTRL1 loads the register. The Altera software inverts the signal that drives DATA3 to account for the inversion of the register's output.

### **Asynchronous Load without Preset or Clear**

When implementing an asynchronous load without preset or clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

**Table 13. FLEX 10K JTAG Instructions**

| JTAG Instruction | Description                                                                                                                                                                                                                           |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SAMPLE/PRELOAD   | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.                                                            |
| EXTEST           | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.                                                                |
| BYPASS           | Places the 1-bit bypass register between the TDI and TD0 pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.                                          |
| USERCODE         | Selects the user electronic signature (USERCODE) register and places it between the TDI and TD0 pins, allowing the USERCODE to be serially shifted out of TD0.                                                                        |
| IDCODE           | Selects the IDCODE register and places it between TDI and TD0, allowing the IDCODE to be serially shifted out of TD0.                                                                                                                 |
| ICR Instructions | These instructions are used when configuring a FLEX 10K device via JTAG ports with a BitBlaster, or ByteBlasterMV or MasterBlaster download cable, or using a Jam File (.jam) or Jam Byte-Code File (.jbc) via an embedded processor. |

The instruction register length of FLEX 10K devices is 10 bits. The USERCODE register length in FLEX 10K devices is 32 bits; 7 bits are determined by the user, and 25 bits are predetermined. [Tables 14 and 15](#) show the boundary-scan register length and device IDCODE information for FLEX 10K devices.

**Table 14. FLEX 10K Boundary-Scan Register Length**

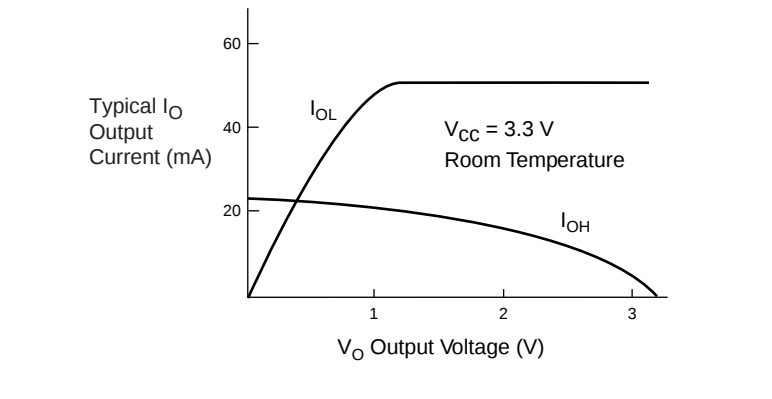
| Device                | Boundary-Scan Register Length |
|-----------------------|-------------------------------|
| EPF10K10, EPF10K10A   | 480                           |
| EPF10K20              | 624                           |
| EPF10K30, EPF10K30A   | 768                           |
| EPF10K40              | 864                           |
| EPF10K50, EPF10K50V   | 960                           |
| EPF10K70              | 1,104                         |
| EPF10K100, EPF10K100A | 1,248                         |
| EPF10K130V            | 1,440                         |
| EPF10K250A            | 1,440                         |

**Table 18. FLEX 10K 5.0-V Device Recommended Operating Conditions**

| Symbol      | Parameter                                           | Conditions         | Min         | Max               | Unit |
|-------------|-----------------------------------------------------|--------------------|-------------|-------------------|------|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | (3), (4)           | 4.75 (4.50) | 5.25 (5.50)       | V    |
| $V_{CCIO}$  | Supply voltage for output buffers, 5.0-V operation  | (3), (4)           | 4.75 (4.50) | 5.25 (5.50)       | V    |
|             | Supply voltage for output buffers, 3.3-V operation  | (3), (4)           | 3.00 (3.00) | 3.60 (3.60)       | V    |
| $V_I$       | Input voltage                                       |                    | −0.5        | $V_{CCINT} + 0.5$ | V    |
| $V_O$       | Output voltage                                      |                    | 0           | $V_{CCIO}$        | V    |
| $T_A$       | Ambient temperature                                 | For commercial use | 0           | 70                | ° C  |
|             |                                                     | For industrial use | −40         | 85                | ° C  |
| $T_J$       | Operating temperature                               | For commercial use | 0           | 85                | ° C  |
|             |                                                     | For industrial use | −40         | 100               | ° C  |
| $t_R$       | Input rise time                                     |                    |             | 40                | ns   |
| $t_F$       | Input fall time                                     |                    |             | 40                | ns   |

Figure 21 shows the typical output drive characteristics of EPF10K50V and EPF10K130V devices.

Figure 21. Output Drive Characteristics of EPF10K50V & EPF10K130V Devices



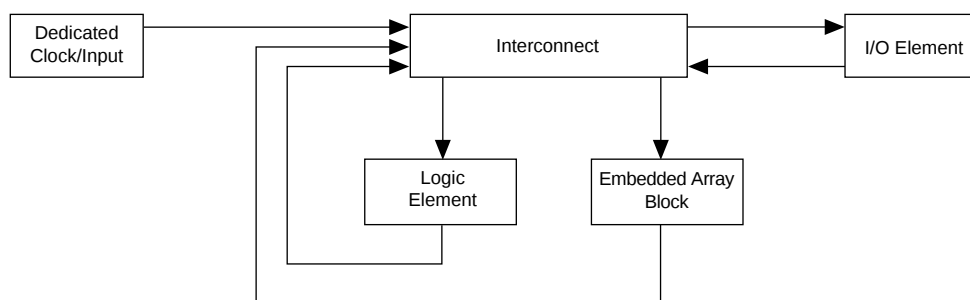
Tables 26 through 31 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 3.3-V FLEX 10K devices.

| Table 26. FLEX 10KA 3.3-V Device Absolute Maximum Ratings <span>Note (1)</span> |                            |                                                |      |      |      |
|---------------------------------------------------------------------------------|----------------------------|------------------------------------------------|------|------|------|
| Symbol                                                                          | Parameter                  | Conditions                                     | Min  | Max  | Unit |
| $V_{CC}$                                                                        | Supply voltage             | With respect to ground (2)                     | -0.5 | 4.6  | V    |
| $V_I$                                                                           | DC input voltage           |                                                | -2.0 | 5.75 | V    |
| $I_{OUT}$                                                                       | DC output current, per pin |                                                | -25  | 25   | mA   |
| $T_{STG}$                                                                       | Storage temperature        | No bias                                        | -65  | 150  | ° C  |
| $T_{AMB}$                                                                       | Ambient temperature        | Under bias                                     | -65  | 135  | ° C  |
| $T_J$                                                                           | Junction temperature       | Ceramic packages, under bias                   |      | 150  | ° C  |
|                                                                                 |                            | PQFP, TQFP, RQFP, and BGA packages, under bias |      | 135  | ° C  |

Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

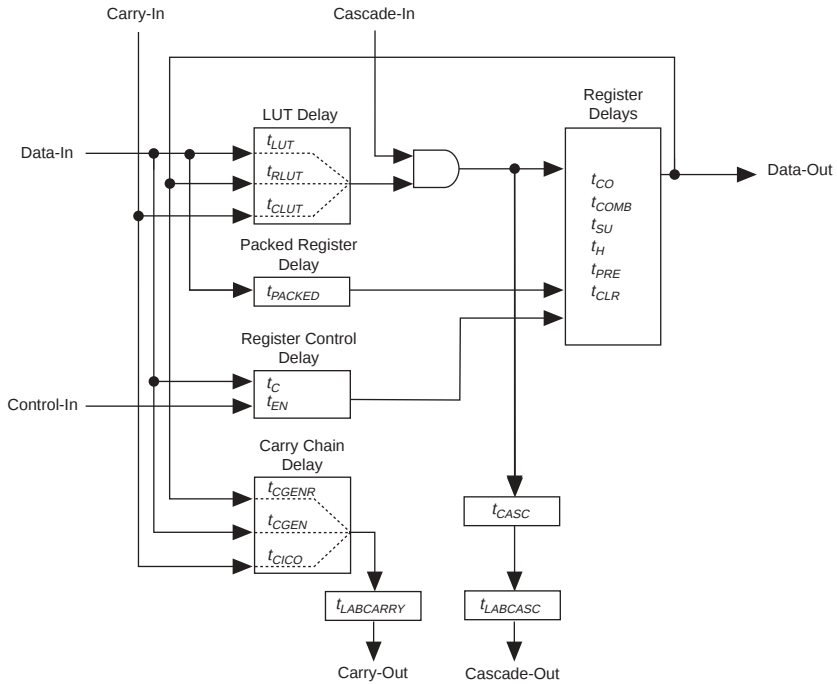
Figure 24 shows the overall timing model, which maps the possible paths to and from the various elements of the FLEX 10K device.

**Figure 24. FLEX 10K Device Timing Model**



Figures 25 through 27 show the delays that correspond to various paths and functions within the LE, IOE, and EAB timing models.

**Figure 25. FLEX 10K Device LE Timing Model**



**Table 35. EAB Timing Macroparameters** *Notes (1), (6)*

| Symbol          | Parameter                                                                               | Conditions |
|-----------------|-----------------------------------------------------------------------------------------|------------|
| $t_{EABAA}$     | EAB address access delay                                                                |            |
| $t_{EABRCCOMB}$ | EAB asynchronous read cycle time                                                        |            |
| $t_{EABRCREG}$  | EAB synchronous read cycle time                                                         |            |
| $t_{EABWP}$     | EAB write pulse width                                                                   |            |
| $t_{EABWCCOMB}$ | EAB asynchronous write cycle time                                                       |            |
| $t_{EABWCREG}$  | EAB synchronous write cycle time                                                        |            |
| $t_{EABDD}$     | EAB data-in to data-out valid delay                                                     |            |
| $t_{EABDATACO}$ | EAB clock-to-output delay when using output registers                                   |            |
| $t_{EABDATASU}$ | EAB data/address setup time before clock when using input register                      |            |
| $t_{EABDATAH}$  | EAB data/address hold time after clock when using input register                        |            |
| $t_{EABWESU}$   | EAB WE setup time before clock when using input register                                |            |
| $t_{EABWEH}$    | EAB WE hold time after clock when using input register                                  |            |
| $t_{EABWDSU}$   | EAB data setup time before falling edge of write pulse when not using input registers   |            |
| $t_{EABWDH}$    | EAB data hold time after falling edge of write pulse when not using input registers     |            |
| $t_{EABWASU}$   | EAB address setup time before rising edge of write pulse when not using input registers |            |
| $t_{EABWAH}$    | EAB address hold time after falling edge of write pulse when not using input registers  |            |
| $t_{EABWO}$     | EAB write enable to data output valid delay                                             |            |

**Table 36. Interconnect Timing Microparameters** *Note (1)*

| Symbol           | Parameter                                                                                                            | Conditions |
|------------------|----------------------------------------------------------------------------------------------------------------------|------------|
| $t_{DIN2IOE}$    | Delay from dedicated input pin to IOE control input                                                                  | (7)        |
| $t_{DCLK2LE}$    | Delay from dedicated clock pin to LE or EAB clock                                                                    | (7)        |
| $t_{DIN2DATA}$   | Delay from dedicated input or clock to LE or EAB data                                                                | (7)        |
| $t_{DCLK2IOE}$   | Delay from dedicated clock pin to IOE clock                                                                          | (7)        |
| $t_{DIN2LE}$     | Delay from dedicated input pin to LE or EAB control input                                                            | (7)        |
| $t_{SAMELAB}$    | Routing delay for an LE driving another LE in the same LAB                                                           |            |
| $t_{SAMEROW}$    | Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row                                | (7)        |
| $t_{SAMECOLUMN}$ | Routing delay for an LE driving an IOE in the same column                                                            | (7)        |
| $t_{DIFFROW}$    | Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row                                   | (7)        |
| $t_{TROWROWS}$   | Routing delay for a row IOE or EAB driving an LE or EAB in a different row                                           | (7)        |
| $t_{LEPERIPH}$   | Routing delay for an LE driving a control signal of an IOE via the peripheral control bus                            | (7)        |
| $t_{LABCARRY}$   | Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB     |            |
| $t_{LABCASC}$    | Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB |            |

**Table 37. External Timing Parameters** *Notes (8), (10)*

| Symbol      | Parameter                                                                                      | Conditions |
|-------------|------------------------------------------------------------------------------------------------|------------|
| $t_{DRR}$   | Register-to-register delay via four LEs, three row interconnects, and four local interconnects | (9)        |
| $t_{INSU}$  | Setup time with global clock at IOE register                                                   |            |
| $t_{INH}$   | Hold time with global clock at IOE register                                                    |            |
| $t_{OUTCO}$ | Clock-to-output delay with global clock at IOE register                                        |            |

**Table 38. External Bidirectional Timing Parameters** *Note (10)*

| Symbol           | Parameter                                                                      | Condition |
|------------------|--------------------------------------------------------------------------------|-----------|
| $t_{INSUBIDIR}$  | Setup time for bidirectional pins with global clock at adjacent LE register    |           |
| $t_{INHBDIR}$    | Hold time for bidirectional pins with global clock at adjacent LE register     |           |
| $t_{OUTCOBIDIR}$ | Clock-to-output delay for bidirectional pins with global clock at IOE register |           |
| $t_{XZBIDIR}$    | Synchronous IOE output buffer disable delay                                    |           |
| $t_{ZXBIDIR}$    | Synchronous IOE output buffer enable delay, slow slew rate = off               |           |

Tables 48 through 56 show EPF10K30, EPF10K40, and EPF10K50 device internal and external timing parameters.

| <b>Table 48. EPF10K30, EPF10K40 &amp; EPF10K50 Device LE Timing Microparameters</b> <i>Note (1)</i> |                |     |                |     |      |
|-----------------------------------------------------------------------------------------------------|----------------|-----|----------------|-----|------|
| Symbol                                                                                              | -3 Speed Grade |     | -4 Speed Grade |     | Unit |
|                                                                                                     | Min            | Max | Min            | Max |      |
| $t_{LUT}$                                                                                           |                | 1.3 |                | 1.8 | ns   |
| $t_{CLUT}$                                                                                          |                | 0.6 |                | 0.6 | ns   |
| $t_{RLUT}$                                                                                          |                | 1.5 |                | 2.0 | ns   |
| $t_{PACKED}$                                                                                        |                | 0.5 |                | 0.8 | ns   |
| $t_{EN}$                                                                                            |                | 0.9 |                | 1.5 | ns   |
| $t_{CICO}$                                                                                          |                | 0.2 |                | 0.4 | ns   |
| $t_{CGEN}$                                                                                          |                | 0.9 |                | 1.4 | ns   |
| $t_{CGENR}$                                                                                         |                | 0.9 |                | 1.4 | ns   |
| $t_{CASC}$                                                                                          |                | 1.0 |                | 1.2 | ns   |
| $t_C$                                                                                               |                | 1.3 |                | 1.6 | ns   |
| $t_{CO}$                                                                                            |                | 0.9 |                | 1.2 | ns   |
| $t_{COMB}$                                                                                          |                | 0.6 |                | 0.6 | ns   |
| $t_{SU}$                                                                                            | 1.4            |     | 1.4            |     | ns   |
| $t_H$                                                                                               | 0.9            |     | 1.3            |     | ns   |
| $t_{PRE}$                                                                                           |                | 0.9 |                | 1.2 | ns   |
| $t_{CLR}$                                                                                           |                | 0.9 |                | 1.2 | ns   |
| $t_{CH}$                                                                                            | 4.0            |     | 4.0            |     | ns   |
| $t_{CL}$                                                                                            | 4.0            |     | 4.0            |     | ns   |

**Table 50. EPF10K30, EPF10K40 & EPF10K50 Device EAB Internal Microparameters** *Note (1)*

| Symbol         | -3 Speed Grade |     | -4 Speed Grade |      | Unit |
|----------------|----------------|-----|----------------|------|------|
|                | Min            | Max | Min            | Max  |      |
| $t_{EABDATA1}$ |                | 1.5 |                | 1.9  | ns   |
| $t_{EABDATA2}$ |                | 4.8 |                | 6.0  | ns   |
| $t_{EABWE1}$   |                | 1.0 |                | 1.2  | ns   |
| $t_{EABWE2}$   |                | 5.0 |                | 6.2  | ns   |
| $t_{EABCLK}$   |                | 1.0 |                | 2.2  | ns   |
| $t_{EABCO}$    |                | 0.5 |                | 0.6  | ns   |
| $t_{EABBPASS}$ |                | 1.5 |                | 1.9  | ns   |
| $t_{EABSU}$    | 1.5            |     | 1.8            |      | ns   |
| $t_{EABH}$     | 2.0            |     | 2.5            |      | ns   |
| $t_{AA}$       |                | 8.7 |                | 10.7 | ns   |
| $t_{WP}$       | 5.8            |     | 7.2            |      | ns   |
| $t_{WDSU}$     | 1.6            |     | 2.0            |      | ns   |
| $t_{WDH}$      | 0.3            |     | 0.4            |      | ns   |
| $t_{WASU}$     | 0.5            |     | 0.6            |      | ns   |
| $t_{WAH}$      | 1.0            |     | 1.2            |      | ns   |
| $t_{WO}$       |                | 5.0 |                | 6.2  | ns   |
| $t_{DD}$       |                | 5.0 |                | 6.2  | ns   |
| $t_{EABOUT}$   |                | 0.5 |                | 0.6  | ns   |
| $t_{EABCH}$    | 4.0            |     | 4.0            |      | ns   |
| $t_{EABCL}$    | 5.8            |     | 7.2            |      | ns   |

**Table 51. EPF10K30, EPF10K40 & EPF10K50 Device EAB Internal Timing Macroparameters***Note (1)*

| Symbol           | -3 Speed Grade |      | -4 Speed Grade |      | Unit |
|------------------|----------------|------|----------------|------|------|
|                  | Min            | Max  | Min            | Max  |      |
| $t_{EABAA}$      |                | 13.7 |                | 17.0 | ns   |
| $t_{EABRCCOMB}$  | 13.7           |      | 17.0           |      | ns   |
| $t_{EABRCREG}$   | 9.7            |      | 11.9           |      | ns   |
| $t_{EABWP}$      | 5.8            |      | 7.2            |      | ns   |
| $t_{EABWCCOMB}$  | 7.3            |      | 9.0            |      | ns   |
| $t_{EABWCREG}$   | 13.0           |      | 16.0           |      | ns   |
| $t_{EABDD}$      |                | 10.0 |                | 12.5 | ns   |
| $t_{EABDATA CO}$ |                | 2.0  |                | 3.4  | ns   |
| $t_{EABDATASU}$  | 5.3            |      | 5.6            |      | ns   |
| $t_{EABDATAH}$   | 0.0            |      | 0.0            |      | ns   |
| $t_{EABWESU}$    | 5.5            |      | 5.8            |      | ns   |
| $t_{EABWEH}$     | 0.0            |      | 0.0            |      | ns   |
| $t_{EABWDSU}$    | 5.5            |      | 5.8            |      | ns   |
| $t_{EABWDH}$     | 0.0            |      | 0.0            |      | ns   |
| $t_{EABWASU}$    | 2.1            |      | 2.7            |      | ns   |
| $t_{EABWAH}$     | 0.0            |      | 0.0            |      | ns   |
| $t_{EABWO}$      |                | 9.5  |                | 11.8 | ns   |

**Table 66. EPF10K100 Device EAB Internal Microparameters** *Note (1)*

| Symbol         | -3DX Speed Grade |     | -3 Speed Grade |     | -4 Speed Grade |      | Unit |
|----------------|------------------|-----|----------------|-----|----------------|------|------|
|                | Min              | Max | Min            | Max | Min            | Max  |      |
| $t_{EABDATA1}$ |                  | 1.5 |                | 1.5 |                | 1.9  | ns   |
| $t_{EABDATA2}$ |                  | 4.8 |                | 4.8 |                | 6.0  | ns   |
| $t_{EABWE1}$   |                  | 1.0 |                | 1.0 |                | 1.2  | ns   |
| $t_{EABWE2}$   |                  | 5.0 |                | 5.0 |                | 6.2  | ns   |
| $t_{EABCLK}$   |                  | 1.0 |                | 1.0 |                | 2.2  | ns   |
| $t_{EABCO}$    |                  | 0.5 |                | 0.5 |                | 0.6  | ns   |
| $t_{EABYPASS}$ |                  | 1.5 |                | 1.5 |                | 1.9  | ns   |
| $t_{EABSU}$    | 1.5              |     | 1.5            |     | 1.8            |      | ns   |
| $t_{EABH}$     | 2.0              |     | 2.0            |     | 2.5            |      | ns   |
| $t_{AA}$       |                  | 8.7 |                | 8.7 |                | 10.7 | ns   |
| $t_{WP}$       | 5.8              |     | 5.8            |     | 7.2            |      | ns   |
| $t_{WDSU}$     | 1.6              |     | 1.6            |     | 2.0            |      | ns   |
| $t_{WDH}$      | 0.3              |     | 0.3            |     | 0.4            |      | ns   |
| $t_{WASU}$     | 0.5              |     | 0.5            |     | 0.6            |      | ns   |
| $t_{WAH}$      | 1.0              |     | 1.0            |     | 1.2            |      | ns   |
| $t_{WO}$       |                  | 5.0 |                | 5.0 |                | 6.2  | ns   |
| $t_{DD}$       |                  | 5.0 |                | 5.0 |                | 6.2  | ns   |
| $t_{EABOUT}$   |                  | 0.5 |                | 0.5 |                | 0.6  | ns   |
| $t_{EABCH}$    | 4.0              |     | 4.0            |     | 4.0            |      | ns   |
| $t_{EABCL}$    | 5.8              |     | 5.8            |     | 7.2            |      | ns   |

**Table 88. EPF10K10A Device EAB Internal Timing Macroparameters** *Note (1)*

| Symbol           | -1 Speed Grade |     | -2 Speed Grade |     | -3 Speed Grade |      | Unit |
|------------------|----------------|-----|----------------|-----|----------------|------|------|
|                  | Min            | Max | Min            | Max | Min            | Max  |      |
| $t_{EABAA}$      |                | 8.1 |                | 9.8 |                | 13.1 | ns   |
| $t_{EABRCCOMB}$  | 8.1            |     | 9.8            |     | 13.1           |      | ns   |
| $t_{EABRCREG}$   | 5.8            |     | 6.9            |     | 9.3            |      | ns   |
| $t_{EABWP}$      | 2.0            |     | 2.4            |     | 3.2            |      | ns   |
| $t_{EABWCCOMB}$  | 3.5            |     | 4.2            |     | 5.6            |      | ns   |
| $t_{EABWCREG}$   | 9.4            |     | 11.2           |     | 14.8           |      | ns   |
| $t_{EABDD}$      |                | 6.9 |                | 8.3 |                | 11.0 | ns   |
| $t_{EABDATA CO}$ |                | 1.3 |                | 1.5 |                | 2.0  | ns   |
| $t_{EABDATASU}$  | 2.4            |     | 3.0            |     | 3.9            |      | ns   |
| $t_{EABDATAH}$   | 0.0            |     | 0.0            |     | 0.0            |      | ns   |
| $t_{EABWESU}$    | 4.1            |     | 4.9            |     | 6.5            |      | ns   |
| $t_{EABWEH}$     | 0.0            |     | 0.0            |     | 0.0            |      | ns   |
| $t_{EABWDSU}$    | 1.4            |     | 1.6            |     | 2.2            |      | ns   |
| $t_{EABWDH}$     | 0.0            |     | 0.0            |     | 0.0            |      | ns   |
| $t_{EABWASU}$    | 2.5            |     | 3.0            |     | 4.1            |      | ns   |
| $t_{EABWAH}$     | 0.0            |     | 0.0            |     | 0.0            |      | ns   |
| $t_{EABWO}$      |                | 6.2 |                | 7.5 |                | 9.9  | ns   |

**Notes to tables:**

- (1) All timing parameters are described in Tables 32 through 38 in this data sheet.
- (2) Using an LE to register the signal may provide a lower setup time.
- (3) This parameter is specified by characterization.

Tables 92 through 98 show EPF10K30A device internal and external timing parameters.

| <b>Table 92. EPF10K30A Device LE Timing Microparameters</b> <i>Note (1)</i> |                |     |                |     |                |     |      |
|-----------------------------------------------------------------------------|----------------|-----|----------------|-----|----------------|-----|------|
| Symbol                                                                      | -1 Speed Grade |     | -2 Speed Grade |     | -3 Speed Grade |     | Unit |
|                                                                             | Min            | Max | Min            | Max | Min            | Max |      |
| $t_{LUT}$                                                                   |                | 0.8 |                | 1.1 |                | 1.5 | ns   |
| $t_{CLUT}$                                                                  |                | 0.6 |                | 0.7 |                | 1.0 | ns   |
| $t_{RLUT}$                                                                  |                | 1.2 |                | 1.5 |                | 2.0 | ns   |
| $t_{PACKED}$                                                                |                | 0.6 |                | 0.6 |                | 1.0 | ns   |
| $t_{EN}$                                                                    |                | 1.3 |                | 1.5 |                | 2.0 | ns   |
| $t_{CICO}$                                                                  |                | 0.2 |                | 0.3 |                | 0.4 | ns   |
| $t_{CGEN}$                                                                  |                | 0.8 |                | 1.0 |                | 1.3 | ns   |
| $t_{CGENR}$                                                                 |                | 0.6 |                | 0.8 |                | 1.0 | ns   |
| $t_{CASC}$                                                                  |                | 0.9 |                | 1.1 |                | 1.4 | ns   |
| $t_C$                                                                       |                | 1.1 |                | 1.3 |                | 1.7 | ns   |
| $t_{CO}$                                                                    |                | 0.4 |                | 0.6 |                | 0.7 | ns   |
| $t_{COMB}$                                                                  |                | 0.6 |                | 0.7 |                | 0.9 | ns   |
| $t_{SU}$                                                                    | 0.9            |     | 0.9            |     | 1.4            |     | ns   |
| $t_H$                                                                       | 1.1            |     | 1.3            |     | 1.7            |     | ns   |
| $t_{PRE}$                                                                   |                | 0.5 |                | 0.6 |                | 0.8 | ns   |
| $t_{CLR}$                                                                   |                | 0.5 |                | 0.6 |                | 0.8 | ns   |
| $t_{CH}$                                                                    | 3.0            |     | 3.5            |     | 4.0            |     | ns   |
| $t_{CL}$                                                                    | 3.0            |     | 3.5            |     | 4.0            |     | ns   |

| <b>Table 93. EPF10K30A Device IOE Timing Microparameters</b> <i>Note (1) (Part 1 of 2)</i> |                |     |                |     |                |     |      |
|--------------------------------------------------------------------------------------------|----------------|-----|----------------|-----|----------------|-----|------|
| Symbol                                                                                     | -1 Speed Grade |     | -2 Speed Grade |     | -3 Speed Grade |     | Unit |
|                                                                                            | Min            | Max | Min            | Max | Min            | Max |      |
| $t_{IOD}$                                                                                  |                | 2.2 |                | 2.6 |                | 3.4 | ns   |
| $t_{IOC}$                                                                                  |                | 0.3 |                | 0.3 |                | 0.5 | ns   |
| $t_{IOCO}$                                                                                 |                | 0.2 |                | 0.2 |                | 0.3 | ns   |
| $t_{IOCOMB}$                                                                               |                | 0.5 |                | 0.6 |                | 0.8 | ns   |
| $t_{IOSU}$                                                                                 | 1.4            |     | 1.7            |     | 2.2            |     | ns   |

**Table 95. EPF10K30A Device EAB Internal Timing Macroparameters***Note (1)*

| Symbol          | -1 Speed Grade |     | -2 Speed Grade |      | -3 Speed Grade |      | Unit |
|-----------------|----------------|-----|----------------|------|----------------|------|------|
|                 | Min            | Max | Min            | Max  | Min            | Max  |      |
| $t_{EABAA}$     |                | 9.7 |                | 11.6 |                | 16.2 | ns   |
| $t_{EABRCCOMB}$ | 9.7            |     | 11.6           |      | 16.2           |      | ns   |
| $t_{EABRCREG}$  | 5.9            |     | 7.1            |      | 9.7            |      | ns   |
| $t_{EABWP}$     | 3.8            |     | 4.5            |      | 5.9            |      | ns   |
| $t_{EABWCCOMB}$ | 4.0            |     | 4.7            |      | 6.3            |      | ns   |
| $t_{EABWCREG}$  | 9.8            |     | 11.6           |      | 16.6           |      | ns   |
| $t_{EABDD}$     |                | 9.2 |                | 11.0 |                | 16.1 | ns   |
| $t_{EABDATACO}$ |                | 1.7 |                | 2.1  |                | 3.4  | ns   |
| $t_{EABDATASU}$ | 2.3            |     | 2.7            |      | 3.5            |      | ns   |
| $t_{EABDATAH}$  | 0.0            |     | 0.0            |      | 0.0            |      | ns   |
| $t_{EABWESU}$   | 3.3            |     | 3.9            |      | 4.9            |      | ns   |
| $t_{EABWEH}$    | 0.0            |     | 0.0            |      | 0.0            |      | ns   |
| $t_{EABWDSU}$   | 3.2            |     | 3.8            |      | 5.0            |      | ns   |
| $t_{EABWDH}$    | 0.0            |     | 0.0            |      | 0.0            |      | ns   |
| $t_{EABWASU}$   | 3.7            |     | 4.4            |      | 5.1            |      | ns   |
| $t_{EABWAH}$    | 0.0            |     | 0.0            |      | 0.0            |      | ns   |
| $t_{EABWO}$     |                | 6.1 |                | 7.3  |                | 11.3 | ns   |



*Notes:*