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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	360
Number of Logic Elements/Cells	2880
Total RAM Bits	20480
Number of I/O	274
Number of Gates	116000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	356-LBGA
Supplier Device Package	356-BGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k50vbi356-4

Notes to tables:
(1) FLEX 10K and FLEX 10KA device package types include plastic J-lead chip carrier (PLCC), thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), ball-grid array (BGA), pin-grid array (PGA), and FineLine BGA™ packages.
(2) This option is supported with a 256-pin FineLine BGA package. By using SameFrame pin migration, all FineLine BGA packages are pin compatible. For example, a board can be designed to support both 256-pin and 484-pin FineLine BGA packages. The Altera software automatically avoids conflicting pins when future migration is set.

General Description

Altera's FLEX 10K devices are the industry's first embedded PLDs. Based on reconfigurable CMOS SRAM elements, the Flexible Logic Element MatriX (FLEX) architecture incorporates all features necessary to implement common gate array megafunctions. With up to 250,000 gates, the FLEX 10K family provides the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device.

FLEX 10K devices are reconfigurable, which allows 100% testing prior to shipment. As a result, the designer is not required to generate test vectors for fault coverage purposes. Additionally, the designer does not need to manage inventories of different ASIC designs; FLEX 10K devices can be configured on the board for the specific functionality required.

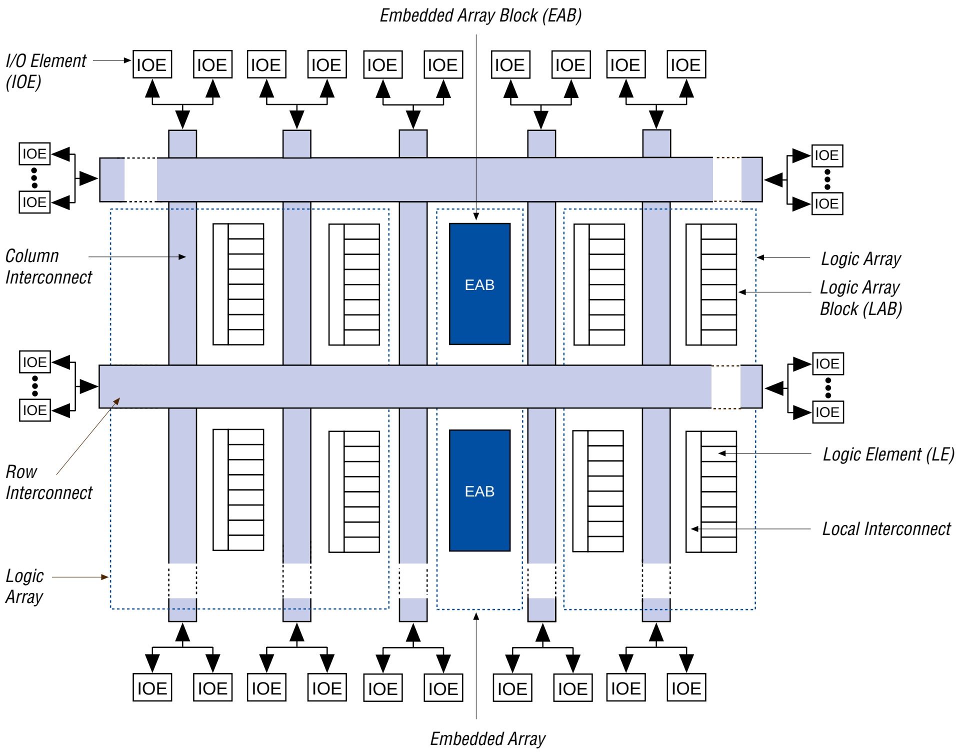
Table 6 shows FLEX 10K performance for some common designs. All performance values were obtained with Synopsys DesignWare or LPM functions. No special design technique was required to implement the applications; the designer simply inferred or instantiated a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

Table 6. FLEX 10K & FLEX 10KA Performance

Application	Resources Used		Performance				Units
	LEs	EABs	-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	-4 Speed Grade	
16-bit loadable counter *(1)*	16	0	204	166	125	95	MHz
16-bit accumulator *(1)*	16	0	204	166	125	95	MHz
16-to-1 multiplexer *(2)*	10	0	4.2	5.8	6.0	7.0	ns
256 × 8 RAM read cycle speed *(3)*	0	1	172	145	108	84	MHz
256 × 8 RAM write cycle speed *(3)*	0	1	106	89	68	63	MHz

Notes:
(1) The speed grade of this application is limited because of clock high and low specifications.
(2) This application uses combinatorial inputs and outputs.
(3) This application uses registered inputs and outputs.

Figure 1. FLEX 10K Device Block Diagram



FLEX 10K devices provide six dedicated inputs that drive the flipflops' control inputs to ensure the efficient distribution of high-speed, low-skew (less than 1.5 ns) control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

Embedded Array Block

The EAB is a flexible block of RAM with registers on the input and output ports, and is used to implement common gate array megafunctions. The EAB is also suitable for functions such as multipliers, vector scalars, and error correction circuits, because it is large and flexible. These functions can be combined in applications such as digital filters and microcontrollers.

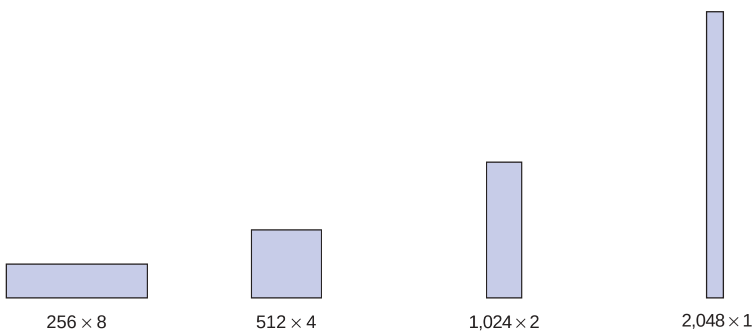
Logic functions are implemented by programming the EAB with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of EABs. The large capacity of EABs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or field-programmable gate array (FPGA) RAM blocks. For example, a single EAB can implement a 4 × 4 multiplier with eight inputs and eight outputs. Parameterized functions such as LPM functions can automatically take advantage of the EAB.

The EAB provides advantages over FPGAs, which implement on-board RAM as arrays of small, distributed RAM blocks. These FPGA RAM blocks contain delays that are less predictable as the size of the RAM increases. In addition, FPGA RAM blocks are prone to routing problems because small blocks of RAM must be connected together to make larger blocks. In contrast, EABs can be used to implement large, dedicated blocks of RAM that eliminate these timing and routing concerns.

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (`WE`) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the `WE` signal. In contrast, the EAB's synchronous RAM generates its own `WE` signal and is self-timed with respect to the global clock. A circuit using the EAB's self-timed RAM need only meet the setup and hold time specifications of the global clock.

When used as RAM, each EAB can be configured in any of the following sizes: 256 × 8, 512 × 4, 1,024 × 2, or 2,048 × 1. See Figure 2.

Figure 2. EAB Memory Configurations



Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across devices; it provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock enable or eight output enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by specific LEs. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, an LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal. The chip-wide reset signal will reset all IOE registers, overriding any other control signals.

Tables 8 and 9 list the sources for each peripheral control signal, and the rows that can drive global signals. These tables also show how the output enable, clock enable, clock, and clear signals share 12 peripheral control signals.

Figure 15. FLEX 10K Column-to-IOE Connections

The values for m and n are provided in Table 11.

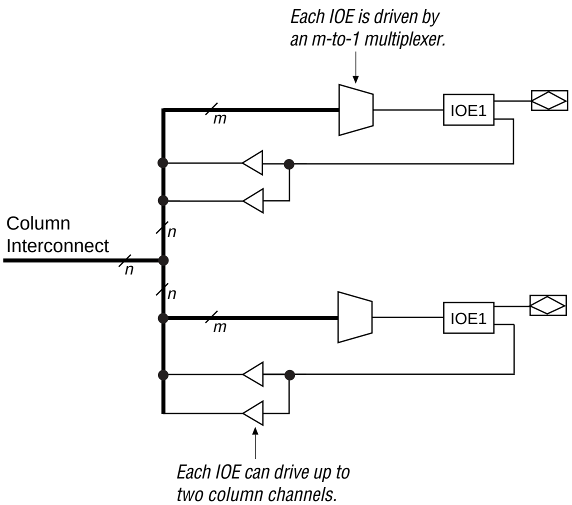


Table 11 lists the FLEX 10K column-to-IOE interconnect resources.

Table 11. FLEX 10K Column-to-IOE Interconnect Resources

Device	Channels per Column (*n*)	Column Channel per Pin (*m*)
EPF10K10 EPF10K10A	24	16
EPF10K20	24	16
EPF10K30 EPF10K30A	24	16
EPF10K40	24	16
EPF10K50 EPF10K50V	24	16
EPF10K70	24	16
EPF10K100 EPF10K100A	24	16
EPF10K130V	32	24
EPF10K250A	40	32

Table 12 describes the FLEX 10K device supply voltages and MultiVolt I/O support levels.

Table 12. Supply Voltages & MultiVolt I/O Support Levels

Devices	Supply Voltage (V)		MultiVolt I/O Support Levels (V)	
	V_{CCINT}	V_{CCIO}	Input	Output
FLEX 10K *(1)*	5.0	5.0	3.3 or 5.0	5.0
	5.0	3.3	3.3 or 5.0	3.3 or 5.0
EPF10K50V *(1)*	3.3	3.3	3.3 or 5.0	3.3 or 5.0
EPF10K130V	3.3	3.3	3.3 or 5.0	3.3 or 5.0
FLEX 10KA *(1)*	3.3	3.3	2.5, 3.3, or 5.0	3.3 or 5.0
	3.3	2.5	2.5, 3.3, or 5.0	2.5

Note

(1) 240-pin QFP packages do not support the MultiVolt I/O features, so they do not have separate V_{CCIO} pins.

Power Sequencing & Hot-Socketing

Because FLEX 10K devices can be used in a multi-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power supplies can be powered in any order.

Signals can be driven into FLEX 10KA devices before and during power up without damaging the device. Additionally, FLEX 10KA devices do not drive out during power up. Once operating conditions are reached, FLEX 10KA devices operate as specified by the user.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

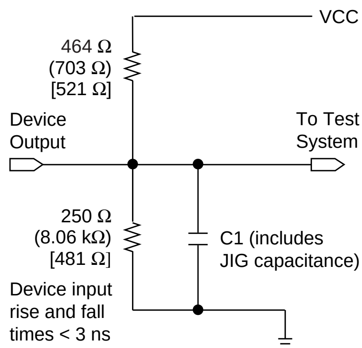
All FLEX 10K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. All FLEX 10K devices can also be configured using the JTAG pins through the BitBlaster serial download cable, or ByteBlasterMV parallel port download cable, or via hardware that uses the Jam™ programming and test language. JTAG BST can be performed before or after configuration, but not during configuration. FLEX 10K devices support the JTAG instructions shown in Table 13.

Generic Testing

Each FLEX 10K device is functionally tested. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% yield. AC test measurements for FLEX 10K devices are made under conditions equivalent to those shown in Figure 19. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 19. FLEX 10K AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers without parentheses are for 5.0-V devices or outputs. Numbers in parentheses are for 3.3-V devices or outputs. Numbers in brackets are for 2.5-V devices or outputs.



Operating Conditions

Tables 17 through 21 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 5.0-V FLEX 10K devices.

Table 17. FLEX 10K 5.0-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground *(2)*	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		PQFP, TQFP, RQFP, and BGA packages, under bias		135	° C

Table 18. FLEX 10K 5.0-V Device Recommended Operating Conditions					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output buffers, 5.0-V operation	*(3)*, *(4)*	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output buffers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
V_I	Input voltage		–0.5	V_{CCINT} + 0.5	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Figure 26. FLEX 10K Device IOE Timing Model

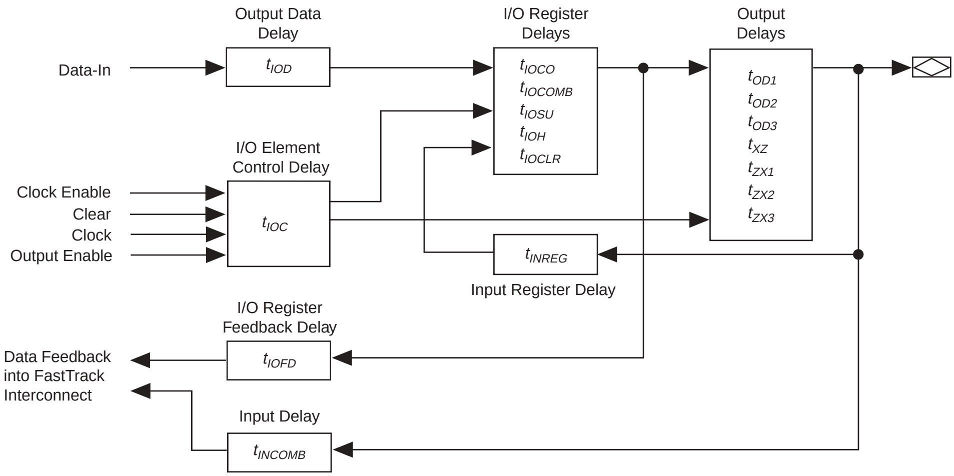
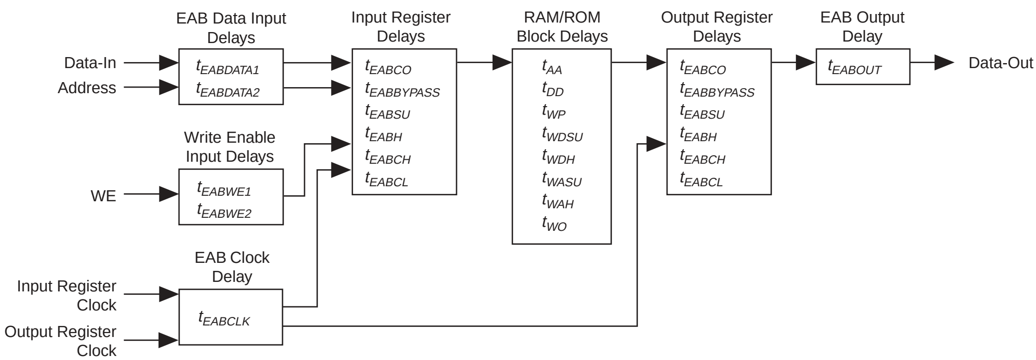


Figure 27. FLEX 10K Device EAB Timing Model



Figures 28 shows the timing model for bidirectional I/O pin timing.

Table 34. EAB Timing Microparameters *Note (1)*		
Symbol	**Parameter**	**Conditions**
$t_{EABDATA1}$	Data or address delay to EAB for combinatorial input	
$t_{EABDATA2}$	Data or address delay to EAB for registered input	
t_{EABWE1}	Write enable delay to EAB for combinatorial input	
t_{EABWE2}	Write enable delay to EAB for registered input	
t_{EABCLK}	EAB register clock delay	
t_{EABCO}	EAB register clock-to-output delay	
$t_{EABBYPASS}$	Bypass register delay	
t_{EABSU}	EAB register setup time before clock	
t_{EABH}	EAB register hold time after clock	
t_{AA}	Address access delay	
t_{WP}	Write pulse width	
t_{WDSU}	Data setup time before falling edge of write pulse	*(5)*
t_{WDH}	Data hold time after falling edge of write pulse	*(5)*
t_{WASU}	Address setup time before rising edge of write pulse	*(5)*
t_{WAH}	Address hold time after falling edge of write pulse	*(5)*
t_{WO}	Write enable to data output valid delay	
t_{DD}	Data-in to data-out valid delay	
t_{EABOUT}	Data-out delay	
t_{EABCH}	Clock high time	
t_{EABCL}	Clock low time	

Table 67. EPF10K100 Device EAB Internal Timing Macroparameters *Note (1)*							
Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		13.7		13.7		17.0	ns
$t_{EABRCCOMB}$	13.7		13.7		17.0		ns
$t_{EABRCREG}$	9.7		9.7		11.9		ns
t_{EABWP}	5.8		5.8		7.2		ns
$t_{EABWCCOMB}$	7.3		7.3		9.0		ns
$t_{EABWCREG}$	13.0		13.0		16.0		ns
t_{EABDD}		10.0		10.0		12.5	ns
$t_{EABDATACO}$		2.0		2.0		3.4	ns
$t_{EABDATASU}$	5.3		5.3		5.6		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	5.5		5.5		5.8		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	5.5		5.5		5.8		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	2.1		2.1		2.7		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		9.5		9.5		11.8	ns

Table 75. EPF10K50V Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		4.7		6.0		7.1		8.2	ns
t_{DIN2LE}		2.5		2.6		3.1		3.9	ns
$t_{DIN2DATA}$		4.4		5.9		6.8		7.7	ns
$t_{DCLK2IOE}$		2.5		3.9		4.7		5.5	ns
$t_{DCLK2LE}$		2.5		2.6		3.1		3.9	ns
$t_{SAMELAB}$		0.2		0.2		0.3		0.3	ns
$t_{SAMEROW}$		2.8		3.0		3.2		3.4	ns
$t_{SAMECOLUMN}$		3.0		3.2		3.4		3.6	ns
$t_{DIFFROW}$		5.8		6.2		6.6		7.0	ns
$t_{TWOROWS}$		8.6		9.2		9.8		10.4	ns
$t_{LEPERIPH}$		4.5		5.5		6.1		7.0	ns
$t_{LABCARRY}$		0.3		0.4		0.5		0.7	ns
$t_{LABCASC}$		0.0		1.3		1.6		2.0	ns

Table 76. EPF10K50V Device External Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{DRR}		11.2		14.0		17.2		21.1	ns
t_{INSU} *(2)*, *(3)*	5.5		4.2		5.2		6.9		ns
t_{INH} *(3)*	0.0		0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	5.9	2.0	7.8	2.0	9.5	2.0	11.1	ns

Table 77. EPF10K50V Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.0		2.8		3.5		4.1		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	5.9	2.0	7.8	2.0	9.5	2.0	11.1	ns
$t_{XZBIDIR}$		8.0		9.8		11.8		14.3	ns
$t_{ZXBIDIR}$		8.0		9.8		11.8		14.3	ns

Notes to tables:
(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Tables 78 through 84 show EPF10K130V device internal and external timing parameters.

Table 78. EPF10K130V Device LE Timing Microparameters *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		1.3		1.8		2.3	ns
t_{CLUT}		0.5		0.7		0.9	ns
t_{RLUT}		1.2		1.7		2.2	ns
t_{PACKED}		0.5		0.6		0.7	ns
t_{EN}		0.6		0.8		1.0	ns
t_{CICO}		0.2		0.3		0.4	ns
t_{CGEN}		0.3		0.4		0.5	ns
t_{CGENR}		0.7		1.0		1.3	ns
t_{CASC}		0.9		1.2		1.5	ns
t_{C}		1.9		2.4		3.0	ns
t_{CO}		0.6		0.9		1.1	ns
t_{COMB}		0.5		0.7		0.9	ns
t_{SU}	0.2		0.2		0.3		ns
t_{H}	0.0		0.0		0.0		ns
t_{PRE}		2.4		3.1		3.9	ns
t_{CLR}		2.4		3.1		3.9	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns

Table 79. EPF10K130V Device IOE Timing Microparameters *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{IOD}		1.3		1.6		2.0	ns
t_{IOC}		0.4		0.5		0.7	ns
t_{IOCO}		0.3		0.4		0.5	ns
t_{IOCOMB}		0.0		0.0		0.0	ns
t_{IOSU}	2.6		3.3		3.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.7		2.2		2.7	ns
t_{OD1}		3.5		4.4		5.0	ns
t_{OD2}		–		–		–	ns
t_{OD3}		8.2		8.1		9.7	ns
t_{XZ}		4.9		6.3		7.4	ns
t_{ZX1}		4.9		6.3		7.4	ns
t_{ZX2}		–		–		–	ns
t_{ZX3}		9.6		10.0		12.1	ns
t_{INREG}		7.9		10.0		12.6	ns
t_{IOFD}		6.2		7.9		9.9	ns
t_{INCOMB}		6.2		7.9		9.9	ns

Table 82. EPF10K130V Device Interconnect Timing Microparameters *Note (1)*							
Symbol	**-2 Speed Grade**		**-3 Speed Grade**		**-4 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{DIN2IOE}$		8.0		9.0		9.5	ns
t_{DIN2LE}		2.4		3.0		3.1	ns
$t_{DIN2DATA}$		5.0		6.3		7.4	ns
$t_{DCLK2IOE}$		3.6		4.6		5.1	ns
$t_{DCLK2LE}$		2.4		3.0		3.1	ns
$t_{SAMELAB}$		0.4		0.6		0.8	ns
$t_{SAMEROW}$		4.5		5.3		6.5	ns
$t_{SAMECOLUMN}$		9.0		9.5		9.7	ns
$t_{DIFFROW}$		13.5		14.8		16.2	ns
$t_{TWOROWS}$		18.0		20.1		22.7	ns
$t_{LEPERIPH}$		8.1		8.6		9.5	ns
$t_{LABCARRY}$		0.6		0.8		1.0	ns
$t_{LABCASC}$		0.8		1.0		1.2	ns

Table 83. EPF10K130V Device External Timing Parameters *Note (1)*							
Symbol	**-2 Speed Grade**		**-3 Speed Grade**		**-4 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{DRR}		15.0		19.1		24.2	ns
t_{INSU} *(2)*, *(3)*	6.9		8.6		11.0		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	7.8	2.0	9.9	2.0	11.3	ns

Table 84. EPF10K130V Device External Bidirectional Timing Parameters *Note (1)*							
Symbol	**-2 Speed Grade**		**-3 Speed Grade**		**-4 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{INSUBIDIR}$	6.7		8.5		10.8		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	6.9	2.0	8.8	2.0	10.2	ns
$t_{XZBIDIR}$		12.9		16.4		19.3	ns
$t_{ZXBIDIR}$		12.9		16.4		19.3	ns

Notes to tables:

(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Tables 92 through 98 show EPF10K30A device internal and external timing parameters.

Table 92. EPF10K30A Device LE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.8		1.1		1.5	ns
t_{CLUT}		0.6		0.7		1.0	ns
t_{RLUT}		1.2		1.5		2.0	ns
t_{PACKED}		0.6		0.6		1.0	ns
t_{EN}		1.3		1.5		2.0	ns
t_{CICO}		0.2		0.3		0.4	ns
t_{CGEN}		0.8		1.0		1.3	ns
t_{CGENR}		0.6		0.8		1.0	ns
t_{CASC}		0.9		1.1		1.4	ns
t_{C}		1.1		1.3		1.7	ns
t_{CO}		0.4		0.6		0.7	ns
t_{COMB}		0.6		0.7		0.9	ns
t_{SU}	0.9		0.9		1.4		ns
t_{H}	1.1		1.3		1.7		ns
t_{PRE}		0.5		0.6		0.8	ns
t_{CLR}		0.5		0.6		0.8	ns
t_{CH}	3.0		3.5		4.0		ns
t_{CL}	3.0		3.5		4.0		ns

Table 93. EPF10K30A Device IOE Timing Microparameters *Note (1)* **(Part 1 of 2)**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{IOD}		2.2		2.6		3.4	ns
t_{IOC}		0.3		0.3		0.5	ns
t_{IOCO}		0.2		0.2		0.3	ns
t_{IOCOMB}		0.5		0.6		0.8	ns
t_{IOSU}	1.4		1.7		2.2		ns

Table 94. EPF10K30A Device EAB Internal Microparameters *Note (1)*							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{EABDATA1}$		5.5		6.5		8.5	ns
$t_{EABDATA2}$		1.1		1.3		1.8	ns
t_{EABWE1}		2.4		2.8		3.7	ns
t_{EABWE2}		2.1		2.5		3.2	ns
t_{EABCLK}		0.0		0.0		0.2	ns
t_{EABCO}		1.7		2.0		2.6	ns
$t_{EABBYPASS}$		0.0		0.0		0.3	ns
t_{EABSU}	1.2		1.4		1.9		ns
t_{EABH}	0.1		0.1		0.3		ns
t_{AA}		4.2		5.0		6.5	ns
t_{WP}	3.8		4.5		5.9		ns
t_{WDSU}	0.1		0.1		0.2		ns
t_{WDH}	0.1		0.1		0.2		ns
t_{WASU}	0.1		0.1		0.2		ns
t_{WAH}	0.1		0.1		0.2		ns
t_{WO}		3.7		4.4		6.4	ns
t_{DD}		3.7		4.4		6.4	ns
t_{EABOUT}		0.0		0.1		0.6	ns
t_{EABCH}	3.0		3.5		4.0		ns
t_{EABCL}	3.8		4.5		5.9		ns

Table 95. EPF10K30A Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		9.7		11.6		16.2	ns
$t_{EABRCCOMB}$	9.7		11.6		16.2		ns
$t_{EABRCREG}$	5.9		7.1		9.7		ns
t_{EABWP}	3.8		4.5		5.9		ns
$t_{EABWCCOMB}$	4.0		4.7		6.3		ns
$t_{EABWCREG}$	9.8		11.6		16.6		ns
t_{EABDD}		9.2		11.0		16.1	ns
$t_{EABDATACO}$		1.7		2.1		3.4	ns
$t_{EABDATASU}$	2.3		2.7		3.5		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	3.3		3.9		4.9		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	3.2		3.8		5.0		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.7		4.4		5.1		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		6.1		7.3		11.3	ns

Table 96. EPF10K30A Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		3.9		4.4		5.1	ns
t_{DIN2LE}		1.2		1.5		1.9	ns
$t_{DIN2DATA}$		3.2		3.6		4.5	ns
$t_{DCLK2IOE}$		3.0		3.5		4.6	ns
$t_{DCLK2LE}$		1.2		1.5		1.9	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		2.3		2.4		2.7	ns
$t_{SAMECOLUMN}$		1.3		1.4		1.9	ns
$t_{DIFFROW}$		3.6		3.8		4.6	ns
$t_{TWOROWS}$		5.9		6.2		7.3	ns
$t_{LEPERIPH}$		3.5		3.8		4.1	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.9		1.1		1.4	ns

Table 97. EPF10K30A External Reference Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		11.0		13.0		17.0	ns
t_{INSU} *(2)*, *(3)*	2.5		3.1		3.9		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	5.4	2.0	6.2	2.0	8.3	ns

Table 98. EPF10K30A Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	4.2		4.9		6.8		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	5.4	2.0	6.2	2.0	8.3	ns
$t_{XZBIDIR}$		6.2		7.5		9.8	ns
$t_{ZXBIDIR}$		6.2		7.5		9.8	ns

Table 101. EPF10K100A Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.8		2.1		2.4	ns
$t_{EABDATA2}$		3.2		3.7		4.4	ns
t_{EABWE1}		0.8		0.9		1.1	ns
t_{EABWE2}		2.3		2.7		3.1	ns
t_{EABCLK}		0.8		0.9		1.1	ns
t_{EABCO}		1.0		1.1		1.4	ns
$t_{EABBYPASS}$		0.3		0.3		0.4	ns
t_{EABSU}	1.3		1.5		1.8		ns
t_{EABH}	0.4		0.5		0.5		ns
t_{AA}		4.1		4.8		5.6	ns
t_{WP}	3.2		3.7		4.4		ns
t_{WDSU}	2.4		2.8		3.3		ns
t_{WDH}	0.2		0.2		0.3		ns
t_{WASU}	0.2		0.2		0.3		ns
t_{WAH}	0.0		0.0		0.0		ns
t_{WO}		3.4		3.9		4.6	ns
t_{DD}		3.4		3.9		4.6	ns
t_{EABOUT}		0.3		0.3		0.4	ns
t_{EABCH}	2.5		3.5		4.0		ns
t_{EABCL}	3.2		3.7		4.4		ns