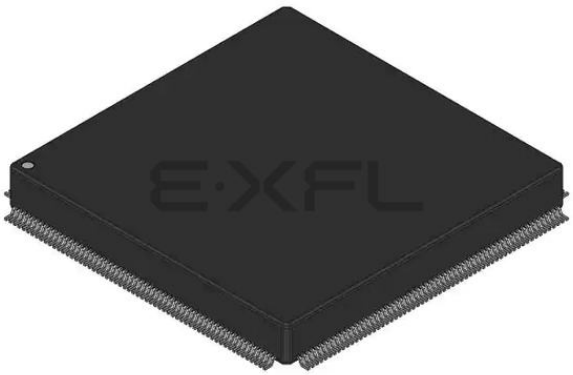
Altera - EPF10K50VQC240-1N Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	360
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	189
Number of Gates	-
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	240-BQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epf10k50vqc240-1n

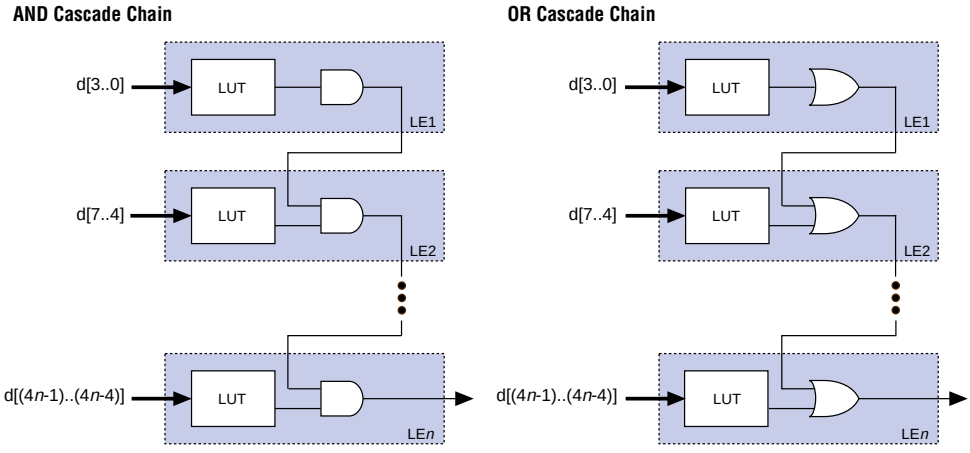
Cascade Chain

With the cascade chain, the FLEX 10K architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay as low as 0.7 ns per LE. Cascade chain logic can be created automatically by the Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than eight bits are implemented automatically by linking several LABs together. For easier routing, a long cascade chain skips every other LAB in a row. A cascade chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB (e.g., the last LE of the first LAB in a row cascades to the first LE of the third LAB). The cascade chain does not cross the center of the row (e.g., in the EPF10K50 device, the cascade chain stops at the eighteenth LAB and a new one begins at the nineteenth LAB). This break is due to the EAB's placement in the middle of the row.

Figure 8 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of 4*n* variables implemented with *n* LEs. The LE delay is as low as 1.6 ns; the cascade chain delay is as low as 0.7 ns. With the cascade chain, 3.7 ns is needed to decode a 16-bit address.

Figure 8. Cascade Chain Operation



Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. Either the register or the LUT can be used to drive both the local interconnect and the FastTrack Interconnect at the same time.

The LUT and the register in the LE can be used independently; this feature is known as register packing. To support register packing, the LE has two outputs; one drives the local interconnect and the other drives the FastTrack Interconnect. The DATA4 signal can drive the register directly, allowing the LUT to compute a function that is independent of the registered signal; a three-input function can be computed in the LUT, and a fourth independent signal can be registered. Alternatively, a four-input function can be generated, and one of the inputs to this function can be used to drive the register. The register in a packed LE can still use the clock enable, clear, and preset signals in the LE. In a packed LE, the register can drive the FastTrack Interconnect while the LUT drives the local interconnect, or vice versa.

Arithmetic Mode

The arithmetic mode offers 2 three-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT computes a three-input function, and the other generates a carry output. As shown in Figure 9 on page 19, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three signals: a, b, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

Table 10 lists the FLEX 10K row-to-IOE interconnect resources.

Table 10. FLEX 10K Row-to-IOE Interconnect Resources

Device	Channels per Row (*n*)	Row Channels per Pin (*m*)
EPF10K10 EPF10K10A	144	18
EPF10K20	144	18
EPF10K30 EPF10K30A	216	27
EPF10K40	216	27
EPF10K50 EPF10K50V	216	27
EPF10K70	312	39
EPF10K100 EPF10K100A	312	39
EPF10K130V	312	39
EPF10K250A	456	57

Column-to-IOE Connections

When an IOE is used as an input, it can drive up to two separate column channels. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the column channels. Two IOEs connect to each side of the column channels. Each IOE can be driven by column channels via a multiplexer. The set of column channels that each IOE can access is different for each IOE. See Figure 15.

Figure 15. FLEX 10K Column-to-IOE Connections

The values for m and n are provided in Table 11.

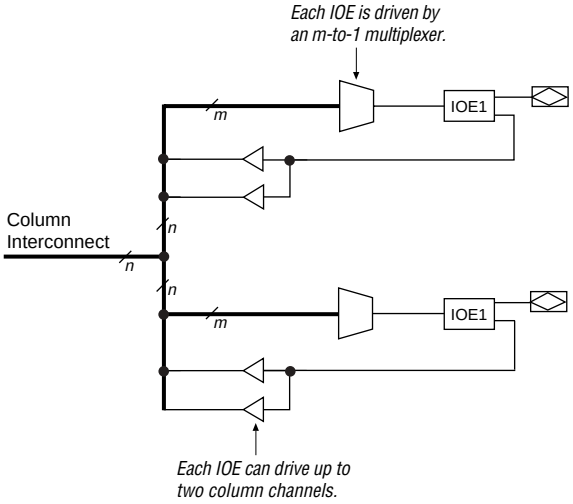


Table 11 lists the FLEX 10K column-to-IOE interconnect resources.

Table 11. FLEX 10K Column-to-IOE Interconnect Resources

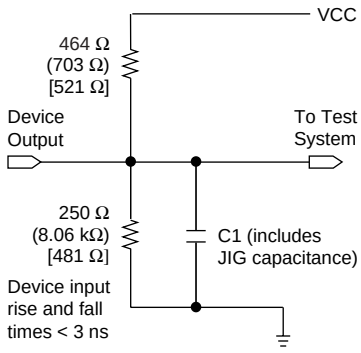
Device	Channels per Column (*n*)	Column Channel per Pin (*m*)
EPF10K10 EPF10K10A	24	16
EPF10K20	24	16
EPF10K30 EPF10K30A	24	16
EPF10K40	24	16
EPF10K50 EPF10K50V	24	16
EPF10K70	24	16
EPF10K100 EPF10K100A	24	16
EPF10K130V	32	24
EPF10K250A	40	32

Generic Testing

Each FLEX 10K device is functionally tested. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% yield. AC test measurements for FLEX 10K devices are made under conditions equivalent to those shown in Figure 19. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 19. FLEX 10K AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers without parentheses are for 5.0-V devices or outputs. Numbers in parentheses are for 3.3-V devices or outputs. Numbers in brackets are for 2.5-V devices or outputs.



Operating Conditions

Tables 17 through 21 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 5.0-V FLEX 10K devices.

Table 17. FLEX 10K 5.0-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground *(2)*	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		PQFP, TQFP, RQFP, and BGA packages, under bias		135	° C

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms. V_{CC} must rise monotonically.
(5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(6) These values are specified under the Recommended Operation Condition shown in Table 18 on page 45.
(7) The I_{OH} parameter refers to high-level TTL or CMOS output current.
(8) The I_{OL} parameter refers to low-level TTL or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(9) This value is specified for normal device operation. The value may vary during power-up.
(10) Capacitance is sample-tested only.

Figure 20 shows the typical output drive characteristics of FLEX 10K devices with 5.0-V and 3.3-V V_{CCIO}. The output driver is compliant with the 5.0-V ***PCI Local Bus Specification, Revision 2.2*** (for 5.0-V V_{CCIO}).

Figure 20. Output Drive Characteristics of FLEX 10K Devices

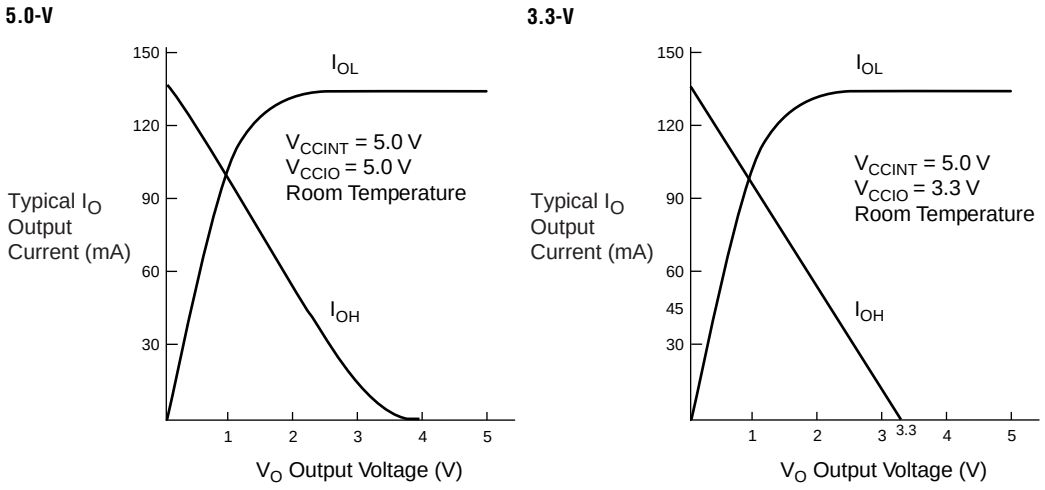


Table 27. FLEX 10KA 3.3-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3)*, *(4)*	2.30 (2.30)	2.70 (2.70)	V
V_I	Input voltage	*(5)*	–0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Figures 25 through 27 show the delays that correspond to various paths and functions within the LE, IOE, and EAB timing models.

Figure 25. FLEX 10K Device LE Timing Model

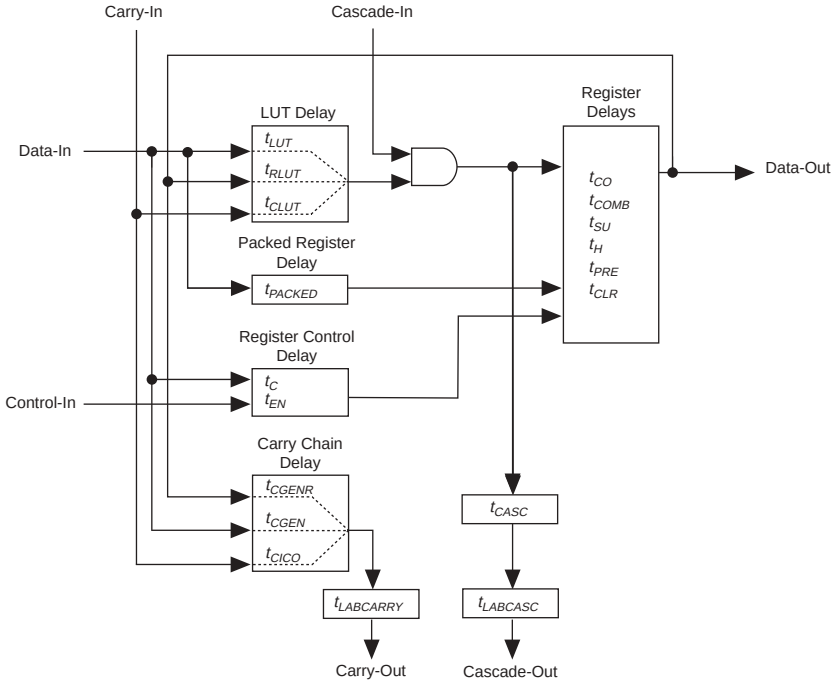
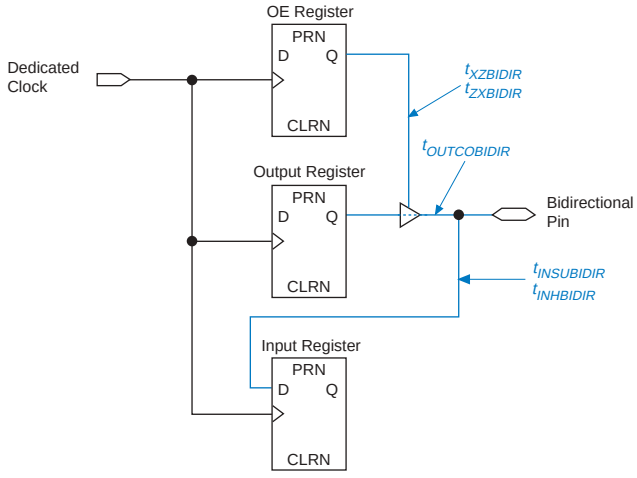


Figure 28. Synchronous Bidirectional Pin External Timing Model



Tables 32 through 36 describe the FLEX 10K device internal timing parameters. These internal timing parameters are expressed as worst-case values. Using hand calculations, these parameters can be used to estimate design performance. However, before committing designs to silicon, actual worst-case performance should be modeled using timing simulation and analysis. Tables 37 through 38 describe FLEX 10K external timing parameters.

Table 32. LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions
t_{LUT}	LUT delay for data-in	
t_{CLUT}	LUT delay for carry-in	
t_{RLUT}	LUT delay for LE register feedback	
t_{PACKED}	Data-in to packed register delay	
t_{EN}	LE register enable delay	
t_{CICO}	Carry-in to carry-out delay	
t_{CGEN}	Data-in to carry-out delay	
t_{CGENR}	LE register feedback to carry-out delay	
t_{CASC}	Cascade-in to cascade-out delay	
t_{C}	LE register control signal delay	
t_{CO}	LE register clock-to-output delay	
t_{COMB}	Combinatorial delay	

Notes to tables:

(1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.

(2) Operating conditions: V_{CCIO} = 5.0 V ± 5% for commercial use in FLEX 10K devices.
V_{CCIO} = 5.0 V ± 10% for industrial use in FLEX 10K devices.
V_{CCIO} = 3.3 V ± 10% for commercial or industrial use in FLEX 10KA devices.

(3) Operating conditions: V_{CCIO} = 3.3 V ± 10% for commercial or industrial use in FLEX 10K devices.
V_{CCIO} = 2.5 V ± 0.2 V for commercial or industrial use in FLEX 10KA devices.

(4) Operating conditions: V_{CCIO} = 2.5 V, 3.3 V, or 5.0 V.

(5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the WE signal is registered.

(6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.

(7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.

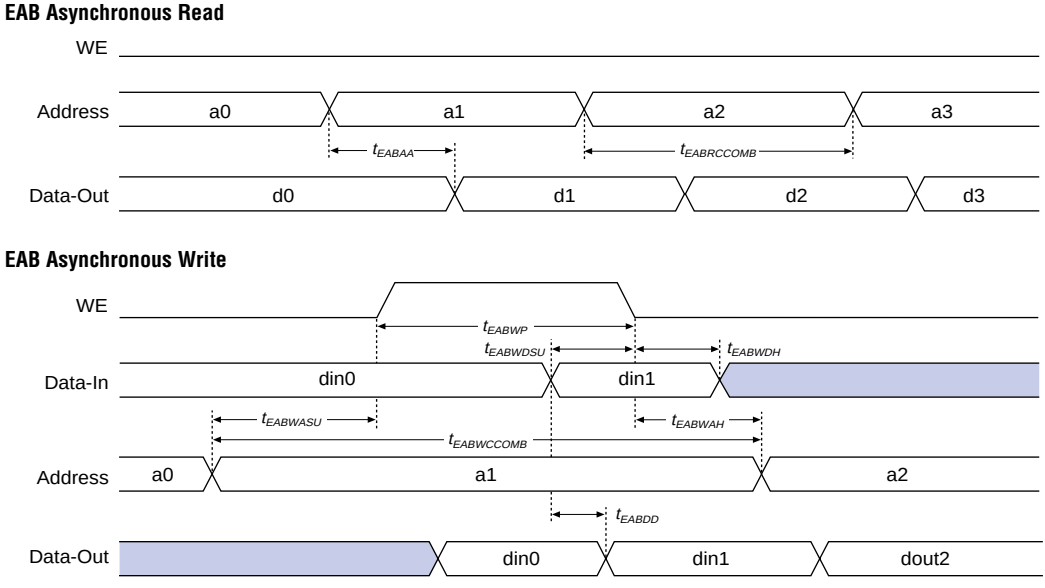
(8) External reference timing parameters are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.

(9) Contact Altera Applications for test circuit specifications and test conditions.

(10) These timing parameters are sample-tested only.

Figures 29 and 30 show the asynchronous and synchronous timing waveforms, respectively, for the EAB macroparameters in Table 34.

Figure 29. EAB Asynchronous Timing Waveforms



Tables 39 through 47 show EPF10K10 and EPF10K20 device internal and external timing parameters.

Table 39. EPF10K10 & EPF10K20 Device LE Timing Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{LUT}		1.4		1.7	ns
t_{CLUT}		0.6		0.7	ns
t_{RLUT}		1.5		1.9	ns
t_{PACKED}		0.6		0.9	ns
t_{EN}		1.0		1.2	ns
t_{CICO}		0.2		0.3	ns
t_{CGEN}		0.9		1.2	ns
t_{CGENR}		0.9		1.2	ns
t_{CASC}		0.8		0.9	ns
t_{C}		1.3		1.5	ns
t_{CO}		0.9		1.1	ns
t_{COMB}		0.5		0.6	ns
t_{SU}	1.3		2.5		ns
t_{H}	1.4		1.6		ns
t_{PRE}		1.0		1.2	ns
t_{CLR}		1.0		1.2	ns
t_{CH}	4.0		4.0		ns
t_{CL}	4.0		4.0		ns

Table 51. EPF10K30, EPF10K40 & EPF10K50 Device EAB Internal Timing Macroparameters *Note (1)*					
Symbol	**-3 Speed Grade**		**-4 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	
t_{EABAA}		13.7		17.0	ns
$t_{EABRCCOMB}$	13.7		17.0		ns
$t_{EABRCREG}$	9.7		11.9		ns
t_{EABWP}	5.8		7.2		ns
$t_{EABWCCOMB}$	7.3		9.0		ns
$t_{EABWCREG}$	13.0		16.0		ns
t_{EABDD}		10.0		12.5	ns
$t_{EABDATACO}$		2.0		3.4	ns
$t_{EABDATASU}$	5.3		5.6		ns
$t_{EABDATAH}$	0.0		0.0		ns
$t_{EABWESU}$	5.5		5.8		ns
t_{EABWEH}	0.0		0.0		ns
$t_{EABWDSU}$	5.5		5.8		ns
t_{EABWDH}	0.0		0.0		ns
$t_{EABWASU}$	2.1		2.7		ns
t_{EABWAH}	0.0		0.0		ns
t_{EABWO}		9.5		11.8	ns

Notes to tables:
(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Tables 64 through 70 show EPF10K100 device internal and external timing parameters.

Table 64. EPF10K100 Device LE Timing Microparameters *Note (1)*

Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		1.5		1.5		2.0	ns
t_{CLUT}		0.4		0.4		0.5	ns
t_{RLUT}		1.6		1.6		2.0	ns
t_{PACKED}		0.9		0.9		1.3	ns
t_{EN}		0.9		0.9		1.2	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		1.1		1.1		1.4	ns
t_{CGENR}		1.2		1.2		1.5	ns
t_{CASC}		1.1		1.1		1.3	ns
t_{C}		0.8		0.8		1.0	ns
t_{CO}		1.0		1.0		1.4	ns
t_{COMB}		0.5		0.5		0.7	ns
t_{SU}	2.1		2.1		2.6		ns
t_{H}	2.3		2.3		3.1		ns
t_{PRE}		1.0		1.0		1.4	ns
t_{CLR}		1.0		1.0		1.4	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns

Table 65. EPF10K100 Device IOE Timing Microparameters *Note (1)*

Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.0		0.0		0.0	ns
t_{IOC}		0.5		0.5		0.7	ns
t_{IOCO}		0.4		0.4		0.9	ns
t_{IOCOMB}		0.0		0.0		0.0	ns
t_{IOSU}	5.5		5.5		6.7		ns
t_{IOH}	0.5		0.5		0.7		ns
t_{IOCLR}		0.7		0.7		1.6	ns
t_{OD1}		4.0		4.0		5.0	ns
t_{OD2}		6.3		6.3		7.3	ns
t_{OD3}		7.7		7.7		8.7	ns
t_{XZ}		6.2		6.2		6.8	ns
t_{ZX1}		6.2		6.2		6.8	ns
t_{ZX2}		8.5		8.5		9.1	ns
t_{ZX3}		9.9		9.9		10.5	ns
t_{INREG} without ClockLock or ClockBoost circuitry		9.0		9.0		10.5	ns
t_{INREG} with ClockLock or ClockBoost circuitry		3.0		–		–	ns
t_{IOFD}		8.1		8.1		10.3	ns
t_{INCOMB}		8.1		8.1		10.3	ns

Table 82. EPF10K130V Device Interconnect Timing Microparameters *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		8.0		9.0		9.5	ns
t_{DIN2LE}		2.4		3.0		3.1	ns
$t_{DIN2DATA}$		5.0		6.3		7.4	ns
$t_{DCLK2IOE}$		3.6		4.6		5.1	ns
$t_{DCLK2LE}$		2.4		3.0		3.1	ns
$t_{SAMELAB}$		0.4		0.6		0.8	ns
$t_{SAMEROW}$		4.5		5.3		6.5	ns
$t_{SAMECOLUMN}$		9.0		9.5		9.7	ns
$t_{DIFFROW}$		13.5		14.8		16.2	ns
$t_{TWOROWS}$		18.0		20.1		22.7	ns
$t_{LEPERIPH}$		8.1		8.6		9.5	ns
$t_{LABCARRY}$		0.6		0.8		1.0	ns
$t_{LABCASC}$		0.8		1.0		1.2	ns

Table 83. EPF10K130V Device External Timing Parameters *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		15.0		19.1		24.2	ns
t_{INSU} *(2)*, *(3)*	6.9		8.6		11.0		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	7.8	2.0	9.9	2.0	11.3	ns

Table 84. EPF10K130V Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	6.7		8.5		10.8		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	6.9	2.0	8.8	2.0	10.2	ns
$t_{XZBIDIR}$		12.9		16.4		19.3	ns
$t_{ZXBIDIR}$		12.9		16.4		19.3	ns

Table 87. EPF10K10A Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		3.3		3.9		5.2	ns
$t_{EABDATA2}$		1.0		1.3		1.7	ns
t_{EABWE1}		2.6		3.1		4.1	ns
t_{EABWE2}		2.7		3.2		4.3	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		1.2		1.4		1.8	ns
$t_{EABBYPASS}$		0.1		0.2		0.2	ns
t_{EABSU}	1.4		1.7		2.2		ns
t_{EABH}	0.1		0.1		0.1		ns
t_{AA}		4.5		5.4		7.3	ns
t_{WP}	2.0		2.4		3.2		ns
t_{WDSU}	0.7		0.8		1.1		ns
t_{WDH}	0.5		0.6		0.7		ns
t_{WASU}	0.6		0.7		0.9		ns
t_{WAH}	0.9		1.1		1.5		ns
t_{WO}		3.3		3.9		5.2	ns
t_{DD}		3.3		3.9		5.2	ns
t_{EABOUT}		0.1		0.1		0.2	ns
t_{EABCH}	3.0		3.5		4.0		ns
t_{EABCL}	3.03		3.5		4.0		ns

Table 95. EPF10K30A Device EAB Internal Timing Macroparameters *Note (1)*							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		9.7		11.6		16.2	ns
$t_{EABRCCOMB}$	9.7		11.6		16.2		ns
$t_{EABRCREG}$	5.9		7.1		9.7		ns
t_{EABWP}	3.8		4.5		5.9		ns
$t_{EABWCCOMB}$	4.0		4.7		6.3		ns
$t_{EABWCREG}$	9.8		11.6		16.6		ns
t_{EABDD}		9.2		11.0		16.1	ns
$t_{EABDATACO}$		1.7		2.1		3.4	ns
$t_{EABDATASU}$	2.3		2.7		3.5		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	3.3		3.9		4.9		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	3.2		3.8		5.0		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.7		4.4		5.1		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		6.1		7.3		11.3	ns

Table 103. EPF10K100A Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		4.8		5.4		6.0	ns
t_{DIN2LE}		2.0		2.4		2.7	ns
$t_{DIN2DATA}$		2.4		2.7		2.9	ns
$t_{DCLK2IOE}$		2.6		3.0		3.5	ns
$t_{DCLK2LE}$		2.0		2.4		2.7	ns
$t_{SAMELAB}$		0.1		0.1		0.1	ns
$t_{SAMEROW}$		1.5		1.7		1.9	ns
$t_{SAMECOLUMN}$		5.5		6.5		7.4	ns
$t_{DIFFROW}$		7.0		8.2		9.3	ns
$t_{TWOROWS}$		8.5		9.9		11.2	ns
$t_{LEPERIPH}$		3.9		4.2		4.5	ns
$t_{LABCARRY}$		0.2		0.2		0.3	ns
$t_{LABCASC}$		0.4		0.5		0.6	ns

Table 104. EPF10K100A Device External Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		12.5		14.5		17.0	ns
t_{INSU} *(2)*, *(3)*	3.7		4.5		5.1		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	5.3	2.0	6.1	2.0	7.2	ns

Table 105. EPF10K100A Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	4.9		5.8		6.8		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	5.3	2.0	6.1	2.0	7.2	ns
$t_{XZBIDIR}$		7.4		8.6		10.1	ns
$t_{ZXBIDIR}$		7.4		8.6		10.1	ns

Table 110. EPF10K250A Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		7.8		8.5		9.4	ns
t_{DIN2LE}		2.7		3.1		3.5	ns
$t_{DIN2DATA}$		1.6		1.6		1.7	ns
$t_{DCLK2IOE}$		3.6		4.0		4.6	ns
$t_{DCLK2LE}$		2.7		3.1		3.5	ns
$t_{SAMELAB}$		0.2		0.3		0.3	ns
$t_{SAMEROW}$		6.7		7.3		8.2	ns
$t_{SAMECOLUMN}$		2.5		2.7		3.0	ns
$t_{DIFFROW}$		9.2		10.0		11.2	ns
$t_{TWOROWS}$		15.9		17.3		19.4	ns
$t_{LEPERIPH}$		7.5		8.1		8.9	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.4		0.4		0.5	ns

Table 111. EPF10K250A Device External Reference Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		15.0		17.0		20.0	ns
t_{INSU} *(2), (3)*	6.9		8.0		9.4		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	8.0	2.0	8.9	2.0	10.4	ns

Table 112. EPF10K250A Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	9.3		10.6		12.7		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	8.0	2.0	8.9	2.0	10.4	ns
$t_{XZBIDIR}$		10.8		12.2		14.2	ns
$t_{ZXBIDIR}$		10.8		12.2		14.2	ns

Table 113. ClockLock & ClockBoost Parameters (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
$f_{CLKDEV1}$	Input deviation from user specification in MAX+PLUS II (ClockBoost clock multiplication factor equals 1) *(1)*			±1	MHz
$f_{CLKDEV2}$	Input deviation from user specification in MAX+PLUS II (ClockBoost clock multiplication factor equals 2) *(1)*			±0.5	MHz
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)			100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock *(2)*			10	µs
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock *(3)*			1	ns
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock	40	50	60	%

Notes:

(1) To implement the ClockLock and ClockBoost circuitry with the MAX+PLUS II software, designers must specify the input frequency. The MAX+PLUS II software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The f_{CLKDEV} parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.

(2) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the t_{LOCK} value is less than the time required for configuration.

(3) The t_{JITTER} specification is measured under long-term observation.

Power Consumption

The supply power (P) for FLEX 10K devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

Typical $I_{CCSTANDBY}$ values are shown as I_{CC0} in the FLEX 10K device DC operating conditions tables on pages 46, 49, and 52 of this data sheet. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value is calculated based on the amount of current that each LE typically consumes. The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

Compared to the rest of the device, the embedded array consumes a negligible amount of power. Therefore, the embedded array can be ignored when calculating supply current.

The $I_{CCACTIVE}$ value is calculated with the following equation:

$$I_{CCACTIVE} = K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}} \times \frac{\mu A}{MHz \times LE}$$

The parameters in this equation are shown below: