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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	360
Number of Logic Elements/Cells	2880
Total RAM Bits	20480
Number of I/O	189
Number of Gates	116000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-RQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k50vrc240-2n

Table 2. FLEX 10K Device Features

Feature	EPF10K70	EPF10K100 EPF10K100A	EPF10K130V	EPF10K250A
Typical gates (logic and RAM) *(1)*	70,000	100,000	130,000	250,000
Maximum system gates	118,000	158,000	211,000	310,000
LEs	3,744	4,992	6,656	12,160
LABs	468	624	832	1,520
EABs	9	12	16	20
Total RAM bits	18,432	24,576	32,768	40,960
Maximum user I/O pins	358	406	470	470

Note to tables:

(1) The embedded IEEE Std. 1149.1 JTAG circuitry adds up to 31,250 gates in addition to the listed typical or maximum system gates.

...and More Features

- Devices are fabricated on advanced processes and operate with a 3.3-V or 5.0-V supply voltage (see Table 3
- In-circuit reconfigurability (ICR) via external configuration device, intelligent controller, or JTAG port
- ClockLock™ and ClockBoost™ options for reduced clock delay/skew and clock multiplication
- Built-in low-skew clock distribution trees
- 100% functional testing of all devices; test vectors or scan chains are not required

Table 3. Supply Voltages for FLEX 10K & FLEX 10KA Devices

5.0-V Devices	3.3-V Devices
EPF10K10 EPF10K20 EPF10K30 EPF10K40 EPF10K50 EPF10K70 EPF10K100	EPF10K10A EPF10K30A EPF10K50V EPF10K100A EPF10K130V EPF10K250A

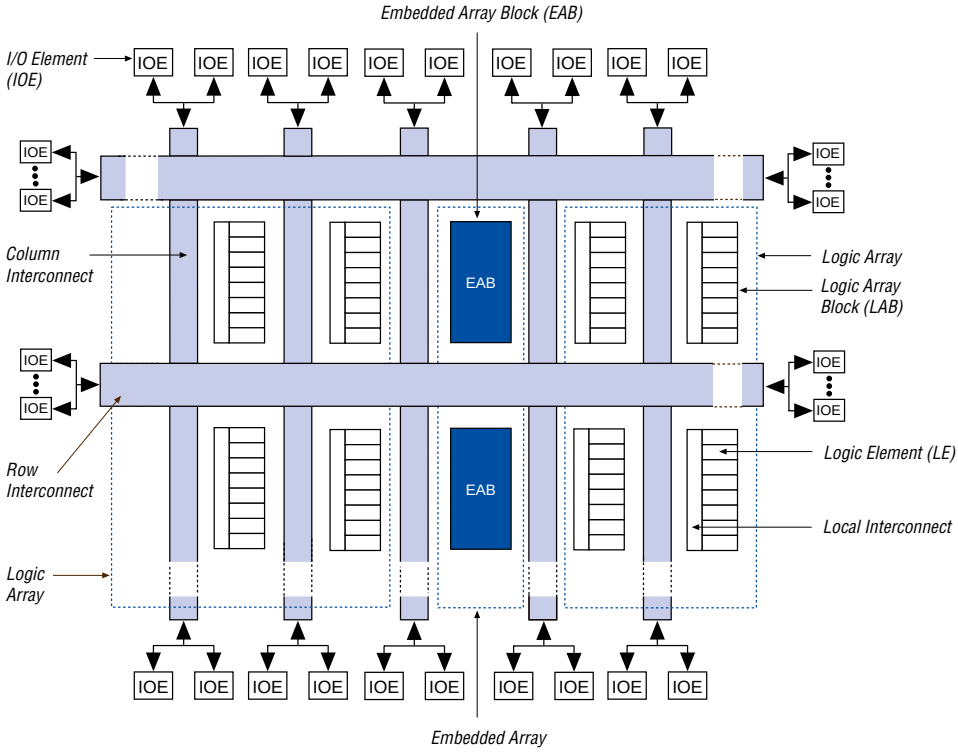
The FLEX 10K architecture is similar to that of embedded gate arrays, the fastest-growing segment of the gate array market. As with standard gate arrays, embedded gate arrays implement general logic in a conventional "sea-of-gates" architecture. In addition, embedded gate arrays have dedicated die areas for implementing large, specialized functions. By embedding functions in silicon, embedded gate arrays provide reduced die area and increased speed compared to standard gate arrays. However, embedded megafunctions typically cannot be customized, limiting the designer's options. In contrast, FLEX 10K devices are programmable, providing the designer with full control over embedded megafunctions and general logic while facilitating iterative design changes during debugging.

Each FLEX 10K device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), microcontroller, wide-data-path manipulation, and data-transformation functions. The logic array performs the same function as the sea-of-gates in the gate array: it is used to implement general logic, such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

FLEX 10K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers the EPC1, EPC2, EPC16, and EPC1441 configuration devices, which configure FLEX 10K devices via a serial data stream. Configuration data can also be downloaded from system RAM or from Altera's BitBlaster™ serial download cable or ByteBlasterMV™ parallel port download cable. After a FLEX 10K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 320 ms, real-time changes can be made during system operation.

FLEX 10K devices contain an optimized interface that permits microprocessors to configure FLEX 10K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat a FLEX 10K device as memory and configure the device by writing to a virtual memory location, making it very easy for the designer to reconfigure the device.

Figure 1. FLEX 10K Device Block Diagram



FLEX 10K devices provide six dedicated inputs that drive the flipflops' control inputs to ensure the efficient distribution of high-speed, low-skew (less than 1.5 ns) control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

Embedded Array Block

The EAB is a flexible block of RAM with registers on the input and output ports, and is used to implement common gate array megafunctions. The EAB is also suitable for functions such as multipliers, vector scalars, and error correction circuits, because it is large and flexible. These functions can be combined in applications such as digital filters and microcontrollers.

For improved routing, the row interconnect is comprised of a combination of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in half of the row. The EAB can be driven by the half-length channels in the left half of the row and by the full-length channels. The EAB drives out to the full-length channels. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-row channel, thereby saving the other half of the channel for the other half of the row.

Table 7 summarizes the FastTrack Interconnect resources available in each FLEX 10K device.

Table 7. FLEX 10K FastTrack Interconnect Resources

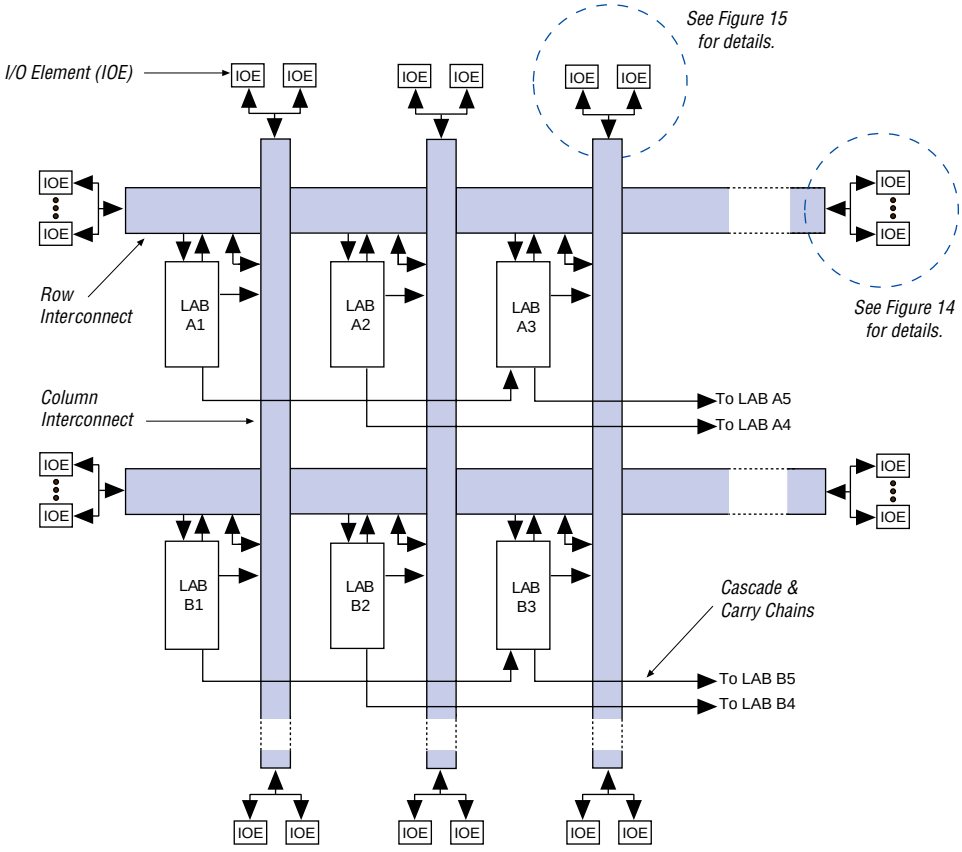
Device	Rows	Channels per Row	Columns	Channels per Column
EPF10K10 EPF10K10A	3	144	24	24
EPF10K20	6	144	24	24
EPF10K30 EPF10K30A	6	216	36	24
EPF10K40	8	216	36	24
EPF10K50 EPF10K50V	10	216	36	24
EPF10K70	9	312	52	24
EPF10K100 EPF10K100A	12	312	52	24
EPF10K130V	16	312	52	32
EPF10K250A	20	456	76	40

In addition to general-purpose I/O pins, FLEX 10K devices have six dedicated input pins that provide low-skew signal distribution across the device. These six inputs can be used for global clock, clear, preset, and peripheral output enable and clock enable control signals. These signals are available as control signals for all LABs and IOEs in the device.

The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device. However, the use of dedicated inputs as data inputs can introduce additional delay into the control signal network.

Figure 12 shows the interconnection of adjacent LABs and EABs with row, column, and local interconnects, as well as the associated cascade and carry chains. Each LAB is labeled according to its location: a letter represents the row and a number represents the column. For example, LAB B3 is in row B, column 3.

Figure 12. Interconnect Resources



Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces system noise and adds a maximum delay of approximately 2.9 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a device-wide basis. The slow slew rate setting affects only the falling edge of the output.

Open-Drain Output Option

FLEX 10K devices provide an optional open-drain (electrically equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane. Additionally, the Altera software can convert tri-state buffers with grounded data inputs to open-drain pins automatically.

Open-drain output pins on FLEX 10K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Output pins on 5.0-V FLEX 10K devices with V_{CCIO} = 3.3 V or 5.0 V (with a pull-up resistor to the 5.0-V supply) can also drive 5.0-V CMOS input pins. In this case, the pull-up transistor will turn off when the pin voltage exceeds 3.3 V. Therefore, the pin does not have to be open-drain.

MultiVolt I/O Interface

The FLEX 10K device architecture supports the MultiVolt I/O interface feature, which allows FLEX 10K devices to interface with systems of differing supply voltages. These devices have one set of V_{CC} pins for internal operation and input buffers (VCCINT) and another set for I/O output drivers (VCCIO).

Table 12 describes the FLEX 10K device supply voltages and MultiVolt I/O support levels.

Table 12. Supply Voltages & MultiVolt I/O Support Levels

Devices	Supply Voltage (V)		MultiVolt I/O Support Levels (V)	
	V_{CCINT}	V_{CCIO}	Input	Output
FLEX 10K *(1)*	5.0	5.0	3.3 or 5.0	5.0
	5.0	3.3	3.3 or 5.0	3.3 or 5.0
EPF10K50V *(1)*	3.3	3.3	3.3 or 5.0	3.3 or 5.0
EPF10K130V	3.3	3.3	3.3 or 5.0	3.3 or 5.0
FLEX 10KA *(1)*	3.3	3.3	2.5, 3.3, or 5.0	3.3 or 5.0
	3.3	2.5	2.5, 3.3, or 5.0	2.5

Note
(1) 240-pin QFP packages do not support the MultiVolt I/O features, so they do not have separate V_{CCIO} pins.

Power Sequencing & Hot-Socketing

Because FLEX 10K devices can be used in a multi-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power supplies can be powered in any order.

Signals can be driven into FLEX 10KA devices before and during power up without damaging the device. Additionally, FLEX 10KA devices do not drive out during power up. Once operating conditions are reached, FLEX 10KA devices operate as specified by the user.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All FLEX 10K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. All FLEX 10K devices can also be configured using the JTAG pins through the BitBlaster serial download cable, or ByteBlasterMV parallel port download cable, or via hardware that uses the Jam™ programming and test language. JTAG BST can be performed before or after configuration, but not during configuration. FLEX 10K devices support the JTAG instructions shown in Table 13.

Table 35. EAB Timing Macroparameters *Notes (1), (6)*		
Symbol	**Parameter**	**Conditions**
t_{EABAA}	EAB address access delay	
$t_{EABRCCOMB}$	EAB asynchronous read cycle time	
$t_{EABRCREG}$	EAB synchronous read cycle time	
t_{EABWP}	EAB write pulse width	
$t_{EABWCCOMB}$	EAB asynchronous write cycle time	
$t_{EABWCREG}$	EAB synchronous write cycle time	
t_{EABDD}	EAB data-in to data-out valid delay	
$t_{EABDATACO}$	EAB clock-to-output delay when using output registers	
$t_{EABDATASU}$	EAB data/address setup time before clock when using input register	
$t_{EABDATAH}$	EAB data/address hold time after clock when using input register	
$t_{EABWESU}$	EAB WE setup time before clock when using input register	
t_{EABWEH}	EAB WE hold time after clock when using input register	
$t_{EABWDSU}$	EAB data setup time before falling edge of write pulse when not using input registers	
t_{EABWDH}	EAB data hold time after falling edge of write pulse when not using input registers	
$t_{EABWASU}$	EAB address setup time before rising edge of write pulse when not using input registers	
t_{EABWAH}	EAB address hold time after falling edge of write pulse when not using input registers	
t_{EABWO}	EAB write enable to data output valid delay	

Table 40. EPF10K10 & EPF10K20 Device IOE Timing Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{IOD}		1.3		1.6	ns
t_{IOC}		0.5		0.7	ns
t_{IOCO}		0.2		0.2	ns
t_{IOCOMB}		0.0		0.0	ns
t_{IOSU}	2.8		3.2		ns
t_{IOH}	1.0		1.2		ns
t_{IOCLR}		1.0		1.2	ns
t_{OD1}		2.6		3.5	ns
t_{OD2}		4.9		6.4	ns
t_{OD3}		6.3		8.2	ns
t_{XZ}		4.5		5.4	ns
t_{ZX1}		4.5		5.4	ns
t_{ZX2}		6.8		8.3	ns
t_{ZX3}		8.2		10.1	ns
t_{INREG}		6.0		7.5	ns
t_{IOFD}		3.1		3.5	ns
t_{INCOMB}		3.1		3.5	ns

Table 41. EPF10K10 & EPF10K20 Device EAB Internal Microparameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{EABDATA1}$		1.5		1.9	ns
$t_{EABDATA2}$		4.8		6.0	ns
t_{EABWE1}		1.0		1.2	ns
t_{EABWE2}		5.0		6.2	ns
t_{EABCLK}		1.0		2.2	ns
t_{EABCO}		0.5		0.6	ns
$t_{EABBYPASS}$		1.5		1.9	ns
t_{EABSU}	1.5		1.8		ns
t_{EABH}	2.0		2.5		ns
t_{AA}		8.7		10.7	ns
t_{WP}	5.8		7.2		ns
t_{WDSU}	1.6		2.0		ns
t_{WDH}	0.3		0.4		ns
t_{WASU}	0.5		0.6		ns
t_{WAH}	1.0		1.2		ns
t_{WO}		5.0		6.2	ns
t_{DD}		5.0		6.2	ns
t_{EABOUT}		0.5		0.6	ns
t_{EABCH}	4.0		4.0		ns
t_{EABCL}	5.8		7.2		ns

Table 59. EPF10K70 Device EAB Internal Microparameters *Note (1)*

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.3		1.5		1.9	ns
$t_{EABDATA2}$		4.3		4.8		6.0	ns
t_{EABWE1}		0.9		1.0		1.2	ns
t_{EABWE2}		4.5		5.0		6.2	ns
t_{EABCLK}		0.9		1.0		2.2	ns
t_{EABCO}		0.4		0.5		0.6	ns
$t_{EABBYPASS}$		1.3		1.5		1.9	ns
t_{EABSU}	1.3		1.5		1.8		ns
t_{EABH}	1.8		2.0		2.5		ns
t_{AA}		7.8		8.7		10.7	ns
t_{WP}	5.2		5.8		7.2		ns
t_{WDSU}	1.4		1.6		2.0		ns
t_{WDH}	0.3		0.3		0.4		ns
t_{WASU}	0.4		0.5		0.6		ns
t_{WAH}	0.9		1.0		1.2		ns
t_{WO}		4.5		5.0		6.2	ns
t_{DD}		4.5		5.0		6.2	ns
t_{EABOUT}		0.4		0.5		0.6	ns
t_{EABCH}	4.0		4.0		4.0		ns
t_{EABCL}	5.2		5.8		7.2		ns

Notes to tables:
(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Tables 64 through 70 show EPF10K100 device internal and external timing parameters.

Table 64. EPF10K100 Device LE Timing Microparameters *Note (1)*

Symbol	-3DX Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		1.5		1.5		2.0	ns
t_{CLUT}		0.4		0.4		0.5	ns
t_{RLUT}		1.6		1.6		2.0	ns
t_{PACKED}		0.9		0.9		1.3	ns
t_{EN}		0.9		0.9		1.2	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		1.1		1.1		1.4	ns
t_{CGENR}		1.2		1.2		1.5	ns
t_{CASC}		1.1		1.1		1.3	ns
t_{C}		0.8		0.8		1.0	ns
t_{CO}		1.0		1.0		1.4	ns
t_{COMB}		0.5		0.5		0.7	ns
t_{SU}	2.1		2.1		2.6		ns
t_{H}	2.3		2.3		3.1		ns
t_{PRE}		1.0		1.0		1.4	ns
t_{CLR}		1.0		1.0		1.4	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns

Tables 71 through 77 show EPF10K50V device internal and external timing parameters.

Table 71. EPF10K50V Device LE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.9		1.0		1.3		1.6	ns
t_{CLUT}		0.1		0.5		0.6		0.6	ns
t_{RLUT}		0.5		0.8		0.9		1.0	ns
t_{PACKED}		0.4		0.4		0.5		0.7	ns
t_{EN}		0.7		0.9		1.1		1.4	ns
t_{CICO}		0.2		0.2		0.2		0.3	ns
t_{CGEN}		0.8		0.7		0.8		1.2	ns
t_{CGENR}		0.4		0.3		0.3		0.4	ns
t_{CASC}		0.7		0.7		0.8		0.9	ns
t_{C}		0.3		1.0		1.3		1.5	ns
t_{CO}		0.5		0.7		0.9		1.0	ns
t_{COMB}		0.4		0.4		0.5		0.6	ns
t_{SU}	0.8		1.6		2.2		2.5		ns
t_{H}	0.5		0.8		1.0		1.4		ns
t_{PRE}		0.8		0.4		0.5		0.5	ns
t_{CLR}		0.8		0.4		0.5		0.5	ns
t_{CH}	2.0		4.0		4.0		4.0		ns
t_{CL}	2.0		4.0		4.0		4.0		ns

Table 87. EPF10K10A Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		3.3		3.9		5.2	ns
$t_{EABDATA2}$		1.0		1.3		1.7	ns
t_{EABWE1}		2.6		3.1		4.1	ns
t_{EABWE2}		2.7		3.2		4.3	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		1.2		1.4		1.8	ns
$t_{EABBYPASS}$		0.1		0.2		0.2	ns
t_{EABSU}	1.4		1.7		2.2		ns
t_{EABH}	0.1		0.1		0.1		ns
t_{AA}		4.5		5.4		7.3	ns
t_{WP}	2.0		2.4		3.2		ns
t_{WDSU}	0.7		0.8		1.1		ns
t_{WDH}	0.5		0.6		0.7		ns
t_{WASU}	0.6		0.7		0.9		ns
t_{WAH}	0.9		1.1		1.5		ns
t_{WO}		3.3		3.9		5.2	ns
t_{DD}		3.3		3.9		5.2	ns
t_{EABOUT}		0.1		0.1		0.2	ns
t_{EABCH}	3.0		3.5		4.0		ns
t_{EABCL}	3.03		3.5		4.0		ns

Table 93. EPF10K30A Device IOE Timing Microparameters *Note (1)* ***(Part 2 of 2)***

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{IOH}	0.9		1.1		1.4		ns
t_{IOCLR}		0.7		0.8		1.0	ns
t_{OD1}		1.9		2.2		2.9	ns
t_{OD2}		4.8		5.6		7.3	ns
t_{OD3}		7.0		8.2		10.8	ns
t_{XZ}		2.2		2.6		3.4	ns
t_{ZX1}		2.2		2.6		3.4	ns
t_{ZX2}		5.1		6.0		7.8	ns
t_{ZX3}		7.3		8.6		11.3	ns
t_{INREG}		4.4		5.2		6.8	ns
t_{IOFD}		3.8		4.5		5.9	ns
t_{INCOMB}		3.8		4.5		5.9	ns

Table 95. EPF10K30A Device EAB Internal Timing Macroparameters *Note (1)*							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{EABAA}		9.7		11.6		16.2	ns
$t_{EABRCCOMB}$	9.7		11.6		16.2		ns
$t_{EABRCREG}$	5.9		7.1		9.7		ns
t_{EABWP}	3.8		4.5		5.9		ns
$t_{EABWCCOMB}$	4.0		4.7		6.3		ns
$t_{EABWCREG}$	9.8		11.6		16.6		ns
t_{EABDD}		9.2		11.0		16.1	ns
$t_{EABDATACO}$		1.7		2.1		3.4	ns
$t_{EABDATASU}$	2.3		2.7		3.5		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	3.3		3.9		4.9		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	3.2		3.8		5.0		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.7		4.4		5.1		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		6.1		7.3		11.3	ns

Notes to tables:
(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Tables 106 through 112 show EPF10K250A device internal and external timing parameters.

Table 106. EPF10K250A Device LE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.9		1.0		1.4	ns
t_{CLUT}		1.2		1.3		1.6	ns
t_{RLUT}		2.0		2.3		2.7	ns
t_{PACKED}		0.4		0.4		0.5	ns
t_{EN}		1.4		1.6		1.9	ns
t_{CICO}		0.2		0.3		0.3	ns
t_{CGEN}		0.4		0.6		0.6	ns
t_{CGENR}		0.8		1.0		1.1	ns
t_{CASC}		0.7		0.8		1.0	ns
t_{C}		1.2		1.3		1.6	ns
t_{CO}		0.6		0.7		0.9	ns
t_{COMB}		0.5		0.6		0.7	ns
t_{SU}	1.2		1.4		1.7		ns
t_{H}	1.2		1.3		1.6		ns
t_{PRE}		0.7		0.8		0.9	ns
t_{CLR}		0.7		0.8		0.9	ns
t_{CH}	2.5		3.0		3.5		ns
t_{CL}	2.5		3.0		3.5		ns

Table 109. EPF10K250A Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		6.1		6.8		8.2	ns
$t_{EABRCCOMB}$	6.1		6.8		8.2		ns
$t_{EABRCREG}$	4.6		5.1		6.1		ns
t_{EABWP}	5.6		6.4		7.5		ns
$t_{EABWCCOMB}$	5.8		6.6		7.9		ns
$t_{EABWCREG}$	15.8		17.8		21.0		ns
t_{EABDD}		5.7		6.4		7.8	ns
$t_{EABDATACO}$		0.7		0.8		1.0	ns
$t_{EABDATASU}$	4.5		5.1		5.9		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	8.2		9.3		10.9		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.7		1.8		2.1		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	0.9		0.9		1.0		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		5.3		6.0		7.4	ns

$\mathbf{f_{MAX}}$ = Maximum operating frequency in MHz
N = Total number of logic cells used in the device
$\mathbf{tog_{LC}}$ = Average percent of logic cells toggling at each clock (typically 12.5%)
K = Constant, shown in Tables 114 and 115

Table 114. FLEX 10K K Constant Values

Device	K Value
EPF10K10	82
EPF10K20	89
EPF10K30	88
EPF10K40	92
EPF10K50	95
EPF10K70	85
EPF10K100	88

Table 115. FLEX 10KA K Constant Values

Device	K Value
EPF10K10A	17
EPF10K30A	17
EPF10K50V	19
EPF10K100A	19
EPF10K130V	22
EPF10K250A	23

This calculation provides an I_{CC} estimate based on typical conditions with no output load. The actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

To better reflect actual designs, the power model (and the constant *K* in the power calculation equations) for continuous interconnect FLEX devices assumes that logic cells drive FastTrack Interconnect channels. In contrast, the power model of segmented FPGAs assumes that all logic cells drive only one short interconnect segment. This assumption may lead to inaccurate results, compared to measured power consumption for an actual design in a segmented interconnect FPGA.

Figure 32 shows the relationship between the current and operating frequency of FLEX 10K devices.

Notes: