Intel - EPF10K50VRI240-4 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	360
Number of Logic Elements/Cells	2880
Total RAM Bits	20480
Number of I/O	189
Number of Gates	116000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-RQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k50vri240-4

Table 4. FLEX 10K Package Options & I/O Pin Count *Note (1)*

Device	84-Pin PLCC	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP RQFP	240-Pin PQFP RQFP
EPF10K10	59		102	134	
EPF10K10A		66	102	134	
EPF10K20			102	147	189
EPF10K30				147	189
EPF10K30A			102	147	189
EPF10K40				147	189
EPF10K50					189
EPF10K50V					189
EPF10K70					189
EPF10K100					
EPF10K100A					189
EPF10K130V					
EPF10K250A					

Table 5. FLEX 10K Package Options & I/O Pin Count (Continued) *Note (1)*

Device	503-Pin PGA	599-Pin PGA	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	600-Pin BGA	403-Pin PGA
EPF10K10							
EPF10K10A			150		150 *(2)*		
EPF10K20							
EPF10K30				246			
EPF10K30A			191	246	246		
EPF10K40							
EPF10K50				274			310
EPF10K50V				274			
EPF10K70	358						
EPF10K100	406						
EPF10K100A				274	369	406	
EPF10K130V		470				470	
EPF10K250A		470				470	

Notes to tables:
(1) FLEX 10K and FLEX 10KA device package types include plastic J-lead chip carrier (PLCC), thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), ball-grid array (BGA), pin-grid array (PGA), and FineLine BGA^{TM} packages.
(2) This option is supported with a 256-pin FineLine BGA package. By using SameFrame pin migration, all FineLine BGA packages are pin compatible. For example, a board can be designed to support both 256-pin and 484-pin FineLine BGA packages. The Altera software automatically avoids conflicting pins when future migration is set.

General Description

Altera's FLEX 10K devices are the industry's first embedded PLDs. Based on reconfigurable CMOS SRAM elements, the Flexible Logic Element MatriX (FLEX) architecture incorporates all features necessary to implement common gate array megafunctions. With up to 250,000 gates, the FLEX 10K family provides the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device.

FLEX 10K devices are reconfigurable, which allows 100% testing prior to shipment. As a result, the designer is not required to generate test vectors for fault coverage purposes. Additionally, the designer does not need to manage inventories of different ASIC designs; FLEX 10K devices can be configured on the board for the specific functionality required.

Table 6 shows FLEX 10K performance for some common designs. All performance values were obtained with Synopsys DesignWare or LPM functions. No special design technique was required to implement the applications; the designer simply inferred or instantiated a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

Table 6. FLEX 10K & FLEX 10KA Performance

Application	Resources Used		Performance				Units
	LEs	EABs	-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	-4 Speed Grade	
16-bit loadable counter *(1)*	16	0	204	166	125	95	MHz
16-bit accumulator *(1)*	16	0	204	166	125	95	MHz
16-to-1 multiplexer *(2)*	10	0	4.2	5.8	6.0	7.0	ns
256 × 8 RAM read cycle speed *(3)*	0	1	172	145	108	84	MHz
256 × 8 RAM write cycle speed *(3)*	0	1	106	89	68	63	MHz

Notes:
(1) The speed grade of this application is limited because of clock high and low specifications.
(2) This application uses combinatorial inputs and outputs.
(3) This application uses registered inputs and outputs.

For more information, see the following documents:

- *Configuration Devices for APEX & FLEX Devices Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Application Note 116 (Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices)*

FLEX 10K devices are supported by Altera development systems; single, integrated packages that offer schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The Altera software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Altera software works easily with common gate array EDA tools for synthesis and simulation. For example, the Altera software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Altera software contains EDA libraries that use device-specific features such as carry chains which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Altera development systems include DesignWare functions that are optimized for the FLEX 10K architecture.

The Altera development systems run on Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations.

See the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* for more information.

Functional Description

Each FLEX 10K device contains an embedded array to implement memory and specialized logic functions, and a logic array to implement general logic.

The embedded array consists of a series of EABs. When implementing memory functions, each EAB provides 2,048 bits, which can be used to create RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. When implementing logic, each EAB can contribute 100 to 600 gates towards complex logic functions, such as multipliers, microcontrollers, state machines, and DSP functions. EABs can be used independently, or multiple EABs can be combined to implement larger functions.

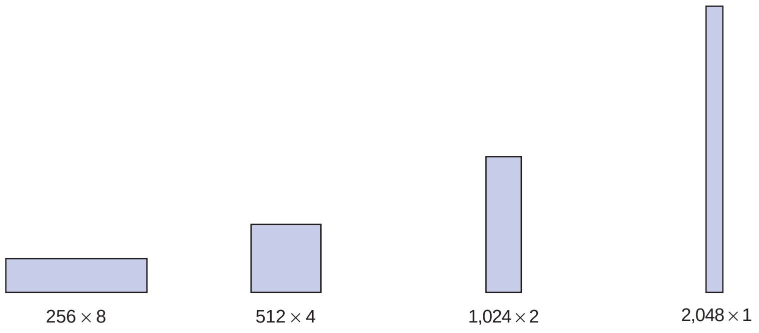
Logic functions are implemented by programming the EAB with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of EABs. The large capacity of EABs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or field-programmable gate array (FPGA) RAM blocks. For example, a single EAB can implement a 4 × 4 multiplier with eight inputs and eight outputs. Parameterized functions such as LPM functions can automatically take advantage of the EAB.

The EAB provides advantages over FPGAs, which implement on-board RAM as arrays of small, distributed RAM blocks. These FPGA RAM blocks contain delays that are less predictable as the size of the RAM increases. In addition, FPGA RAM blocks are prone to routing problems because small blocks of RAM must be connected together to make larger blocks. In contrast, EABs can be used to implement large, dedicated blocks of RAM that eliminate these timing and routing concerns.

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (`WE`) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the `WE` signal. In contrast, the EAB's synchronous RAM generates its own `WE` signal and is self-timed with respect to the global clock. A circuit using the EAB's self-timed RAM need only meet the setup and hold time specifications of the global clock.

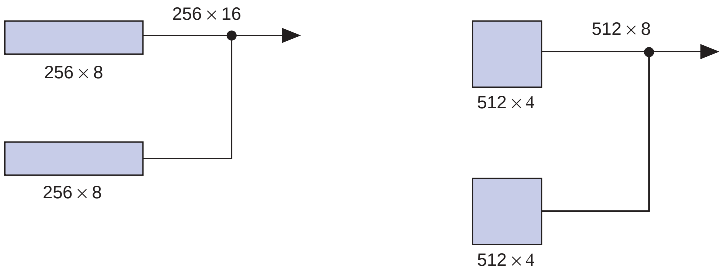
When used as RAM, each EAB can be configured in any of the following sizes: 256 × 8, 512 × 4, 1,024 × 2, or 2,048 × 1. See Figure 2.

Figure 2. EAB Memory Configurations



Larger blocks of RAM are created by combining multiple EABs. For example, two 256 × 8 RAM blocks can be combined to form a 256 × 16 RAM block; two 512 × 4 blocks of RAM can be combined to form a 512 × 8 RAM block. See Figure 3.

Figure 3. Examples of Combining EABs

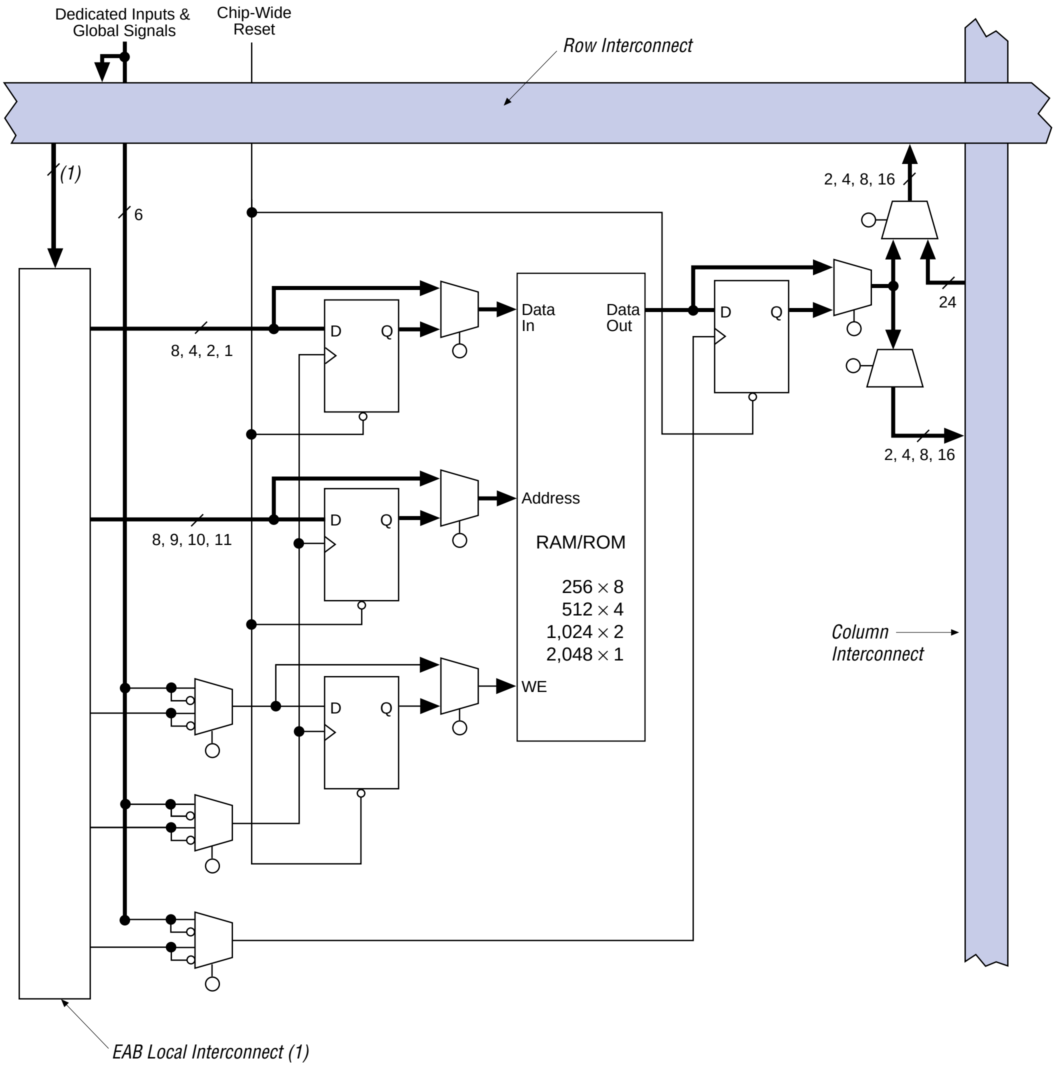


If necessary, all EABs in a device can be cascaded to form a single RAM block. EABs can be cascaded to form RAM blocks of up to 2,048 words without impacting timing. Altera's software automatically combines EABs to meet a designer's RAM specifications.

EABs provide flexible options for driving and controlling clock signals. Different clocks can be used for the EAB inputs and outputs. Registers can be independently inserted on the data input, EAB output, or the address and `WE` inputs. The global signals and the EAB local interconnect can drive the `WE` signal. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control the `WE` signal or the EAB clock signals.

Each EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs. See Figure 4.

Figure 4. FLEX 10K Embedded Array Block



Note:

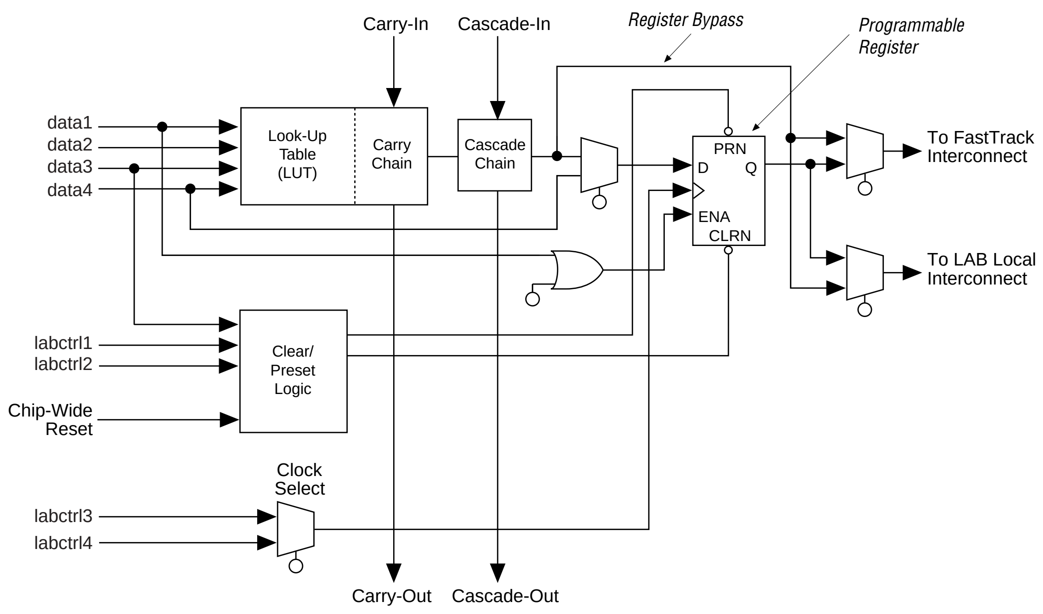
(1) EPF10K10, EPF10K10A, EPF10K20, EPF10K30, EPF10K30A, EPF10K40, EPF10K50, and EPF10K50V devices have 22 EAB local interconnect channels; EPF10K70, EPF10K100, EPF10K100A, EPF10K130V, and EPF10K250A devices have 26.

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks; the other two can be used for clear/preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I/O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I/O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

Logic Element

The LE, the smallest unit of logic in the FLEX 10K architecture, has a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect. See Figure 6.

Figure 6. FLEX 10K Logic Element



Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Compiler automatically selects the carry-in or the `DATA3` signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. Either the register or the LUT can be used to drive both the local interconnect and the FastTrack Interconnect at the same time.

The LUT and the register in the LE can be used independently; this feature is known as register packing. To support register packing, the LE has two outputs; one drives the local interconnect and the other drives the FastTrack Interconnect. The `DATA4` signal can drive the register directly, allowing the LUT to compute a function that is independent of the registered signal; a three-input function can be computed in the LUT, and a fourth independent signal can be registered. Alternatively, a four-input function can be generated, and one of the inputs to this function can be used to drive the register. The register in a packed LE can still use the clock enable, clear, and preset signals in the LE. In a packed LE, the register can drive the FastTrack Interconnect while the LUT drives the local interconnect, or vice versa.

Arithmetic Mode

The arithmetic mode offers 2 three-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT computes a three-input function, and the other generates a carry output. As shown in Figure 9 on page 19, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three signals: `a`, `b`, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

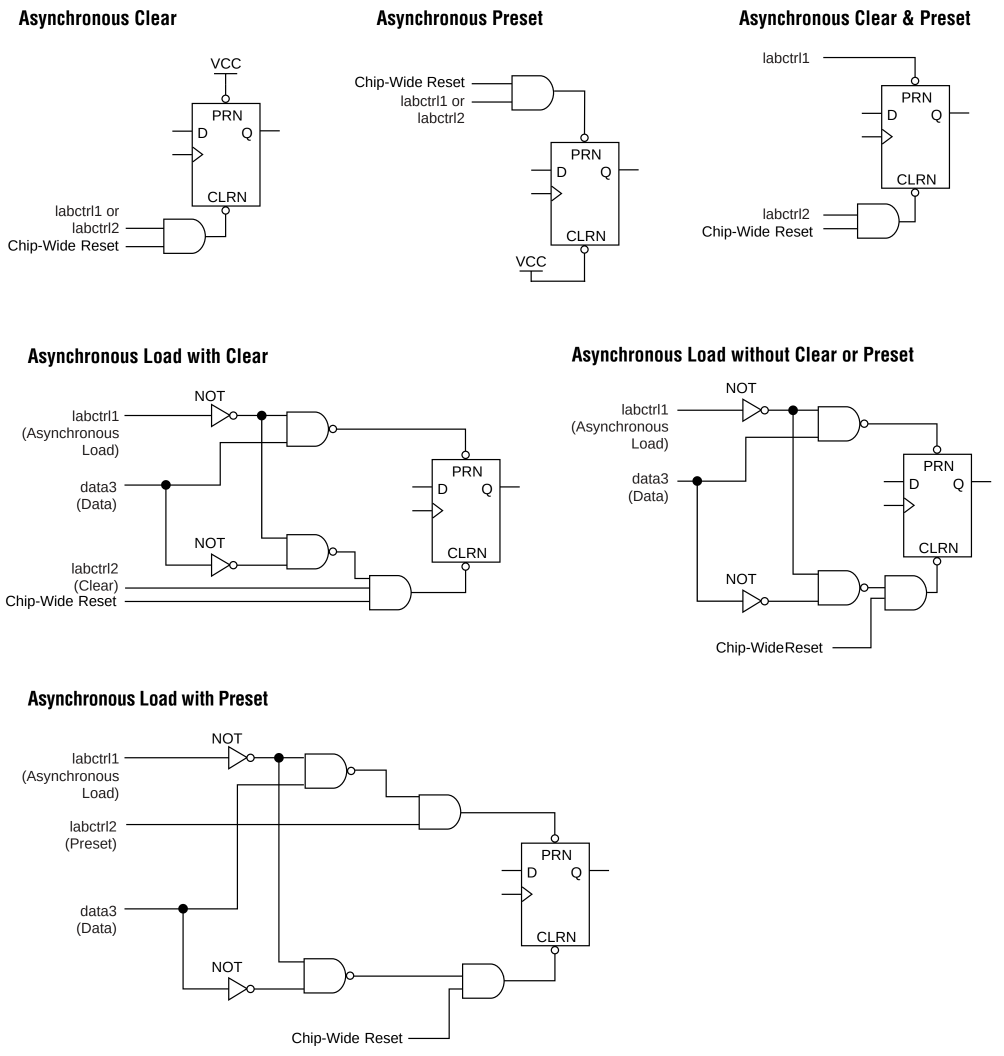
During compilation, the Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six modes chosen during design entry:

- Asynchronous clear
- Asynchronous preset
- Asynchronous clear and preset
- Asynchronous load with clear
- Asynchronous load with preset
- Asynchronous load without clear or preset

In addition to the six clear and preset modes, FLEX 10K devices provide a chip-wide reset pin that can reset all registers in the device. Use of this feature is set during design entry. In any of the clear and preset modes, the chip-wide reset overrides all other signals. Registers with asynchronous presets may be preset when the chip-wide reset is asserted. Inversion can be used to implement the asynchronous preset. Figure 10 shows examples of how to enter a section of a design for the desired functionality.

Figure 10. LE Clear & Preset Modes



Asynchronous Clear

The flipflop can be cleared by either `LABCTRL1` or `LABCTRL2`. In this mode, the preset signal is tied to V_{CC} to deactivate it.

FastTrack Interconnect

In the FLEX 10K architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, which is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect. The row interconnect can drive I/O pins and feed other LABs in the device. The column interconnect routes signals between rows and can drive I/O pins.

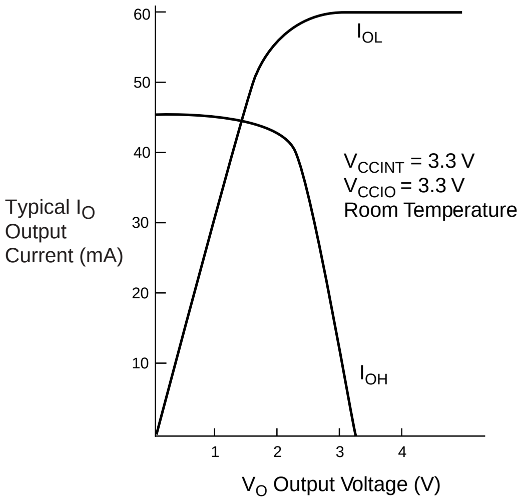
A row channel can be driven by an LE or by one of three column channels. These four signals feed dual 4-to-1 multiplexers that connect to two specific row channels. These multiplexers, which are connected to each LE, allow column channels to drive row channels even when all eight LEs in an LAB drive the row interconnect.

Each column of LABs is served by a dedicated column interconnect. The column interconnect can then drive I/O pins or another row's interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must be routed to the row interconnect before it can enter an LAB or EAB. Each row channel that is driven by an IOE or EAB can drive one specific column channel.

Access to row and column channels can be switched between LEs in adjacent pairs of LABs. For example, an LE in one LAB can drive the row and column channels normally driven by a particular LE in the adjacent LAB in the same row, and vice versa. This routing flexibility enables routing resources to be used more efficiently. See Figure 11.

Figure 22 shows the typical output drive characteristics of EPF10K10A, EPF10K30A, EPF10K100A, and EPF10K250A devices with 3.3-V and 2.5-V V_{CCIO}. The output driver is compliant with the 3.3-V ***PCI Local Bus Specification, Revision 2.2*** (with 3.3-V V_{CCIO}). Moreover, device analysis shows that the EPF10K10A, EPF10K30A, and EPF 10K100A devices can drive a 5.0-V PCI bus with eight or fewer loads.

Figure 22. Output Drive Characteristics for EPF10K10A, EPF10K30A & EPF10K100A Devices



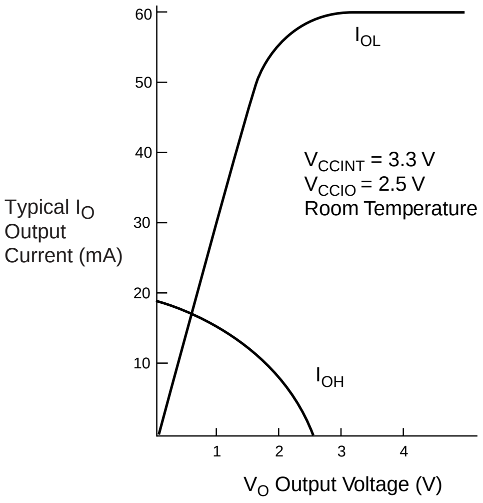


Figure 23 shows the typical output drive characteristics of the EPF10K250A device with 3.3-V and 2.5-V V_{CCIO}.

Table 36. Interconnect Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
$t_{DIN2IOE}$	Delay from dedicated input pin to IOE control input	(7)
$t_{DCLK2LE}$	Delay from dedicated clock pin to LE or EAB clock	(7)
$t_{DIN2DATA}$	Delay from dedicated input or clock to LE or EAB data	(7)
$t_{DCLK2IOE}$	Delay from dedicated clock pin to IOE clock	(7)
t_{DIN2LE}	Delay from dedicated input pin to LE or EAB control input	(7)
$t_{SAMELAB}$	Routing delay for an LE driving another LE in the same LAB	
$t_{SAMEROW}$	Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row	(7)
$t_{SAMECOLUMN}$	Routing delay for an LE driving an IOE in the same column	(7)
$t_{DIFFROW}$	Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row	(7)
$t_{TWOROWS}$	Routing delay for a row IOE or EAB driving an LE or EAB in a different row	(7)
$t_{LEPERIPH}$	Routing delay for an LE driving a control signal of an IOE via the peripheral control bus	(7)
$t_{LABCARRY}$	Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	

Table 37. External Timing Parameters *Notes (8), (10)*

Symbol	Parameter	Conditions
t_{DRR}	Register-to-register delay via four LEs, three row interconnects, and four local interconnects	(9)
t_{INSU}	Setup time with global clock at IOE register	
t_{INH}	Hold time with global clock at IOE register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE register	

Table 38. External Bidirectional Timing Parameters *Note (10)*

Symbol	Parameter	Condition
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at adjacent LE register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at adjacent LE register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	
$t_{XZBIDIR}$	Synchronous IOE output buffer disable delay	
$t_{ZXBIDIR}$	Synchronous IOE output buffer enable delay, slow slew rate = off	

Table 41. EPF10K10 & EPF10K20 Device EAB Internal Microparameters Note (1)					
Symbol	**-3 Speed Grade**		**-4 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	
$t_{EABDATA1}$		1.5		1.9	ns
$t_{EABDATA2}$		4.8		6.0	ns
t_{EABWE1}		1.0		1.2	ns
t_{EABWE2}		5.0		6.2	ns
t_{EABCLK}		1.0		2.2	ns
t_{EABCO}		0.5		0.6	ns
$t_{EABBYPASS}$		1.5		1.9	ns
t_{EABSU}	1.5		1.8		ns
t_{EABH}	2.0		2.5		ns
t_{AA}		8.7		10.7	ns
t_{WP}	5.8		7.2		ns
t_{WDSU}	1.6		2.0		ns
t_{WDH}	0.3		0.4		ns
t_{WASU}	0.5		0.6		ns
t_{WAH}	1.0		1.2		ns
t_{WO}		5.0		6.2	ns
t_{DD}		5.0		6.2	ns
t_{EABOUT}		0.5		0.6	ns
t_{EABCH}	4.0		4.0		ns
t_{EABCL}	5.8		7.2		ns

Table 45. EPF10K10 & EPF10K20 Device External Timing Parameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
t_{DRR}		16.1		20.0	ns
t_{INSU} (2), (3)	5.5		6.0		ns
t_{INH} (3)	0.0		0.0		ns
t_{OUTCO} (3)	2.0	6.7	2.0	8.4	ns

Table 46. EPF10K10 Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{INSUBIDIR}$	4.5		5.6		ns
$t_{INHBIDIR}$	0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	6.7	2.0	8.4	ns
$t_{XZBIDIR}$		10.5		13.4	ns
$t_{ZXBIDIR}$		10.5		13.4	ns

Table 47. EPF10K20 Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	
$t_{INSUBIDIR}$	4.6		5.7		ns
$t_{INHBIDIR}$	0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	6.7	2.0	8.4	ns
$t_{XZBIDIR}$		10.5		13.4	ns
$t_{ZXBIDIR}$		10.5		13.4	ns

Notes to tables:
(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.

Table 73. EPF10K50V Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.7		2.8		3.4		4.6	ns
$t_{EABDATA2}$		4.9		3.9		4.8		5.9	ns
t_{EABWE1}		0.0		2.5		3.0		3.7	ns
t_{EABWE2}		4.0		4.1		5.0		6.2	ns
t_{EABCLK}		0.4		0.8		1.0		1.2	ns
t_{EABCO}		0.1		0.2		0.3		0.4	ns
$t_{EABBYPASS}$		0.9		1.1		1.3		1.6	ns
t_{EABSU}	0.8		1.5		1.8		2.2		ns
t_{EABH}	0.8		1.6		2.0		2.5		ns
t_{AA}		5.5		8.2		10.0		12.4	ns
t_{WP}	6.0		4.9		6.0		7.4		ns
t_{WDSU}	0.1		0.8		1.0		1.2		ns
t_{WDH}	0.1		0.2		0.3		0.4		ns
t_{WASU}	0.1		0.4		0.5		0.6		ns
t_{WAH}	0.1		0.8		1.0		1.2		ns
t_{WO}		2.8		4.3		5.3		6.5	ns
t_{DD}		2.8		4.3		5.3		6.5	ns
t_{EABOUT}		0.5		0.4		0.5		0.6	ns
t_{EABCH}	2.0		4.0		4.0		4.0		ns
t_{EABCL}	6.0		4.9		6.0		7.4		ns

Table 93. EPF10K30A Device IOE Timing Microparameters Note (1) **(Part 2 of 2)**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{IOH}	0.9		1.1		1.4		ns
t_{IOCLR}		0.7		0.8		1.0	ns
t_{OD1}		1.9		2.2		2.9	ns
t_{OD2}		4.8		5.6		7.3	ns
t_{OD3}		7.0		8.2		10.8	ns
t_{XZ}		2.2		2.6		3.4	ns
t_{ZX1}		2.2		2.6		3.4	ns
t_{ZX2}		5.1		6.0		7.8	ns
t_{ZX3}		7.3		8.6		11.3	ns
t_{INREG}		4.4		5.2		6.8	ns
t_{IOFD}		3.8		4.5		5.9	ns
t_{INCOMB}		3.8		4.5		5.9	ns

Table 96. EPF10K30A Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		3.9		4.4		5.1	ns
t_{DIN2LE}		1.2		1.5		1.9	ns
$t_{DIN2DATA}$		3.2		3.6		4.5	ns
$t_{DCLK2IOE}$		3.0		3.5		4.6	ns
$t_{DCLK2LE}$		1.2		1.5		1.9	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		2.3		2.4		2.7	ns
$t_{SAMECOLUMN}$		1.3		1.4		1.9	ns
$t_{DIFFROW}$		3.6		3.8		4.6	ns
$t_{TWOROWS}$		5.9		6.2		7.3	ns
$t_{LEPERIPH}$		3.5		3.8		4.1	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.9		1.1		1.4	ns

Table 97. EPF10K30A External Reference Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		11.0		13.0		17.0	ns
t_{INSU} *(2)*, *(3)*	2.5		3.1		3.9		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	5.4	2.0	6.2	2.0	8.3	ns

Table 98. EPF10K30A Device External Bidirectional Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	4.2		4.9		6.8		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	5.4	2.0	6.2	2.0	8.3	ns
$t_{XZBIDIR}$		6.2		7.5		9.8	ns
$t_{ZXBIDIR}$		6.2		7.5		9.8	ns

Table 102. EPF10K100A Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		6.8		7.8		9.2	ns
$t_{EABRCCOMB}$	6.8		7.8		9.2		ns
$t_{EABRCREG}$	5.4		6.2		7.4		ns
t_{EABWP}	3.2		3.7		4.4		ns
$t_{EABWCCOMB}$	3.4		3.9		4.7		ns
$t_{EABWCREG}$	9.4		10.8		12.8		ns
t_{EABDD}		6.1		6.9		8.2	ns
$t_{EABDATACO}$		2.1		2.3		2.9	ns
$t_{EABDATASU}$	3.7		4.3		5.1		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	2.8		3.3		3.8		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	3.4		4.0		4.6		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	1.9		2.3		2.6		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		5.1		5.7		6.9	ns

SRAM configuration elements allow FLEX 10K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation.

The entire reconfiguration process may be completed in less than 320 ms using an EPF10K250A device with a `DCLK` frequency of 10 MHz. This process can be used to reconfigure an entire system dynamically. In-field upgrades can be performed by distributing new configuration files.

☞ Refer to the configuration device data sheet to obtain the POR delay when using a configuration device method.

Programming Files

Despite being function- and pin-compatible, FLEX 10KA and FLEX 10KE devices are not programming- or configuration-file compatible with FLEX 10K devices. A design should be recompiled before it is transferred from a FLEX 10K device to an equivalent FLEX 10KA or FLEX 10KE device. This recompilation should be performed to create a new programming or configuration file and to check design timing on the faster FLEX 10KA or FLEX 10KE device. The programming or configuration files for EPF10K50 devices can program or configure an EPF10K50V device. However, Altera recommends recompiling a design for the EPF10K50V device when transferring it from the EPF10K50 device.

Configuration Schemes

The configuration data for a FLEX 10K device can be loaded with one of five configuration schemes (see Table 116), chosen on the basis of the target application. An EPC1, EPC2, EPC16, or EPC1441 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of a FLEX 10K device, allowing automatic configuration on system power-up.