# Intel - EPF10K70RC240-2N Datasheet


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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

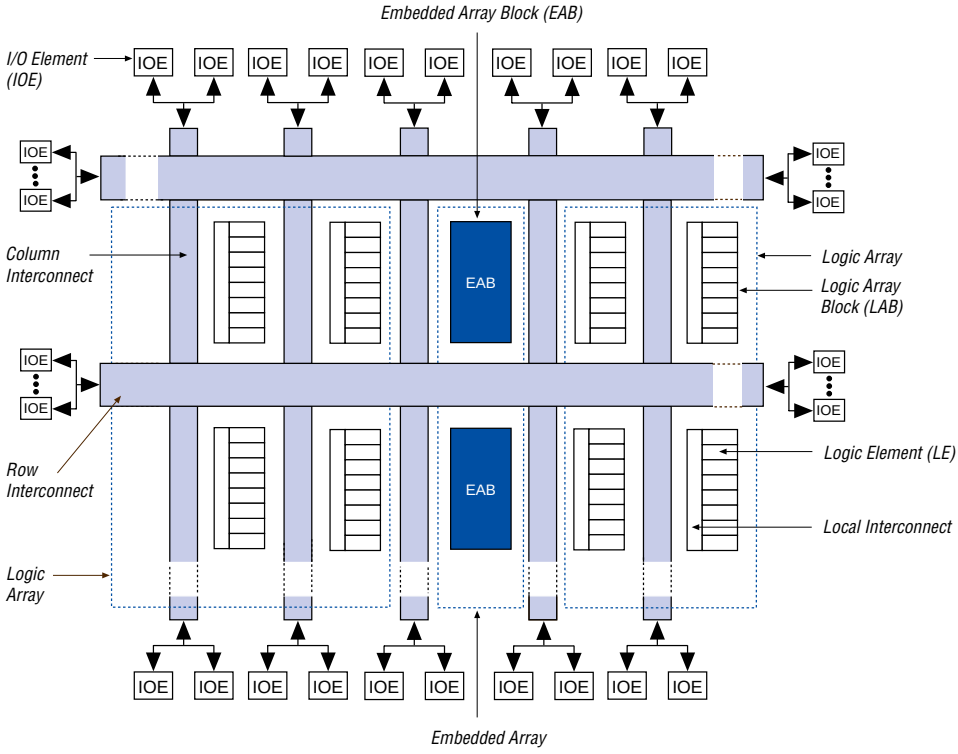
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 468 |
| Number of Logic Elements/Cells | 3744 |
| Total RAM Bits | 18432 |
| Number of I/O | 189 |
| Number of Gates | 118000 |
| Voltage - Supply | 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 240-BFQFP Exposed Pad |
| Supplier Device Package | 240-RQFP (32x32) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epf10k70rc240-2n |

*Figure 1. FLEX 10K Device Block Diagram*

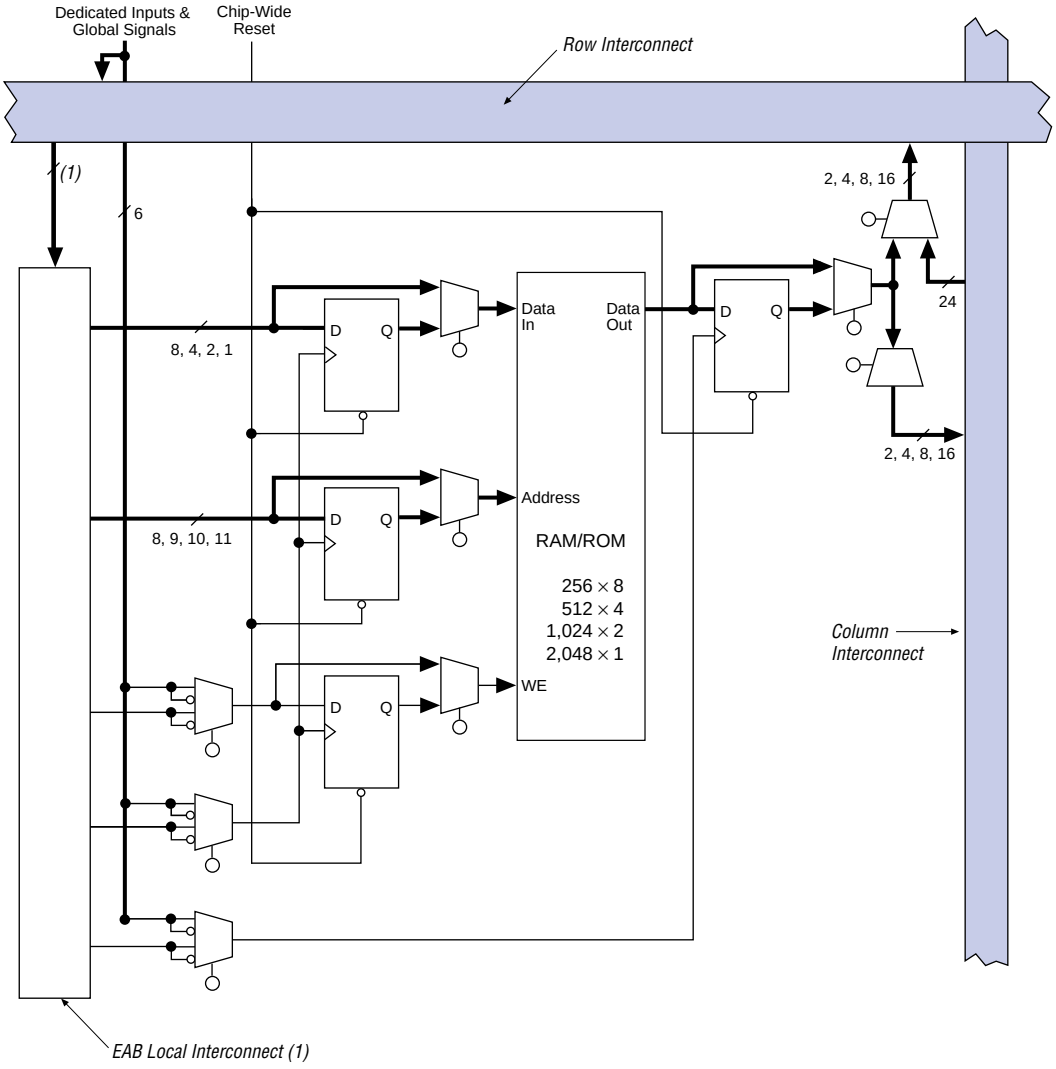



FLEX 10K devices provide six dedicated inputs that drive the flipflops' control inputs to ensure the efficient distribution of high-speed, low-skew (less than 1.5 ns) control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

## Embedded Array Block

The EAB is a flexible block of RAM with registers on the input and output ports, and is used to implement common gate array megafunctions. The EAB is also suitable for functions such as multipliers, vector scalars, and error correction circuits, because it is large and flexible. These functions can be combined in applications such as digital filters and microcontrollers.

*Figure 4. FLEX 10K Embedded Array Block*




*Note:*

(1) EPF10K10, EPF10K10A, EPF10K20, EPF10K30, EPF10K30A, EPF10K40, EPF10K50, and EPF10K50V devices have 22 EAB local interconnect channels; EPF10K70, EPF10K100, EPF10K100A, EPF10K130V, and EPF10K250A devices have 26.

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks; the other two can be used for clear/preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I/O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I/O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

## Logic Element

The LE, the smallest unit of logic in the FLEX 10K architecture, has a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect. See Figure 6.

*Figure 6. FLEX 10K Logic Element*

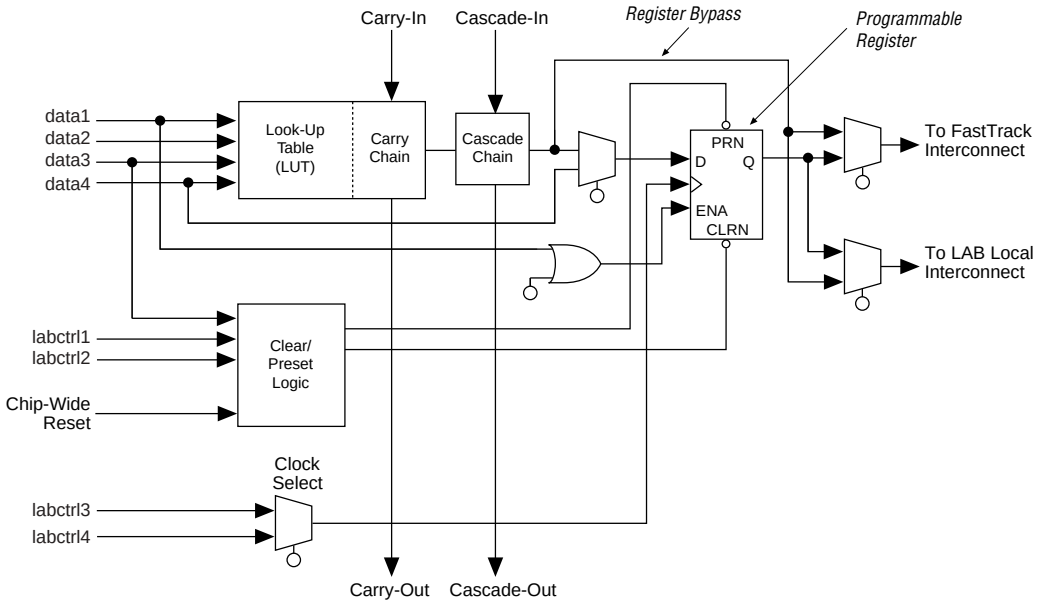
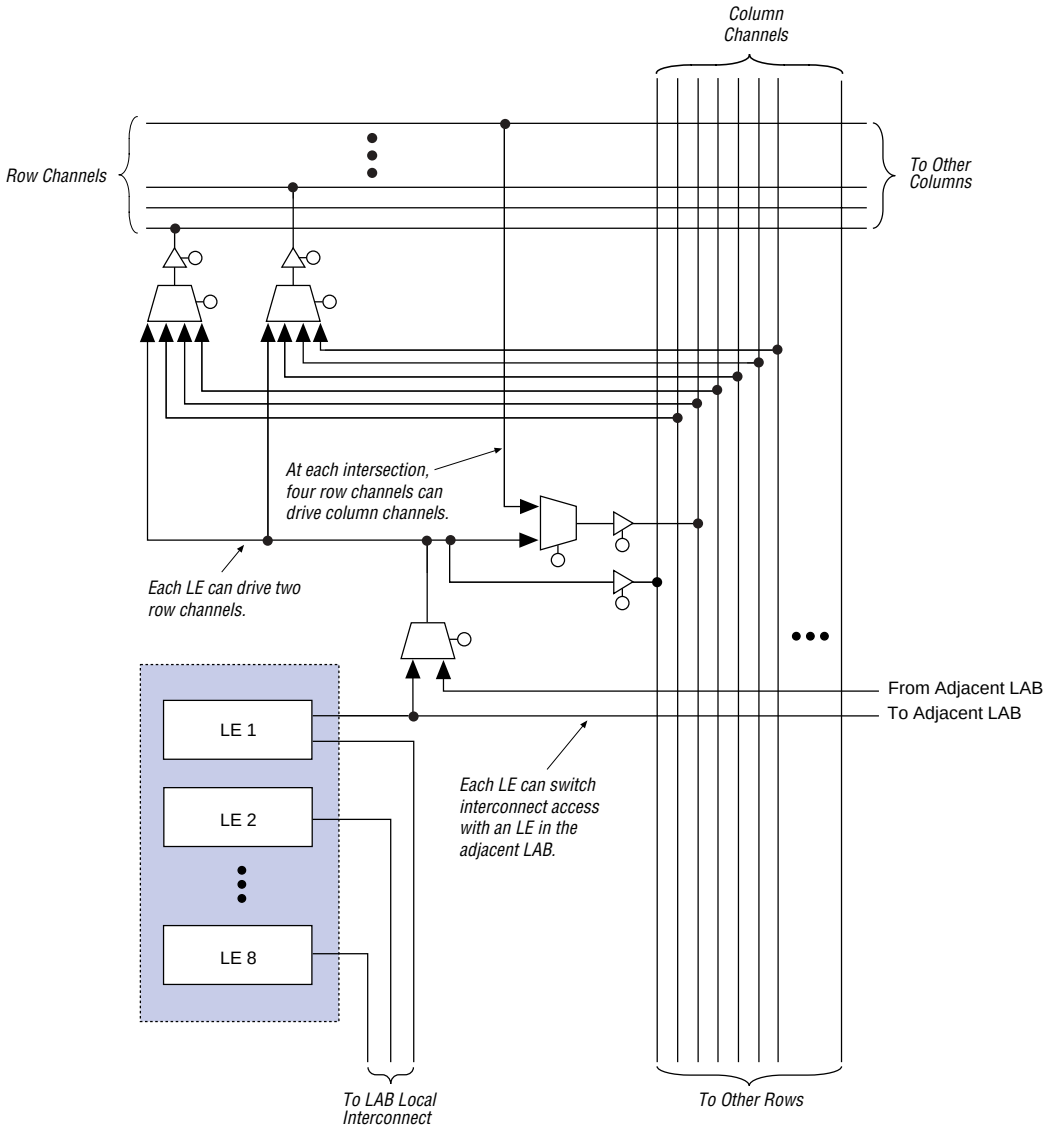


*Figure 11. LAB Connections to Row & Column Interconnect*



## ClockLock & ClockBoost Features

To support high-speed designs, selected FLEX 10K devices offer optional ClockLock and ClockBoost circuitry containing a phase-locked loop (PLL) that is used to increase design speed and reduce resource usage. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost feature allows the designer to distribute a low-speed clock and multiply that clock on-device. Combined, the ClockLock and ClockBoost features provide significant improvements in system performance and bandwidth.

The ClockLock and ClockBoost features in FLEX 10K devices are enabled through the Altera software. External devices are not required to use these features. The output of the ClockLock and ClockBoost circuits is not available at any of the device pins.

The ClockLock and ClockBoost circuitry locks onto the rising edge of the incoming clock. The circuit output can only drive the clock inputs of registers; the generated clock cannot be gated or inverted.

The dedicated clock pin (`GCLK1`) supplies the clock to the ClockLock and ClockBoost circuitry. When the dedicated clock pin is driving the ClockLock or ClockBoost circuitry, it cannot drive elsewhere in the device.

In designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to `GCLK1`. With the Altera software, `GCLK1` can feed both the ClockLock and ClockBoost circuitry in the FLEX 10K device. However, when both circuits are used, the other clock pin (`GCLK0`) cannot be used. Figure 17 shows a block diagram of how to enable both the ClockLock and ClockBoost circuits in the Altera software. The example shown is a schematic, but a similar approach applies for designs created in AHDL, VHDL, and Verilog HDL. When the ClockLock and ClockBoost circuits are used simultaneously, the input frequency parameter must be the same for both circuits. In Figure 17, the input frequency must meet the requirements specified when the ClockBoost multiplication factor is two.

## Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces system noise and adds a maximum delay of approximately 2.9 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a device-wide basis. The slow slew rate setting affects only the falling edge of the output.

## Open-Drain Output Option

FLEX 10K devices provide an optional open-drain (electrically equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane. Additionally, the Altera software can convert tri-state buffers with grounded data inputs to open-drain pins automatically.

Open-drain output pins on FLEX 10K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a $V_{IH}$ of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The $I_{OL}$ current specification should be considered when selecting a pull-up resistor.

Output pins on 5.0-V FLEX 10K devices with $V_{CCIO}$ = 3.3 V or 5.0 V (with a pull-up resistor to the 5.0-V supply) can also drive 5.0-V CMOS input pins. In this case, the pull-up transistor will turn off when the pin voltage exceeds 3.3 V. Therefore, the pin does not have to be open-drain.

## MultiVolt I/O Interface

The FLEX 10K device architecture supports the MultiVolt I/O interface feature, which allows FLEX 10K devices to interface with systems of differing supply voltages. These devices have one set of $V_{CC}$ pins for internal operation and input buffers (VCCINT) and another set for I/O output drivers (VCCIO).

Table 12 describes the FLEX 10K device supply voltages and MultiVolt I/O support levels.

*Table 12. Supply Voltages & MultiVolt I/O Support Levels*

| Devices | Supply Voltage (V) | | MultiVolt I/O Support Levels (V) | |
|---|---|---|---|---|
| | $V_{CCINT}$ | $V_{CCIO}$ | Input | Output |
| FLEX 10K *(1)* | 5.0 | 5.0 | 3.3 or 5.0 | 5.0 |
| | 5.0 | 3.3 | 3.3 or 5.0 | 3.3 or 5.0 |
| EPF10K50V *(1)* | 3.3 | 3.3 | 3.3 or 5.0 | 3.3 or 5.0 |
| EPF10K130V | 3.3 | 3.3 | 3.3 or 5.0 | 3.3 or 5.0 |
| FLEX 10KA *(1)* | 3.3 | 3.3 | 2.5, 3.3, or 5.0 | 3.3 or 5.0 |
| | 3.3 | 2.5 | 2.5, 3.3, or 5.0 | 2.5 |

*Note*
(1) 240-pin QFP packages do not support the MultiVolt I/O features, so they do not have separate $V_{CCIO}$ pins.

### Power Sequencing & Hot-Socketing

Because FLEX 10K devices can be used in a multi-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The $V_{CCIO}$ and $V_{CCINT}$ power supplies can be powered in any order.

Signals can be driven into FLEX 10KA devices before and during power up without damaging the device. Additionally, FLEX 10KA devices do not drive out during power up. Once operating conditions are reached, FLEX 10KA devices operate as specified by the user.

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All FLEX 10K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. All FLEX 10K devices can also be configured using the JTAG pins through the BitBlaster serial download cable, or ByteBlasterMV parallel port download cable, or via hardware that uses the Jam™ programming and test language. JTAG BST can be performed before or after configuration, but not during configuration. FLEX 10K devices support the JTAG instructions shown in Table 13.

Tables 22 through 25 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for EPF10K50V and EPF10K130V devices.

*Table 22. EPF10K50V & EPF10K130V Device Absolute Maximum Ratings* *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to ground *(2)* | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –2.0 | 5.75 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | Ceramic packages, under bias | | 150 | ° C |
| | | RQFP and BGA packages, under bias | | 135 | ° C |

*Table 23. EPF10K50V & EPF10K130V Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| $V_{CCIO}$ | Supply voltage for output buffers | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| $V_I$ | Input voltage | *(5)* | -0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | For commercial use | 0 | 70 | ° C |
| | | For industrial use | –40 | 85 | ° C |
| $T_J$ | Operating temperature | For commercial use | 0 | 85 | ° C |
| | | For industrial use | –40 | 100 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

Figure 22 shows the typical output drive characteristics of EPF10K10A, EPF10K30A, EPF10K100A, and EPF10K250A devices with 3.3-V and 2.5-V $V_{CCIO}$. The output driver is compliant with the 3.3-V ***PCI Local Bus Specification, Revision 2.2*** (with 3.3-V $V_{CCIO}$). Moreover, device analysis shows that the EPF10K10A, EPF10K30A, and EPF 10K100A devices can drive a 5.0-V PCI bus with eight or fewer loads.

***Figure 22. Output Drive Characteristics for EPF10K10A, EPF10K30A & EPF10K100A Devices***

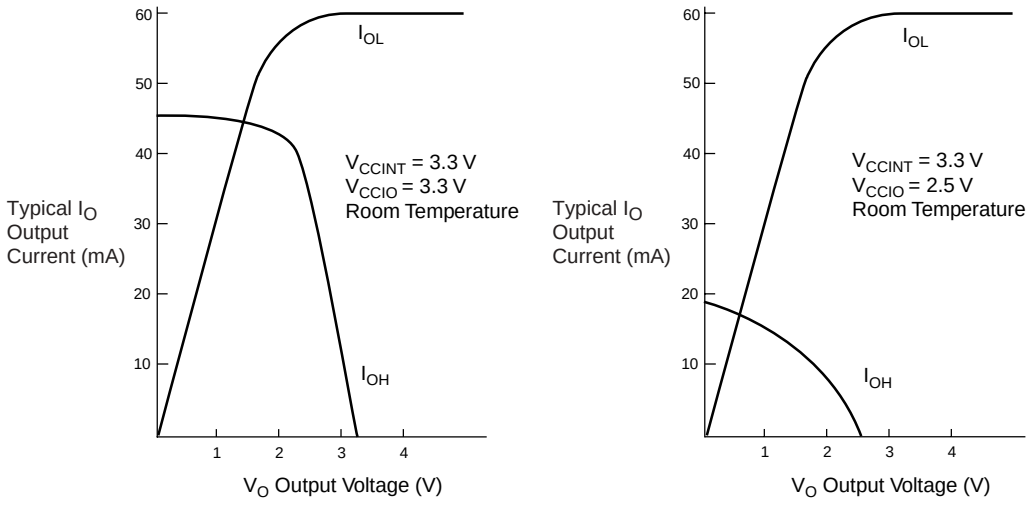



Figure 23 shows the typical output drive characteristics of the EPF10K250A device with 3.3-V and 2.5-V $V_{CCIO}$.

Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Figure 24 shows the overall timing model, which maps the possible paths to and from the various elements of the FLEX 10K device.

*Figure 24. FLEX 10K Device Timing Model*

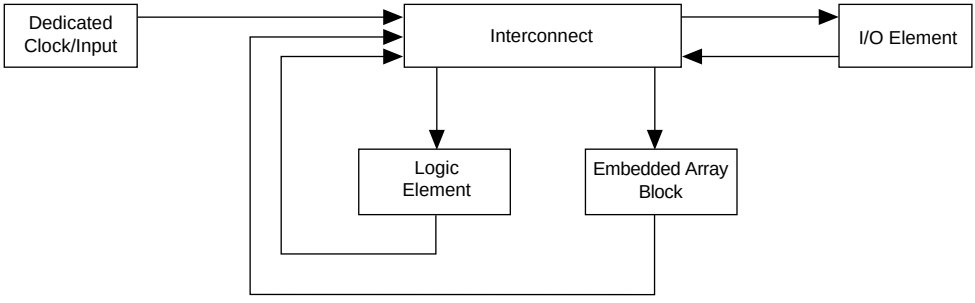
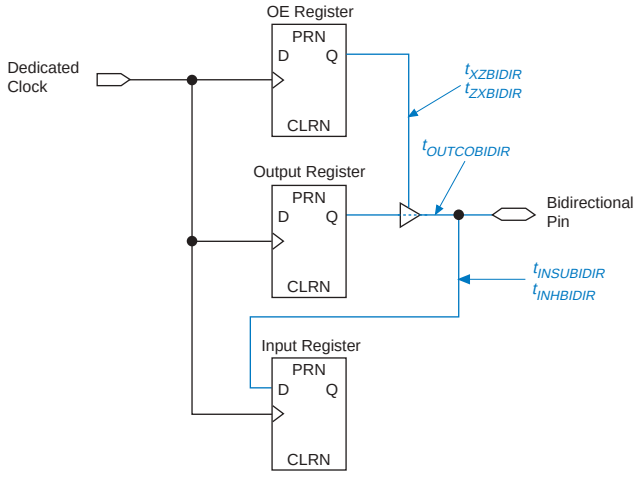


*Figure 28. Synchronous Bidirectional Pin External Timing Model*




Tables 32 through 36 describe the FLEX 10K device internal timing parameters. These internal timing parameters are expressed as worst-case values. Using hand calculations, these parameters can be used to estimate design performance. However, before committing designs to silicon, actual worst-case performance should be modeled using timing simulation and analysis. Tables 37 through 38 describe FLEX 10K external timing parameters.

*Table 32. LE Timing Microparameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{LUT}$ | LUT delay for data-in | |
| $t_{CLUT}$ | LUT delay for carry-in | |
| $t_{RLUT}$ | LUT delay for LE register feedback | |
| $t_{PACKED}$ | Data-in to packed register delay | |
| $t_{EN}$ | LE register enable delay | |
| $t_{CICO}$ | Carry-in to carry-out delay | |
| $t_{CGEN}$ | Data-in to carry-out delay | |
| $t_{CGENR}$ | LE register feedback to carry-out delay | |
| $t_{CASC}$ | Cascade-in to cascade-out delay | |
| $t_{C}$ | LE register control signal delay | |
| $t_{CO}$ | LE register clock-to-output delay | |
| $t_{COMB}$ | Combinatorial delay | |

*Table 68. EPF10K100 Device Interconnect Timing Microparameters* *Note (1)*

| Symbol | -3DX Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 10.3 | | 10.3 | | 12.2 | ns |
| $t_{DIN2LE}$ | | 4.8 | | 4.8 | | 6.0 | ns |
| $t_{DIN2DATA}$ | | 7.3 | | 7.3 | | 11.0 | ns |
| $t_{DCLK2IOE}$ without ClockLock or ClockBoost circuitry | | 6.2 | | 6.2 | | 7.7 | ns |
| $t_{DCLK2IOE}$ with ClockLock or ClockBoost circuitry | | 2.3 | | – | | – | ns |
| $t_{DCLK2LE}$ without ClockLock or ClockBoost circuitry | | 4.8 | | 4.8 | | 6.0 | ns |
| $t_{DCLK2LE}$ with ClockLock or ClockBoost circuitry | | 2.3 | | – | | – | ns |
| $t_{SAMELAB}$ | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{SAMEROW}$ | | 4.9 | | 4.9 | | 5.5 | ns |
| $t_{SAMECOLUMN}$ | | 5.1 | | 5.1 | | 5.4 | ns |
| $t_{DIFFROW}$ | | 10.0 | | 10.0 | | 10.9 | ns |
| $t_{TWOROWS}$ | | 14.9 | | 14.9 | | 16.4 | ns |
| $t_{LEPERIPH}$ | | 6.9 | | 6.9 | | 8.1 | ns |
| $t_{LABCARRY}$ | | 0.9 | | 0.9 | | 1.1 | ns |
| $t_{LABCASC}$ | | 3.0 | | 3.0 | | 3.2 | ns |

**Table 69. EPF10K100 Device External Timing Parameters** *Note (1)*

| Symbol | -3DX Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 19.1 | | 19.1 | | 24.2 | ns |
| $t_{INSU}$ *(2)*, *(3)*, *(4)* | 7.8 | | 7.8 | | 8.5 | | ns |
| $t_{OUTCO}$ *(3)*, *(4)* | 2.0 | 11.1 | 2.0 | 11.1 | 2.0 | 14.3 | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ *(2)*, *(3)*, *(5)* | 6.2 | | – | | – | | ns |
| $t_{OUTCO}$ *(3)*, *(5)* | 2.0 | 6.7 | | – | | – | ns |

**Table 70. EPF10K100 Device External Bidirectional Timing Parameters** *Note (1)*

| Symbol | -3DX Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ *(4)* | 8.1 | | 8.1 | | 10.4 | | ns |
| $t_{INHBIDIR}$ *(4)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ *(4)* | 2.0 | 11.1 | 2.0 | 11.1 | 2.0 | 14.3 | ns |
| $t_{XZBIDIR}$ *(4)* | | 15.3 | | 15.3 | | 18.4 | ns |
| $t_{ZXBIDIR}$ *(4)* | | 15.3 | | 15.3 | | 18.4 | ns |
| $t_{INSUBIDIR}$ *(5)* | 9.1 | | – | | – | | ns |
| $t_{INHBIDIR}$ *(5)* | 0.0 | | – | | – | | ns |
| $t_{OUTCOBIDIR}$ *(5)* | 2.0 | 7.2 | – | – | – | – | ns |
| $t_{XZBIDIR}$ *(5)* | | 14.3 | | – | | – | ns |
| $t_{ZXBIDIR}$ *(5)* | | 14.3 | | – | | – | ns |

*Notes to tables:*

(1) All timing parameters are described in Tables 32 through 38 in this data sheet.
(2) Using an LE to register the signal may provide a lower setup time.
(3) This parameter is specified by characterization.
(4) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(5) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

*Table 80. EPF10K130V Device EAB Internal Microparameters* *Note (1)*

| Symbol | -2 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.9 | | 2.4 | | 2.4 | ns |
| $t_{EABDATA2}$ | | 3.7 | | 4.7 | | 4.7 | ns |
| $t_{EABWE1}$ | | 1.9 | | 2.4 | | 2.4 | ns |
| $t_{EABWE2}$ | | 3.7 | | 4.7 | | 4.7 | ns |
| $t_{EABCLK}$ | | 0.7 | | 0.9 | | 0.9 | ns |
| $t_{EABCO}$ | | 0.5 | | 0.6 | | 0.6 | ns |
| $t_{EABBYPASS}$ | | 0.6 | | 0.8 | | 0.8 | ns |
| $t_{EABSU}$ | 1.4 | | 1.8 | | 1.8 | | ns |
| $t_{EABH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{AA}$ | | 5.6 | | 7.1 | | 7.1 | ns |
| $t_{WP}$ | 3.7 | | 4.7 | | 4.7 | | ns |
| $t_{WDSU}$ | 4.6 | | 5.9 | | 5.9 | | ns |
| $t_{WDH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASU}$ | 3.9 | | 5.0 | | 5.0 | | ns |
| $t_{WAH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WO}$ | | 5.6 | | 7.1 | | 7.1 | ns |
| $t_{DD}$ | | 5.6 | | 7.1 | | 7.1 | ns |
| $t_{EABOUT}$ | | 2.4 | | 3.1 | | 3.1 | ns |
| $t_{EABCH}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{EABCL}$ | 4.0 | | 4.7 | | 4.7 | | ns |

*Table 87. EPF10K10A Device EAB Internal Microparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 3.3 | | 3.9 | | 5.2 | ns |
| $t_{EABDATA2}$ | | 1.0 | | 1.3 | | 1.7 | ns |
| $t_{EABWE1}$ | | 2.6 | | 3.1 | | 4.1 | ns |
| $t_{EABWE2}$ | | 2.7 | | 3.2 | | 4.3 | ns |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCO}$ | | 1.2 | | 1.4 | | 1.8 | ns |
| $t_{EABBYPASS}$ | | 0.1 | | 0.2 | | 0.2 | ns |
| $t_{EABSU}$ | 1.4 | | 1.7 | | 2.2 | | ns |
| $t_{EABH}$ | 0.1 | | 0.1 | | 0.1 | | ns |
| $t_{AA}$ | | 4.5 | | 5.4 | | 7.3 | ns |
| $t_{WP}$ | 2.0 | | 2.4 | | 3.2 | | ns |
| $t_{WDSU}$ | 0.7 | | 0.8 | | 1.1 | | ns |
| $t_{WDH}$ | 0.5 | | 0.6 | | 0.7 | | ns |
| $t_{WASU}$ | 0.6 | | 0.7 | | 0.9 | | ns |
| $t_{WAH}$ | 0.9 | | 1.1 | | 1.5 | | ns |
| $t_{WO}$ | | 3.3 | | 3.9 | | 5.2 | ns |
| $t_{DD}$ | | 3.3 | | 3.9 | | 5.2 | ns |
| $t_{EABOUT}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{EABCH}$ | 3.0 | | 3.5 | | 4.0 | | ns |
| $t_{EABCL}$ | 3.03 | | 3.5 | | 4.0 | | ns |

*Table 88. EPF10K10A Device EAB Internal Timing Macroparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABAA}$ | | 8.1 | | 9.8 | | 13.1 | ns |
| $t_{EABRCCOMB}$ | 8.1 | | 9.8 | | 13.1 | | ns |
| $t_{EABRCREG}$ | 5.8 | | 6.9 | | 9.3 | | ns |
| $t_{EABWP}$ | 2.0 | | 2.4 | | 3.2 | | ns |
| $t_{EABWCCOMB}$ | 3.5 | | 4.2 | | 5.6 | | ns |
| $t_{EABWCREG}$ | 9.4 | | 11.2 | | 14.8 | | ns |
| $t_{EABDD}$ | | 6.9 | | 8.3 | | 11.0 | ns |
| $t_{EABDATACO}$ | | 1.3 | | 1.5 | | 2.0 | ns |
| $t_{EABDATASU}$ | 2.4 | | 3.0 | | 3.9 | | ns |
| $t_{EABDATAH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWESU}$ | 4.1 | | 4.9 | | 6.5 | | ns |
| $t_{EABWEH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWDSU}$ | 1.4 | | 1.6 | | 2.2 | | ns |
| $t_{EABWDH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWASU}$ | 2.5 | | 3.0 | | 4.1 | | ns |
| $t_{EABWAH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWO}$ | | 6.2 | | 7.5 | | 9.9 | ns |

**Table 89. EPF10K10A Device Interconnect Timing Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 4.2 | | 5.0 | | 6.5 | ns |
| $t_{DIN2LE}$ | | 2.2 | | 2.6 | | 3.4 | ns |
| $t_{DIN2DATA}$ | | 4.3 | | 5.2 | | 7.1 | ns |
| $t_{DCLK2IOE}$ | | 4.2 | | 4.9 | | 6.6 | ns |
| $t_{DCLK2LE}$ | | 2.2 | | 2.6 | | 3.4 | ns |
| $t_{SAMELAB}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{SAMEROW}$ | | 2.2 | | 2.4 | | 2.9 | ns |
| $t_{SAMECOLUMN}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{DIFFROW}$ | | 3.0 | | 3.4 | | 4.3 | ns |
| $t_{TWOROWS}$ | | 5.2 | | 5.8 | | 7.2 | ns |
| $t_{LEPERIPH}$ | | 1.8 | | 2.2 | | 2.8 | ns |
| $t_{LABCARRY}$ | | 0.5 | | 0.5 | | 0.7 | ns |
| $t_{LABCASC}$ | | 0.9 | | 1.0 | | 1.5 | ns |

**Table 90. EPF10K10A External Reference Timing Parameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 10.0 | | 12.0 | | 16.0 | ns |
| $t_{INSU}$ *(2)*, *(3)* | 1.6 | | 2.1 | | 2.8 | | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(3)* | 2.0 | 5.8 | 2.0 | 6.9 | 2.0 | 9.2 | ns |

**Table 91. EPF10K10A Device External Bidirectional Timing Parameters** *Note (1)*

| Symbol | -2 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.4 | | 3.3 | | 4.5 | | ns |
| $t_{INHBIDIR}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ | 2.0 | 5.8 | 2.0 | 6.9 | 2.0 | 9.2 | ns |
| $t_{XZBIDIR}$ | | 6.3 | | 7.5 | | 9.9 | ns |
| $t_{ZXBIDIR}$ | | 6.3 | | 7.5 | | 9.9 | ns |

*Table 101. EPF10K100A Device EAB Internal Microparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.8 | | 2.1 | | 2.4 | ns |
| $t_{EABDATA2}$ | | 3.2 | | 3.7 | | 4.4 | ns |
| $t_{EABWE1}$ | | 0.8 | | 0.9 | | 1.1 | ns |
| $t_{EABWE2}$ | | 2.3 | | 2.7 | | 3.1 | ns |
| $t_{EABCLK}$ | | 0.8 | | 0.9 | | 1.1 | ns |
| $t_{EABCO}$ | | 1.0 | | 1.1 | | 1.4 | ns |
| $t_{EABBYPASS}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{EABSU}$ | 1.3 | | 1.5 | | 1.8 | | ns |
| $t_{EABH}$ | 0.4 | | 0.5 | | 0.5 | | ns |
| $t_{AA}$ | | 4.1 | | 4.8 | | 5.6 | ns |
| $t_{WP}$ | 3.2 | | 3.7 | | 4.4 | | ns |
| $t_{WDSU}$ | 2.4 | | 2.8 | | 3.3 | | ns |
| $t_{WDH}$ | 0.2 | | 0.2 | | 0.3 | | ns |
| $t_{WASU}$ | 0.2 | | 0.2 | | 0.3 | | ns |
| $t_{WAH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WO}$ | | 3.4 | | 3.9 | | 4.6 | ns |
| $t_{DD}$ | | 3.4 | | 3.9 | | 4.6 | ns |
| $t_{EABOUT}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{EABCH}$ | 2.5 | | 3.5 | | 4.0 | | ns |
| $t_{EABCL}$ | 3.2 | | 3.7 | | 4.4 | | ns |

*Table 110. EPF10K250A Device Interconnect Timing Microparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 7.8 | | 8.5 | | 9.4 | ns |
| $t_{DIN2LE}$ | | 2.7 | | 3.1 | | 3.5 | ns |
| $t_{DIN2DATA}$ | | 1.6 | | 1.6 | | 1.7 | ns |
| $t_{DCLK2IOE}$ | | 3.6 | | 4.0 | | 4.6 | ns |
| $t_{DCLK2LE}$ | | 2.7 | | 3.1 | | 3.5 | ns |
| $t_{SAMELAB}$ | | 0.2 | | 0.3 | | 0.3 | ns |
| $t_{SAMEROW}$ | | 6.7 | | 7.3 | | 8.2 | ns |
| $t_{SAMECOLUMN}$ | | 2.5 | | 2.7 | | 3.0 | ns |
| $t_{DIFFROW}$ | | 9.2 | | 10.0 | | 11.2 | ns |
| $t_{TWOROWS}$ | | 15.9 | | 17.3 | | 19.4 | ns |
| $t_{LEPERIPH}$ | | 7.5 | | 8.1 | | 8.9 | ns |
| $t_{LABCARRY}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{LABCASC}$ | | 0.4 | | 0.4 | | 0.5 | ns |

*Table 111. EPF10K250A Device External Reference Timing Parameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 15.0 | | 17.0 | | 20.0 | ns |
| $t_{INSU}$ *(2), (3)* | 6.9 | | 8.0 | | 9.4 | | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(3)* | 2.0 | 8.0 | 2.0 | 8.9 | 2.0 | 10.4 | ns |

*Table 112. EPF10K250A Device External Bidirectional Timing Parameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 9.3 | | 10.6 | | 12.7 | | ns |
| $t_{INHBIDIR}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ | 2.0 | 8.0 | 2.0 | 8.9 | 2.0 | 10.4 | ns |
| $t_{XZBIDIR}$ | | 10.8 | | 12.2 | | 14.2 | ns |
| $t_{ZXBIDIR}$ | | 10.8 | | 12.2 | | 14.2 | ns |

SRAM configuration elements allow FLEX 10K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation.

The entire reconfiguration process may be completed in less than 320 ms using an EPF10K250A device with a DCLK frequency of 10 MHz. This process can be used to reconfigure an entire system dynamically. In-field upgrades can be performed by distributing new configuration files.

Refer to the configuration device data sheet to obtain the POR delay when using a configuration device method.

## Programming Files

Despite being function- and pin-compatible, FLEX 10KA and FLEX 10KE devices are not programming- or configuration-file compatible with FLEX 10K devices. A design should be recompiled before it is transferred from a FLEX 10K device to an equivalent FLEX 10KA or FLEX 10KE device. This recompilation should be performed to create a new programming or configuration file and to check design timing on the faster FLEX 10KA or FLEX 10KE device. The programming or configuration files for EPF10K50 devices can program or configure an EPF10K50V device. However, Altera recommends recompiling a design for the EPF10K50V device when transferring it from the EPF10K50 device.

## Configuration Schemes

The configuration data for a FLEX 10K device can be loaded with one of five configuration schemes (see Table 116), chosen on the basis of the target application. An EPC1, EPC2, EPC16, or EPC1441 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of a FLEX 10K device, allowing automatic configuration on system power-up.