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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	47
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2131fbd64-01-11

3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	RAM	ADC	DAC	Enhanced UARTs, ADC, Fast I/Os, and BOD	Temperature range
LPC2131FBD64/01	32 kB	8 kB	1	-	yes	−40 °C to +85 °C
LPC2132FBD64/01	64 kB	16 kB	1	1	yes	−40 °C to +85 °C
LPC2132FHN64/01	64 kB	16 kB	1	1	yes	−40 °C to +85 °C
LPC2134FBD64/01	128 kB	16 kB	2	1	yes	−40 °C to +85 °C
LPC2136FBD64/01	256 kB	32 kB	2	1	yes	−40 °C to +85 °C
LPC2138FBD64/01	512 kB	32 kB	2	1	yes	−40 °C to +85 °C
LPC2138FHN64/01	512 kB	32 kB	2	1	yes	−40 °C to +85 °C

5. Pinning information

5.1 Pinning

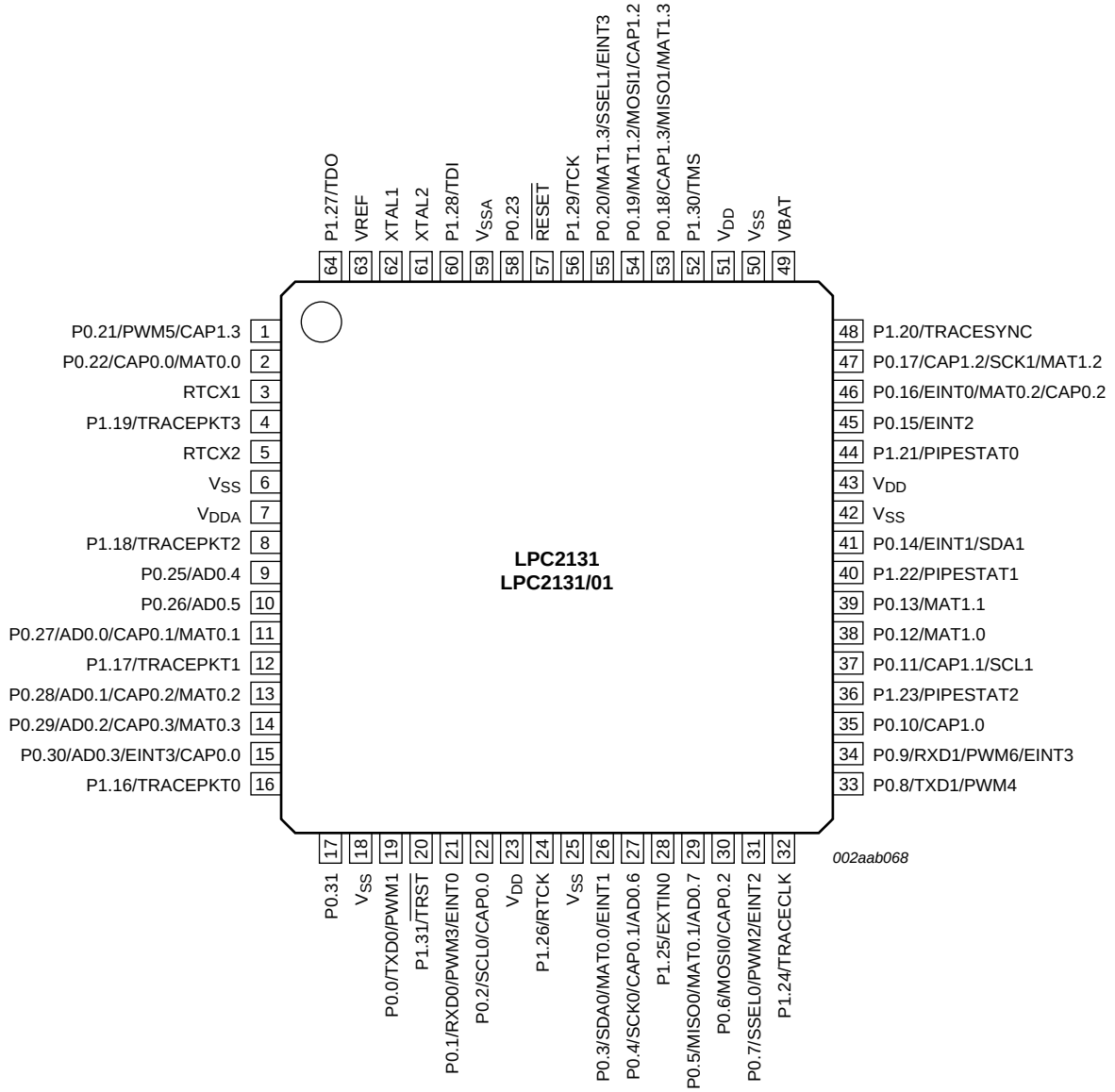


Fig 2. LPC2131 LQFP64 pin configuration

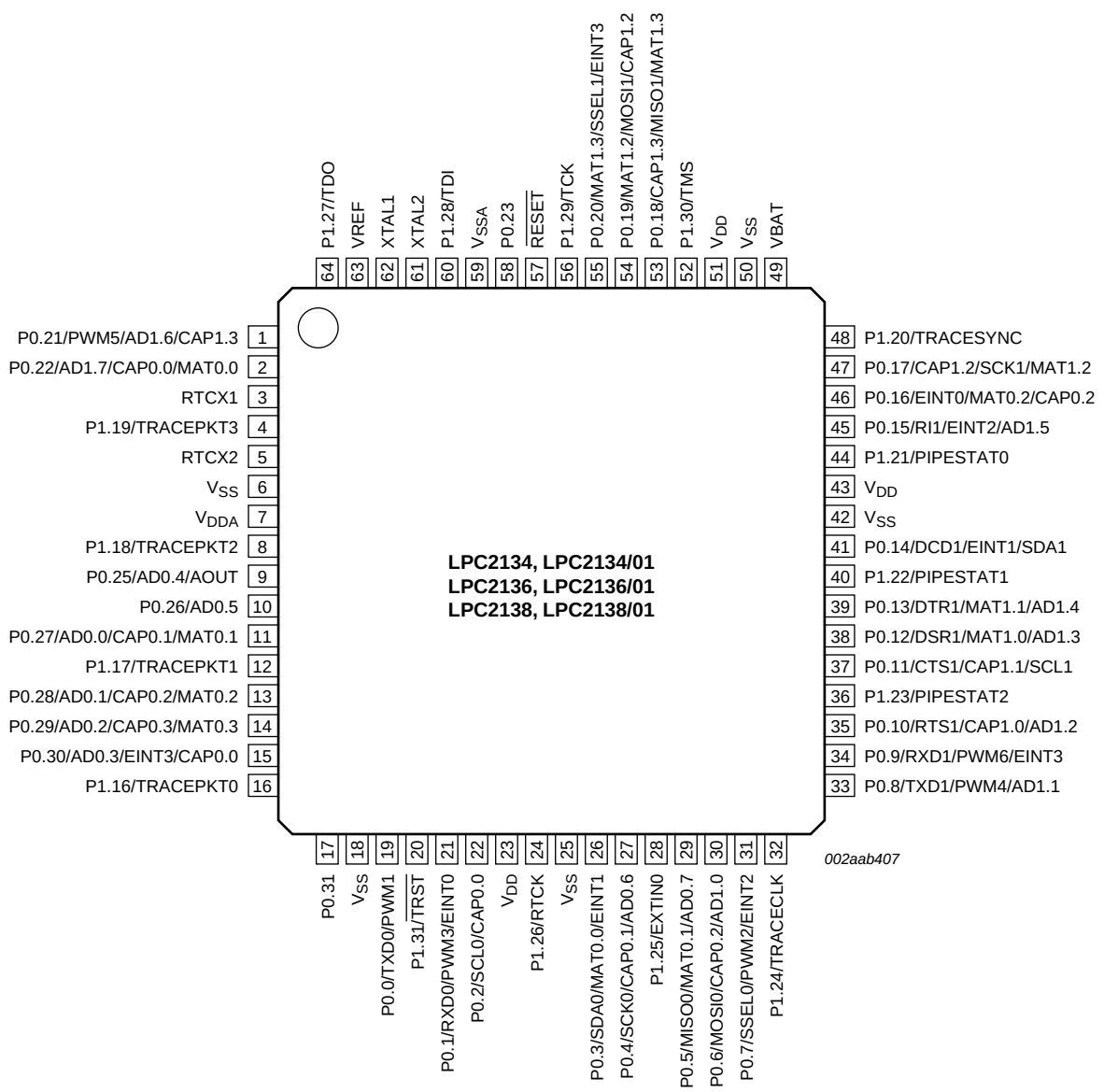
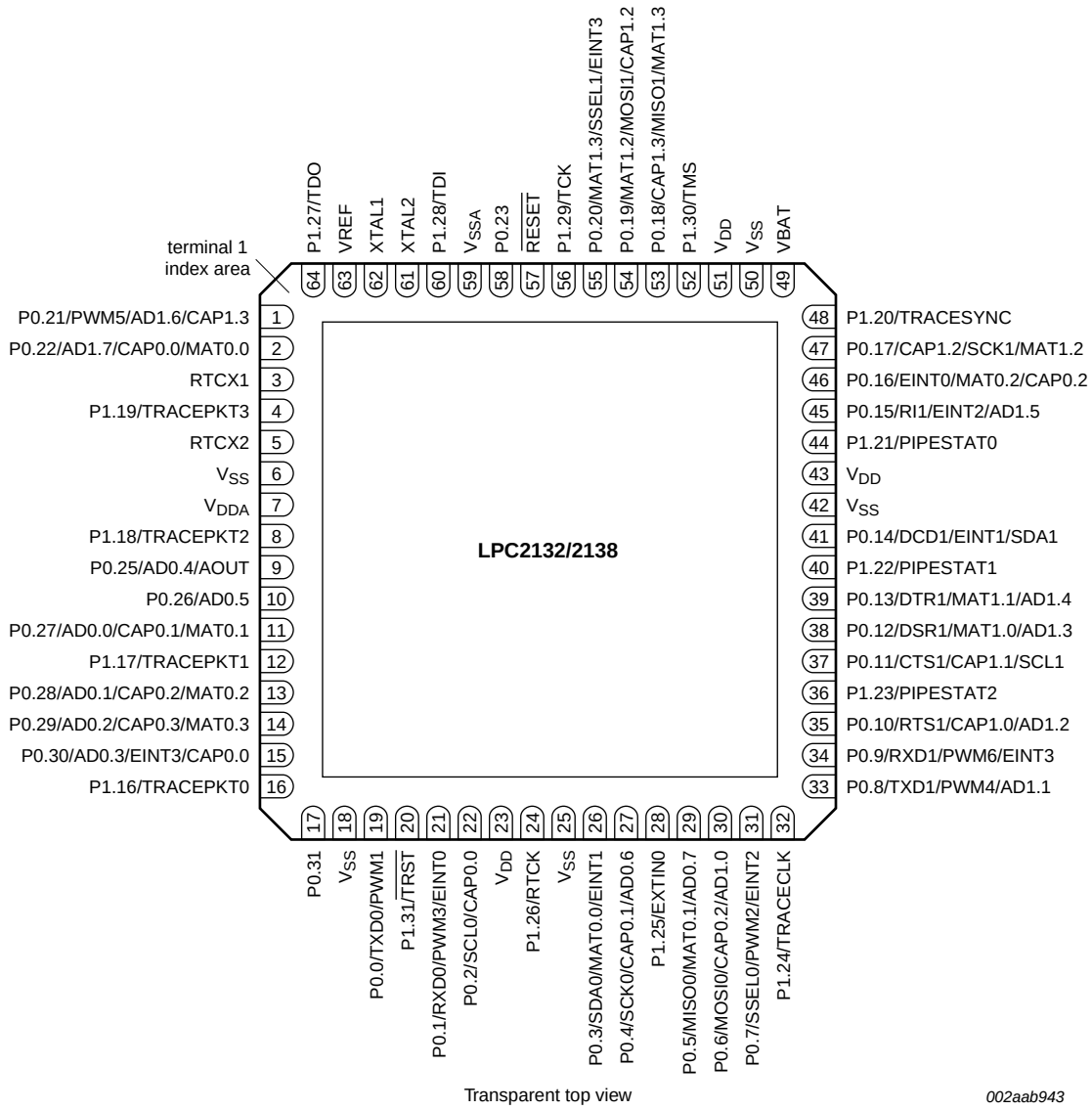


Fig 4. LPC2134/36/38 LQFP64 pin configuration



AD1.7 to AD1.0 only available on LPC2134/36/38.

Fig 5. LPC2132/38 HVQFN64 pin configuration

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P0.11/CTS1/ CAP1.1/SCL1	37[3]	I	**CTS1 —** Clear to Send input for UART1. Available in LPC2134/36/38.
		I	**CAP1.1 —** Capture input for Timer 1, channel 1.
		I/O	**SCL1 —** I^2C1 clock input/output. Open drain output (for I^2C-bus compliance)
P0.12/DSR1/ MAT1.0/AD1.3	38[4]	I	**DSR1 —** Data Set Ready input for UART1. Available in LPC2134/36/38.
		O	**MAT1.0 —** Match output for Timer 1, channel 0.
		I	**AD1.3 —** ADC 1, input 3. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
P0.13/DTR1/ MAT1.1/AD1.4	39[4]	O	**DTR1 —** Data Terminal Ready output for UART1. Available in LPC2134/36/38.
		O	**MAT1.1 —** Match output for Timer 1, channel 1.
		I	**AD1.4 —** ADC 1, input 4. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
P0.14/DCD1/ EINT1/SDA1	41[3]	I	**DCD1 —** Data Carrier Detect input for UART1. Available in LPC2134/36/38.
		I	**EINT1 —** External interrupt 1 input.
		I/O	**SDA1 —** I^2C1 data input/output. Open drain output (for I^2C-bus compliance).
P0.15/RI1/ EINT2/AD1.5	45[4]	I	**RI1 —** Ring Indicator input for UART1. Available in LPC2134/36/38.
		I	**EINT2 —** External interrupt 2 input.
		I	**AD1.5 —** ADC 1, input 5. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
P0.16/EINT0/ MAT0.2/CAP0.2	46[2]	I	**EINT0 —** External interrupt 0 input.
		O	**MAT0.2 —** Match output for Timer 0, channel 2.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
P0.17/CAP1.2/ SCK1/MAT1.2	47[1]	I	**CAP1.2 —** Capture input for Timer 1, channel 2.
		I/O	**SCK1 —** Serial Clock for SSP. Clock output from master or input to slave.
		O	**MAT1.2 —** Match output for Timer 1, channel 2.
P0.18/CAP1.3/ MISO1/MAT1.3	53[1]	I	**CAP1.3 —** Capture input for Timer 1, channel 3.
		I/O	**MISO1 —** Master In Slave Out for SSP. Data input to SPI master or data output from SSP slave.
		O	**MAT1.3 —** Match output for Timer 1, channel 3.
P0.19/MAT1.2/ MOSI1/CAP1.2	54[1]	O	**MAT1.2 —** Match output for Timer 1, channel 2.
		I/O	**MOSI1 —** Master Out Slave In for SSP. Data output from SSP master or data input to SSP slave.
		I	**CAP1.2 —** Capture input for Timer 1, channel 2.
P0.20/MAT1.3/ SSEL1/EINT3	55[2]	O	**MAT1.3 —** Match output for Timer 1, channel 3.
		I	**SSEL1 —** Slave Select for SSP. Selects the SSP interface as a slave.
		I	**EINT3 —** External interrupt 3 input.
P0.21/PWM5/ AD1.6/CAP1.3	1[4]	O	**PWM5 —** Pulse Width Modulator output 5.
		I	**AD1.6 —** ADC 1, input 6. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
		I	**CAP1.3 —** Capture input for Timer 1, channel 3.
P0.22/AD1.7/ CAP0.0/MAT0.0	2[4]	I	**AD1.7 —** ADC 1, input 7. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
		O	**MAT0.0 —** Match output for Timer 0, channel 0.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P0.23	58[1]	I/O	General purpose digital input/output pin.
P0.25/AD0.4/ AOUT	9[5]	I	**AD0.4 —** ADC 0, input 4. This analog input is always connected to its pin.
		O	**AOUT —** DAC output. Not available in LPC2131.
P0.26/AD0.5	10[4]	I	**AD0.5 —** ADC 0, input 5. This analog input is always connected to its pin.
P0.27/AD0.0/ CAP0.1/MAT0.1	11[4]	I	**AD0.0 —** ADC 0, input 0. This analog input is always connected to its pin.
		I	**CAP0.1 —** Capture input for Timer 0, channel 1.
		O	**MAT0.1 —** Match output for Timer 0, channel 1.
P0.28/AD0.1/ CAP0.2/MAT0.2	13[4]	I	**AD0.1 —** ADC 0, input 1. This analog input is always connected to its pin.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
		O	**MAT0.2 —** Match output for Timer 0, channel 2.
P0.29/AD0.2/ CAP0.3/MAT0.3	14[4]	I	**AD0.2 —** ADC 0, input 2. This analog input is always connected to its pin.
		I	**CAP0.3 —** Capture input for Timer 0, channel 3.
		O	**MAT0.3 —** Match output for Timer 0, channel 3.
P0.30/AD0.3/ EINT3/CAP0.0	15[4]	I	**AD0.3 —** ADC 0, input 3. This analog input is always connected to its pin.
		I	**EINT3 —** External interrupt 3 input.
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.31	17[6]	O	General purpose digital output only pin. **Important:** This pin MUST NOT be externally pulled LOW when $\overline{\text{RESET}}$ pin is LOW or the JTAG port will be disabled.
P1.0 to P1.31		I/O	**Port 1:** Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the pin connect block. Pins 0 through 15 of port 1 are not available.
P1.16/ TRACEPKT0	16[6]	O	**TRACEPKT0 —** Trace Packet, bit 0. Standard I/O port with internal pull-up.
P1.17/ TRACEPKT1	12[6]	O	**TRACEPKT1 —** Trace Packet, bit 1. Standard I/O port with internal pull-up.
P1.18/ TRACEPKT2	8[6]	O	**TRACEPKT2 —** Trace Packet, bit 2. Standard I/O port with internal pull-up.
P1.19/ TRACEPKT3	4[6]	O	**TRACEPKT3 —** Trace Packet, bit 3. Standard I/O port with internal pull-up.
P1.20/ TRACESYNC	48[6]	O	**TRACESYNC —** Trace Synchronization. Standard I/O port with internal pull-up. LOW on TRACESYNC while $\overline{\text{RESET}}$ is LOW enables pins P1.25:16 to operate as Trace port after reset.
P1.21/ PIPESTAT0	44[6]	O	**PIPESTAT0 —** Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P1.22/ PIPESTAT1	40[6]	O	**PIPESTAT1 —** Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P1.23/ PIPESTAT2	36[6]	O	**PIPESTAT2 —** Pipeline Status, bit 2. Standard I/O port with internal pull-up.
P1.24/ TRACECLK	32[6]	O	**TRACECLK —** Trace Clock. Standard I/O port with internal pull-up.
P1.25/EXTIN0	28[6]	I	**EXTIN0 —** External Trigger Input. Standard I/O with internal pull-up.

6.5 Interrupt controller

The Vectored Interrupt Controller (VIC) accepts all of the interrupt request inputs and categorizes them as Fast Interrupt reQuest (FIQ), vectored Interrupt ReQuest (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are requesting, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.5.1 Interrupt sources

Table 4 lists the interrupt sources for each peripheral function. Each peripheral device has one interrupt line connected to the Vectored Interrupt Controller, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Table 4. Interrupt sources

Block	Flag(s)	VIC channel #
WDT	Watchdog Interrupt (WDINT)	0
-	Reserved for software interrupts only	1
ARM Core	EmbeddedICE, DbgCommRX	2
ARM Core	EmbeddedICE, DbgCommTX	3
TIMER0	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	4
TIMER1	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	5
UART0	RX Line Status (RLS) Transmit Holding Register empty (THRE) RX Data Available (RDA) Character Time-out Indicator (CTI)	6

Table 4. Interrupt sources *…continued*

Block	Flag(s)	VIC channel #
UART1	RX Line Status (RLS)	7
	Transmit Holding Register empty (THRE)	
	RX Data Available (RDA)	
	Character Time-out Indicator (CTI)	
	Modem Status Interrupt (MSI) (Available in LPC2134/36/38 only)	
PWM0	Match 0 to 6 (MR0, MR1, MR2, MR3, MR4, MR5, MR6)	8
	Capture 0 to 3 (CR0, CR1, CR2, CR3)	
I^2C0	SI (state change)	9
SPI0	SPIF, MODF	10
SSP	TX FIFO at least half empty (TXRIS)	11
	RX FIFO at least half full (RXRIS)	
	Receive Timeout (RTRIS)	
	Receive Overrun (RORRIS)	
PLL	PLL Lock (PLOCK)	12
RTC	RTCCIF (Counter Increment), RTCALF (Alarm)	13
System Control	External Interrupt 0 (EINT0)	14
	External Interrupt 1 (EINT1)	15
	External Interrupt 2 (EINT2)	16
	External Interrupt 3 (EINT3)	17
AD0	ADC 0	18
I2C1	SI (state change)	19
BOD	Brown Out Detect	20
AD1	ADC 1 (Available in LPC2134/36/38 only)	21

6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

6.7 General purpose parallel I/O and Fast I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

6.7.1 Features

- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.7.2 Fast I/O features available in LPC213x/01 only

- Fast I/O registers are located on the ARM local bus for the fastest possible I/O timing.
- All GPIO registers are byte addressable.
- Entire port value can be written in one instruction.
- Mask registers allow single instruction to set or clear any number of bits in one port.

6.8 10-bit ADC

The LPC2131/32 contain one and the LPC2134/36/38 contain two ADCs. These converters are single 10-bit successive approximation ADCs with eight multiplexed channels.

6.8.1 Features

- Measurement range of 0 V to 3.3 V.
- Each converter capable of performing more than 400000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal.
- Global Start command for both converters (LPC2134/36/38 only).

6.8.2 ADC features available in LPC213x/01 only

- Every analog input has a dedicated result register to reduce interrupt overhead.
- Every analog input can generate an interrupt once the conversion is completed.

6.9 10-bit DAC

This peripheral is available in the LPC2132/34/36/38 only. The DAC enables the LPC2132/34/36/38 to generate variable analog output.

6.9.1 Features

- 10-bit digital to analog converter.
- Buffered output.
- Power-down mode available.
- Selectable speed versus power.

6.10 UARTs

The LPC2131/32/34/36/38 each contain two UARTs. In addition to standard transmit and receive data lines, the LPC2134/36/38 UART1 also provides a full modem control handshake interface.

6.10.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B

- Built-in baud rate generator.
- Standard modem interface signals included on UART1. (LPC2134/36/38 only)
- The LPC2131/32/34/36/38 transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs and hardware (CTS/RTS) flow control on the LPC2134/36/38 UART1 only.

6.10.2 UART features available in LPC213x/01 only

- Fractional baud rate generator enables standard baud rates such as 115200 to be achieved with any crystal frequency above 2 MHz.
- Auto-bauding.
- Auto-CTS/RTS flow-control fully implemented in hardware (LPC2134/36/38 only).

6.11 I^2C-bus serial I/O controller

The LPC2131/32/34/36/38 each contain two I^2C-bus controllers.

The I^2C-bus is bidirectional, for inter-IC control using only two wires: a Serial Clock Line (SCL), and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver or a transmitter with the capability to both receive and send information (such as memory)). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

This I^2C-bus implementation supports bit rates up to 400 kbit/s (Fast I^2C).

6.11.1 Features

- Standard I^2C compliant bus interface.
- Easy to configure as Master, Slave, or Master/Slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus may be used for test and diagnostic purposes.

6.12 SPI serial I/O controller

The LPC2131/32/34/36/38 each contain one SPI controller. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

6.12.1 Features

- Compliant with Serial Peripheral Interface (SPI) specification.
- Synchronous, Serial, Full Duplex, Communication.
- Combined SPI master and slave.
- Maximum data bit rate of one eighth of the input clock rate.

6.13 SSP serial I/O controller

The LPC2131/32/34/36/38 each contain one Serial Synchronous Port controller (SSP). The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. However, only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. Often only one of these data flows carries meaningful data.

6.13.1 Features

- Compatible with Motorola SPI, 4-wire TI SSI and National Semiconductor Microwire buses.
- Synchronous Serial Communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- Four bits to 16 bits per frame.

6.14 General purpose timers/external event counters

The Timer/Counter is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock, and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with ‘or’ and ‘and’, as well as ‘broadcast’ functions among them.

At any given time only one of peripheral’s capture inputs can be selected as an external event signal source, i.e., timer’s clock. The rate of external events that can be successfully counted is limited to PCLK/2. In this configuration, unused capture lines can be selected as regular timer capture inputs.

6.14.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.
- External Event Counter or timer operation.
- Four 32-bit capture channels per timer/counter that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.

- Stop timer on match with optional interrupt generation.
- Reset timer on match with optional interrupt generation.

- Four external outputs per timer/counter corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

6.15 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

6.15.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal pre-scaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

6.16 Real-time clock

The Real-Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.16.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra-low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Can use either the RTC dedicated 32 kHz oscillator input or clock derived from the external crystal/oscillator input at XTAL1. Programmable Reference Clock Divider allows fine adjustment of the RTC.
- Dedicated power supply pin can be connected to a battery or the main 3.3 V.

[4] V_{DD} supply voltages must be present.

[5] 3-state outputs go into 3-state mode when V_{DD} is grounded.

[6] Please also see the errata note mentioned in the errata sheet.

[7] Accounts for 100 mV voltage drop in all supply lines.

[8] Only allowed for a short time period.

[9] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

[10] Applies to P1.16 to P1.25.

[11] On pin VBAT.

[12] Optimized for low battery consumption.

[13] To V_{SS}.

9. Dynamic characteristics

Table 7. Dynamic characteristics

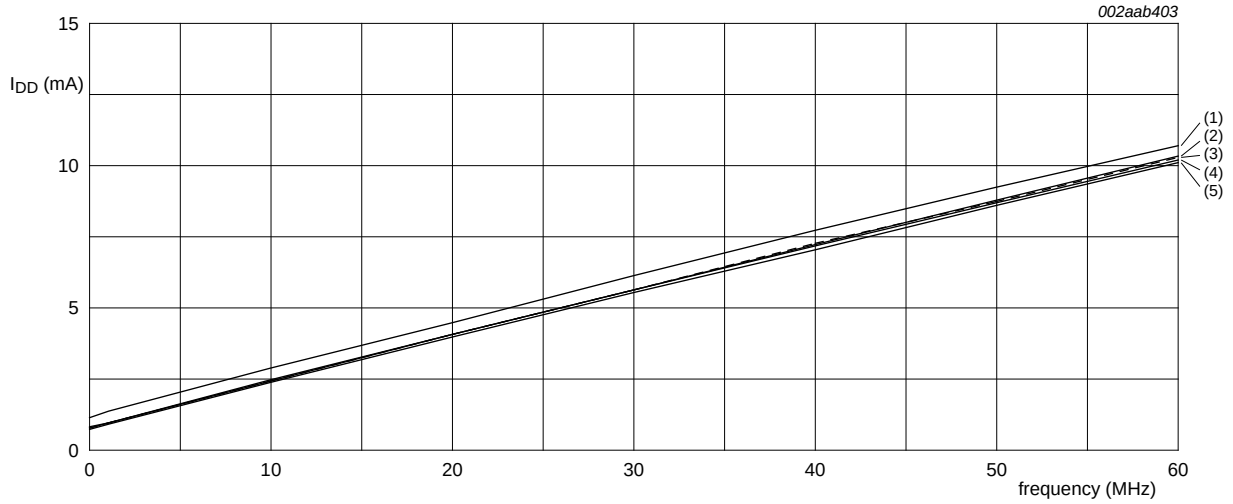
T_{amb} = −40 °C to +85 °C for commercial applications, V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
External clock						
f_{osc}	oscillator frequency		10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	100	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0.2 and P0.3)						
$t_{r(o)}$	output rise time		-	10	-	ns
$t_{f(o)}$	output fall time		-	10	-	ns
I^2C-bus pins (P0.2 and P0.3)						
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$[3]	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.



Test conditions: Idle mode entered executing code from flash; all peripherals are enabled in PCONP register; PCLK = CCLK/4.

(1) V_{DD} = 3.6 V at 140 °C (max)

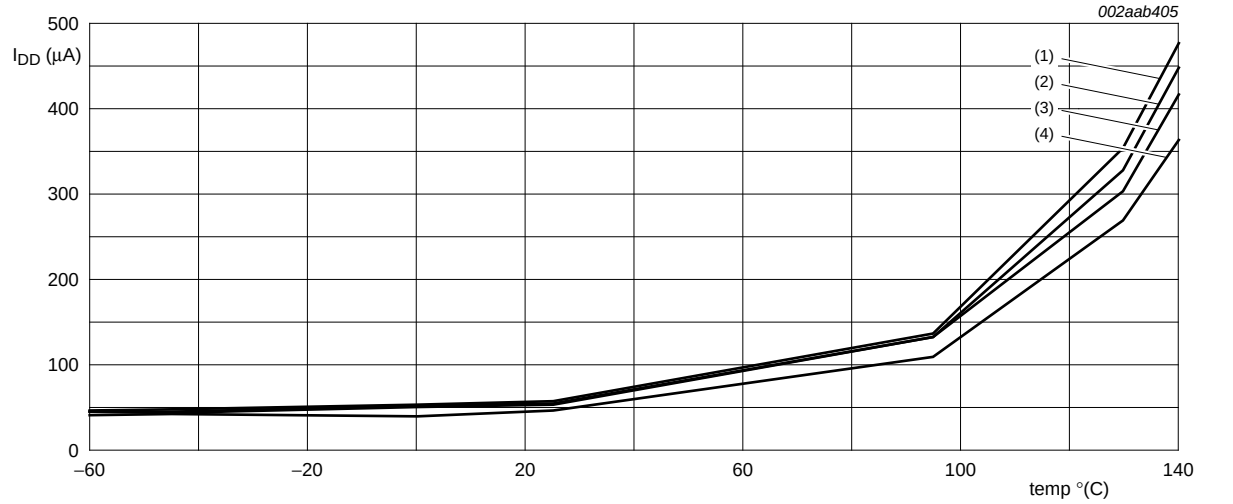
(2) V_{DD} = 3.6 V at −60 °C

(3) V_{DD} = 3.6 V at 25 °C

(4) V_{DD} = 3.3 V at 25 °C (typical)

(5) V_{DD} = 3.3 V at 95 °C (typical)

Fig 9. I_{DD} idle measured at different frequencies (CCLK) and temperatures



Test conditions: Power-down mode entered executing code from flash; all peripherals are enabled in PCONP register.

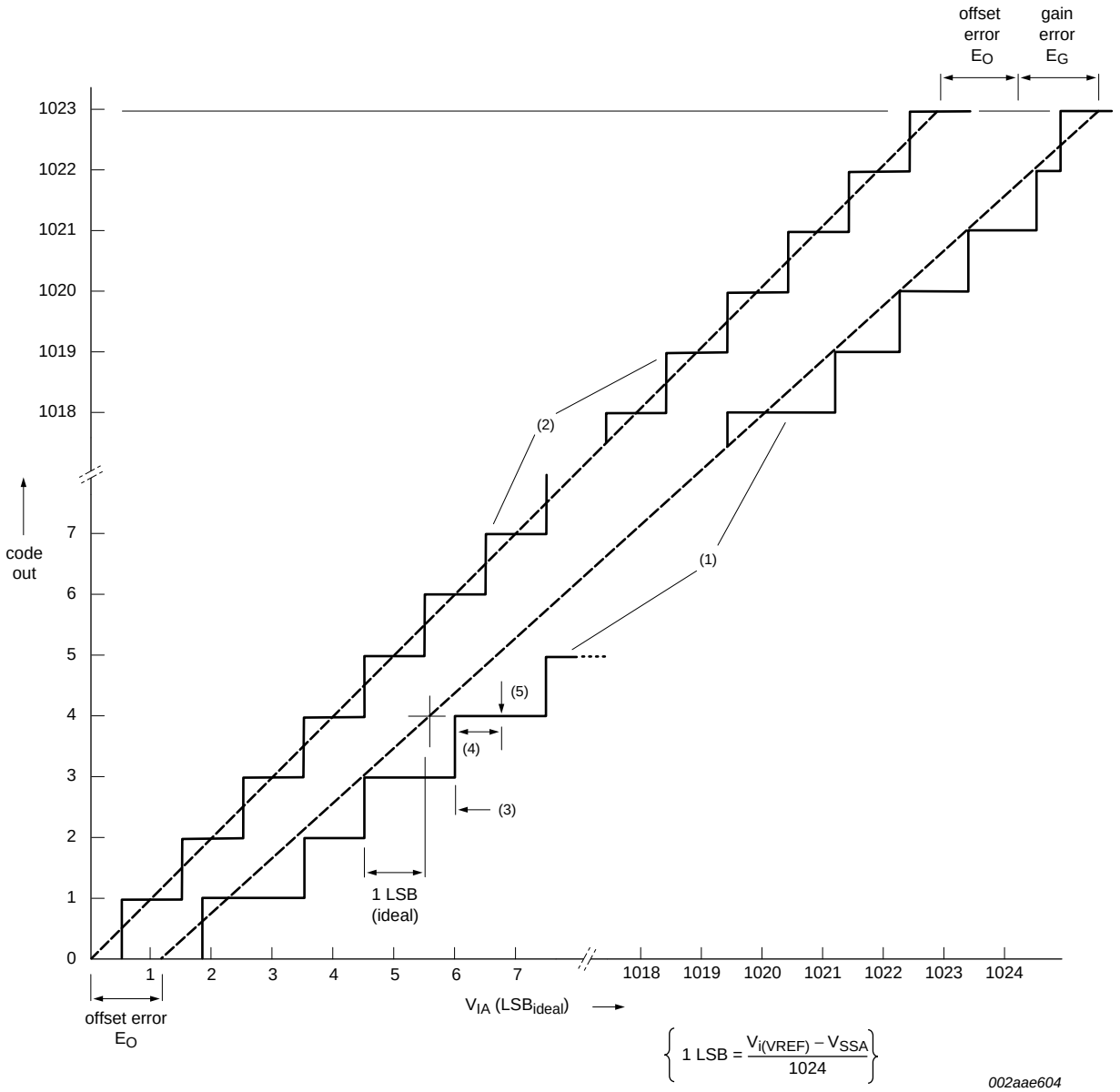
(1) V_{DD} = 3.6 V

(2) V_{DD} = 3.3 V (max)

(3) V_{DD} = 3.0 V

(4) V_{DD} = 3.3 V (typical)

Fig 10. $I_{DD(pd)}$ measured at different temperatures



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 11. ADC characteristics

12. Application information

12.1 Crystal oscillator XTAL input and component selection

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i / (C_i + C_g)$. In slave mode, a minimum of 200 mV (RMS) is needed.

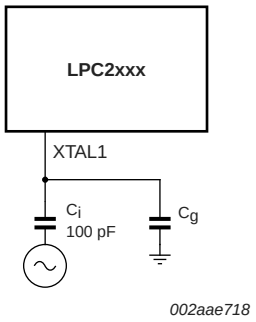


Fig 13. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 13), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTAL2 pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 14 and in Table 10 and Table 11. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 14 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer.

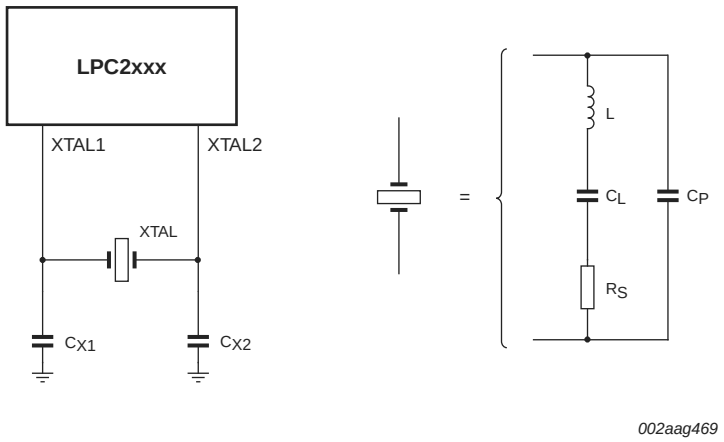


Fig 14. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 10. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 11. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

12.2 RTC 32 kHz oscillator component selection

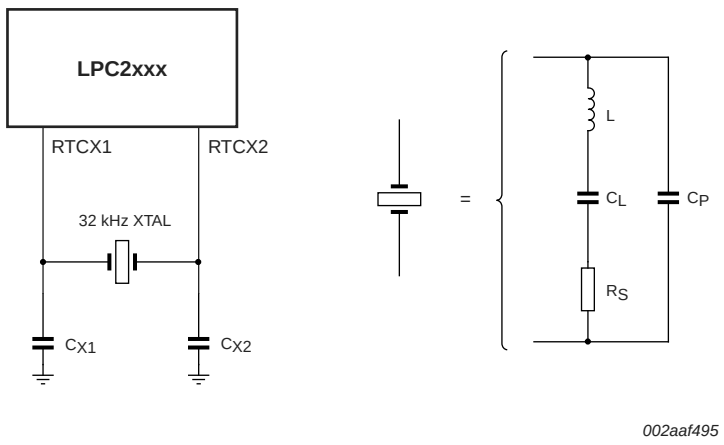


Fig 15. RTC oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

The RTC external oscillator circuit is shown in Figure 15. Since the feedback resistance is integrated on chip, only a crystal, the capacitances C_{X1} and C_{X2} need to be connected externally to the microcontroller.

Table 12 gives the crystal parameters that should be used. C_L is the typical load capacitance of the crystal and is usually specified by the crystal manufacturer. The actual C_L influences oscillation frequency. When using a crystal that is manufactured for a different load capacitance, the circuit will oscillate at a slightly different frequency (depending on the quality of the crystal) compared to the specified one. Therefore for an accurate time reference it is advised to use the load capacitors as specified in Table 12 that belong to a specific C_L. The value of external capacitances C_{X1} and C_{X2} specified in this table are calculated from the internal parasitic capacitances and the C_L. Parasitics from PCB and package are not taken into account.

Table 12. Recommended values for the RTC external 32 kHz oscillator C_{X1}/C_{X2} components

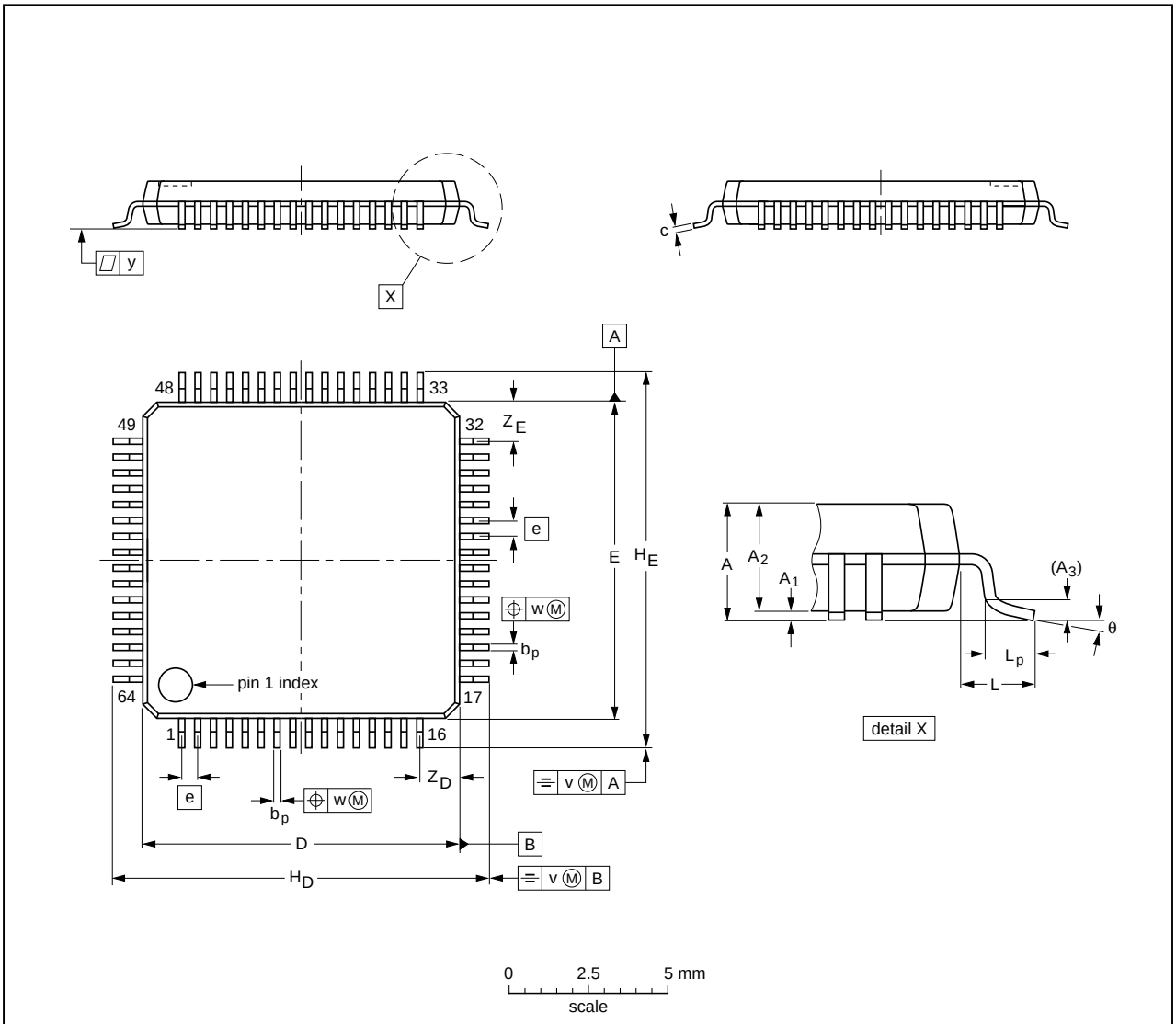
Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
11 pF	< 100 kΩ	18 pF, 18 pF
13 pF	< 100 kΩ	22 pF, 22 pF
15 pF	< 100 kΩ	27 pF, 27 pF

12.3 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plane. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

13. Package outline

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 16. Package outline SOT314-2 (LQFP64)

14. Abbreviations

Table 13. Acronym list

Acronym	Description
A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DCC	Debug Communications Channel
ETM	Embedded Trace Macrocell
FIFO	First In, First Out
GPIO	General Purpose Input/Output
JTAG	Joint Test Action Group
LSB	Least Significant Bit
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulator
RAM	Random Access Memory
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSP	Synchronous Serial Port
UART	Universal Asynchronous Receiver/Transmitter