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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	47
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2131fbd64-151

- One (LPC2131/32) or two (LPC2134/36/38) 8-channel 10-bit ADCs provide a total of up to 16 analog inputs, with conversion times as low as 2.44 μs per channel.
- Single 10-bit DAC provides variable analog output (LPC2132/34/36/38).
- Two 32-bit timers/external event counters (with four capture and four compare channels each), PWM unit (six outputs) and watchdog.
- Low power Real-time clock with independent power and dedicated 32 kHz clock input.
- Multiple serial interfaces including two UARTs (16C550), two Fast I^2C-bus (400 kbit/s), SPI and SSP with buffering and variable data length capabilities.
- Vectored interrupt controller with configurable priorities and vector addresses.
- Up to forty-seven 5 V tolerant general purpose I/O pins in tiny LQFP64 or HVQFN package.
- Up to nine edge or level sensitive external interrupt pins available.
- 60 MHz maximum CPU clock available from programmable on-chip PLL with settling time of 100 μs.
- On-chip integrated oscillator operates with external crystal in range of 1 MHz to 30 MHz and with external oscillator up to 50 MHz.
- Power saving modes include Idle and Power-down.
- Individual enable/disable of peripheral functions as well as peripheral clock scaling down for additional power optimization.
- Processor wake-up from Power-down mode via external interrupt or BOD.
- Single power supply chip with POR and BOD circuits:
  - CPU operating voltage range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2131FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2132FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2132FHN64/01	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-2
LPC2134FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2136FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2138FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2138FHN64/01	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-2

5. Pinning information

5.1 Pinning

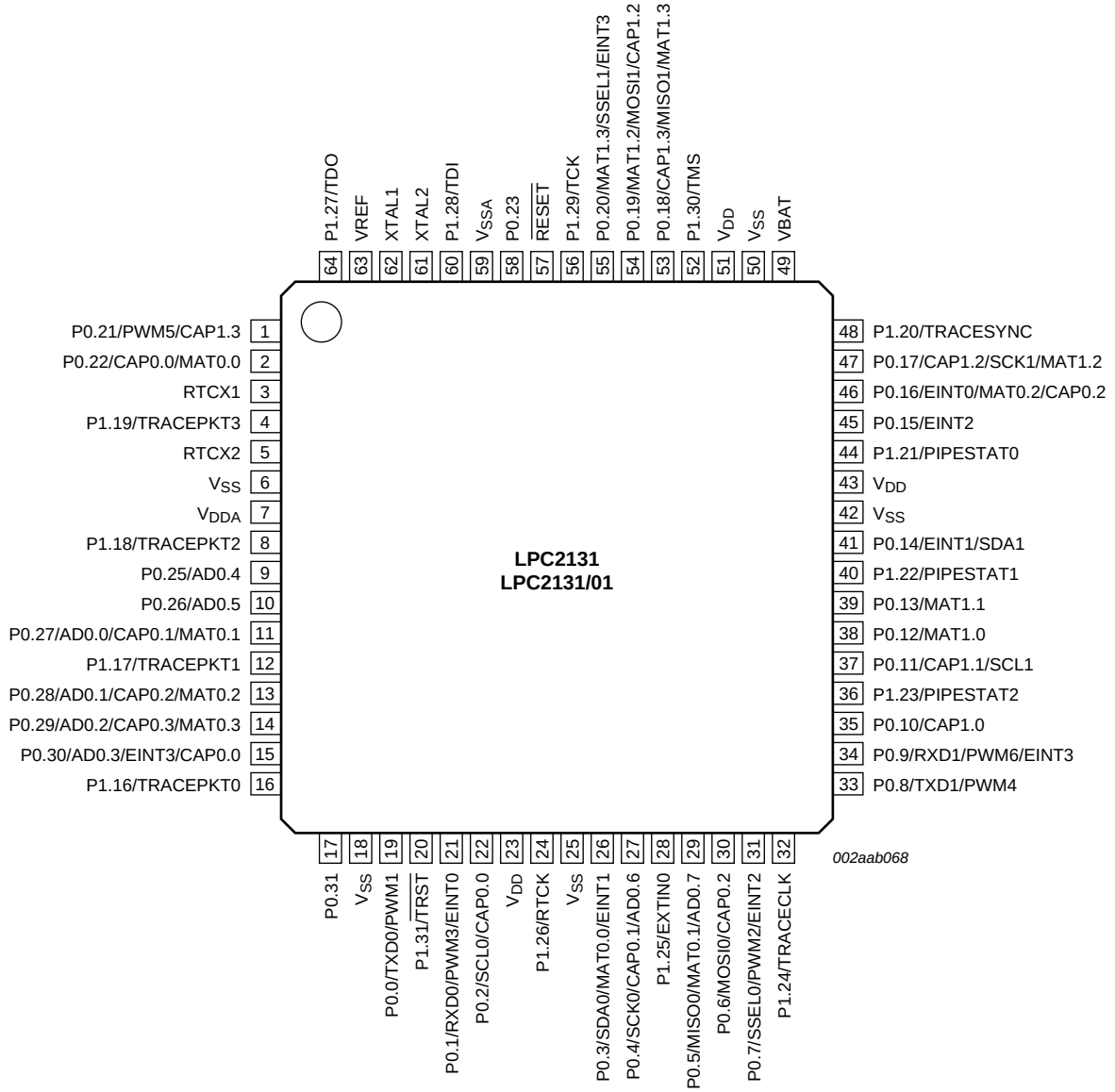


Fig 2. LPC2131 LQFP64 pin configuration

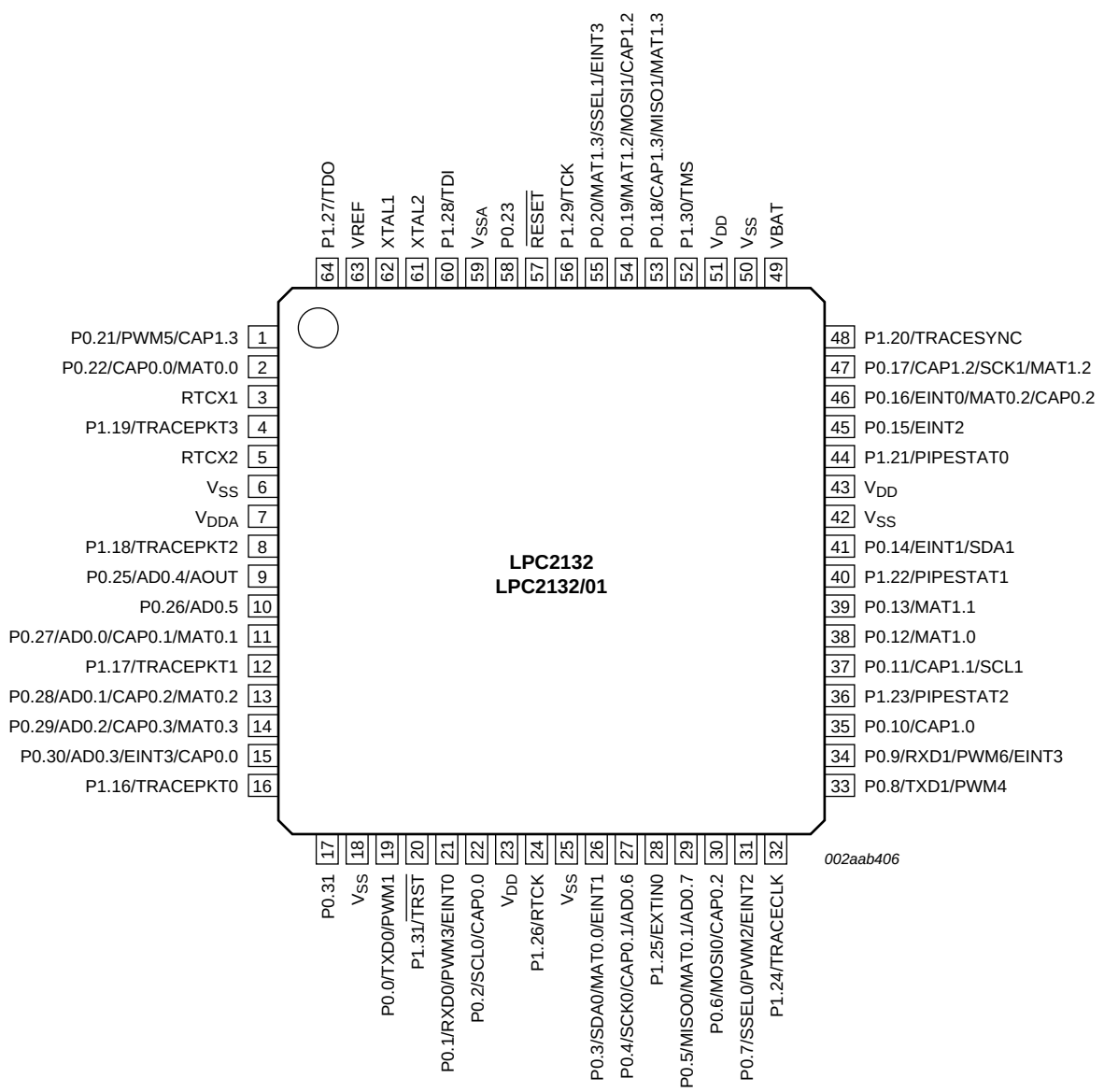


Fig 3. LPC2132 LQFP64 pin configuration

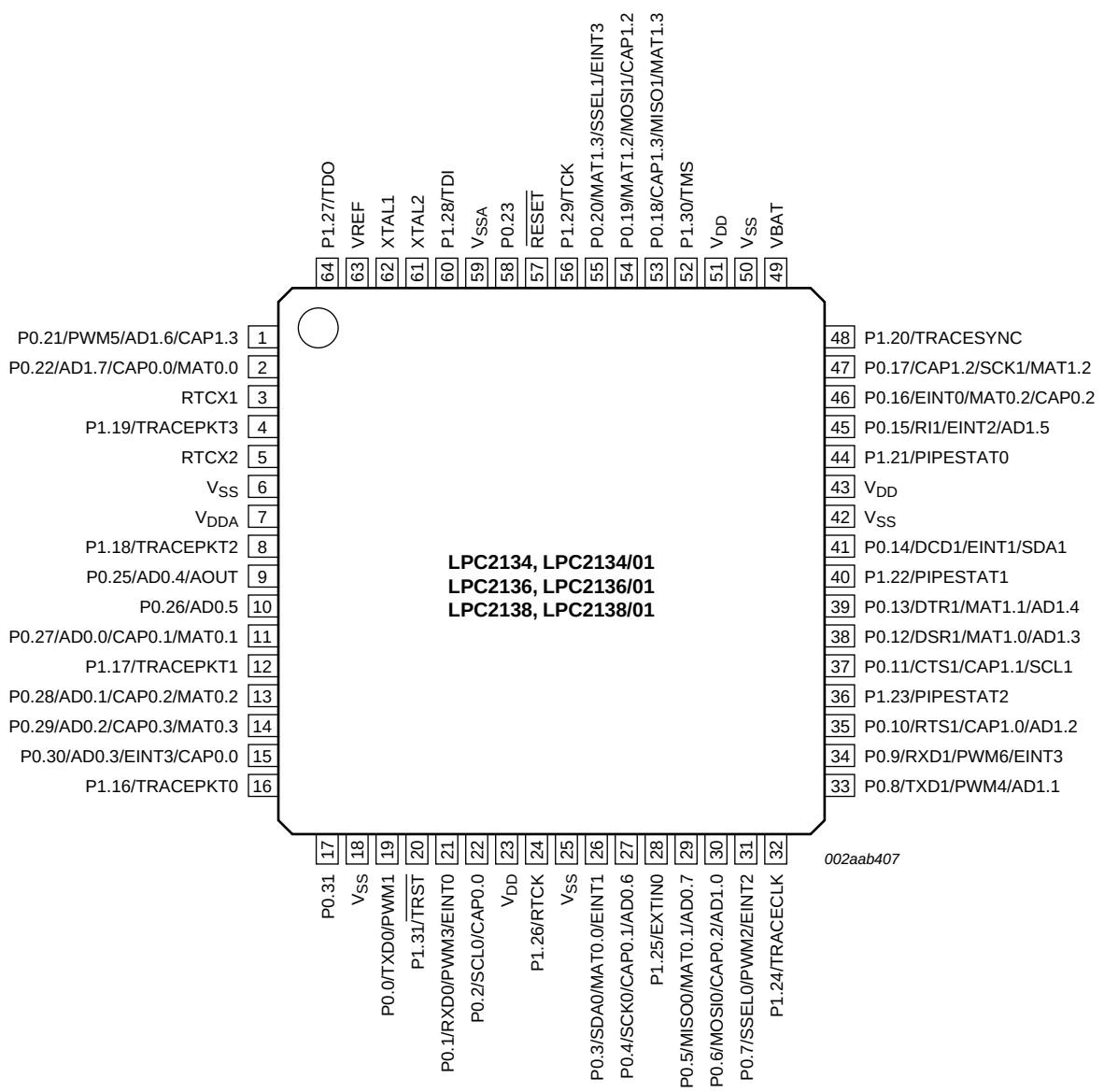


Fig 4. LPC2134/36/38 LQFP64 pin configuration

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
P0.0 to P0.31		I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. Total of 31 pins of the Port 0 can be used as a general purpose bidirectional digital I/Os while P0.31 is output only pin. The operation of port 0 pins depends upon the pin function selected via the pin connect block. Pin P0.24 is not available.
P0.0/TXD0/ PWM1	19[1]	O	**TXD0 —** Transmitter output for UART0.
		O	**PWM1 —** Pulse Width Modulator output 1.
P0.1/RXD0/ PWM3/EINT0	21[2]	I	**RXD0 —** Receiver input for UART0.
		O	**PWM3 —** Pulse Width Modulator output 3.
		I	**EINT0 —** External interrupt 0 input.
P0.2/SCL0/ CAP0.0	22[3]	I/O	**SCL0 —** I^2C0 clock input/output. Open drain output (for I^2C-bus compliance).
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.3/SDA0/ MAT0.0/EINT1	26[3]	I/O	**SDA0 —** I^2C0 data input/output. Open drain output (for I^2C-bus compliance).
		O	**MAT0.0 —** Match output for Timer 0, channel 0.
		I	**EINT1 —** External interrupt 1 input.
P0.4/SCK0/ CAP0.1/AD0.6	27[4]	I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
		I	**CAP0.1 —** Capture input for Timer 0, channel 1.
		I	**AD0.6 —** ADC 0, input 6. This analog input is always connected to its pin.
P0.5/MISO0/ MAT0.1/AD0.7	29[4]	I/O	**MISO0 —** Master In Slave V_{DD} = 3.6 V for SPI0. Data input to SPI master or data output from SPI slave.
		O	**MAT0.1 —** Match output for Timer 0, channel 1.
		I	**AD0.7 —** ADC 0, input 7. This analog input is always connected to its pin.
P0.6/MOSI0/ CAP0.2/AD1.0	30[4]	I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
		I	**AD1.0 —** ADC 1, input 0. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
P0.7/SSEL0/ PWM2/EINT2	31[2]	I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
		O	**PWM2 —** Pulse Width Modulator output 2.
		I	**EINT2 —** External interrupt 2 input.
P0.8/TXD1/ PWM4/AD1.1	33[4]	O	**TXD1 —** Transmitter output for UART1.
		O	**PWM4 —** Pulse Width Modulator output 4.
		I	**AD1.1 —** ADC 1, input 1. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
P0.9/RXD1/ PWM6/EINT3	34[2]	I	**RXD1 —** Receiver input for UART1.
		O	**PWM6 —** Pulse Width Modulator output 6.
		I	**EINT3 —** External interrupt 3 input.
P0.10/RTS1/ CAP1.0/AD1.2	35[4]	O	**RTS1 —** Request to Send output for UART1. Available in LPC2134/36/38.
		I	**CAP1.0 —** Capture input for Timer 1, channel 0.
		I	**AD1.2 —** ADC 1, input 2. This analog input is always connected to its pin. Available in LPC2134/36/38 only.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P0.23	58[1]	I/O	General purpose digital input/output pin.
P0.25/AD0.4/ AOUT	9[5]	I	**AD0.4 —** ADC 0, input 4. This analog input is always connected to its pin.
		O	**AOUT —** DAC output. Not available in LPC2131.
P0.26/AD0.5	10[4]	I	**AD0.5 —** ADC 0, input 5. This analog input is always connected to its pin.
P0.27/AD0.0/ CAP0.1/MAT0.1	11[4]	I	**AD0.0 —** ADC 0, input 0. This analog input is always connected to its pin.
		I	**CAP0.1 —** Capture input for Timer 0, channel 1.
		O	**MAT0.1 —** Match output for Timer 0, channel 1.
P0.28/AD0.1/ CAP0.2/MAT0.2	13[4]	I	**AD0.1 —** ADC 0, input 1. This analog input is always connected to its pin.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
		O	**MAT0.2 —** Match output for Timer 0, channel 2.
P0.29/AD0.2/ CAP0.3/MAT0.3	14[4]	I	**AD0.2 —** ADC 0, input 2. This analog input is always connected to its pin.
		I	**CAP0.3 —** Capture input for Timer 0, channel 3.
		O	**MAT0.3 —** Match output for Timer 0, channel 3.
P0.30/AD0.3/ EINT3/CAP0.0	15[4]	I	**AD0.3 —** ADC 0, input 3. This analog input is always connected to its pin.
		I	**EINT3 —** External interrupt 3 input.
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.31	17[6]	O	General purpose digital output only pin. **Important:** This pin MUST NOT be externally pulled LOW when $\overline{\text{RESET}}$ pin is LOW or the JTAG port will be disabled.
P1.0 to P1.31		I/O	**Port 1:** Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the pin connect block. Pins 0 through 15 of port 1 are not available.
P1.16/ TRACEPKT0	16[6]	O	**TRACEPKT0 —** Trace Packet, bit 0. Standard I/O port with internal pull-up.
P1.17/ TRACEPKT1	12[6]	O	**TRACEPKT1 —** Trace Packet, bit 1. Standard I/O port with internal pull-up.
P1.18/ TRACEPKT2	8[6]	O	**TRACEPKT2 —** Trace Packet, bit 2. Standard I/O port with internal pull-up.
P1.19/ TRACEPKT3	4[6]	O	**TRACEPKT3 —** Trace Packet, bit 3. Standard I/O port with internal pull-up.
P1.20/ TRACESYNC	48[6]	O	**TRACESYNC —** Trace Synchronization. Standard I/O port with internal pull-up. LOW on TRACESYNC while $\overline{\text{RESET}}$ is LOW enables pins P1.25:16 to operate as Trace port after reset.
P1.21/ PIPESTAT0	44[6]	O	**PIPESTAT0 —** Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P1.22/ PIPESTAT1	40[6]	O	**PIPESTAT1 —** Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P1.23/ PIPESTAT2	36[6]	O	**PIPESTAT2 —** Pipeline Status, bit 2. Standard I/O port with internal pull-up.
P1.24/ TRACECLK	32[6]	O	**TRACECLK —** Trace Clock. Standard I/O port with internal pull-up.
P1.25/EXTIN0	28[6]	I	**EXTIN0 —** External Trigger Input. Standard I/O with internal pull-up.

6. Functional description

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

6.2 On-chip flash program memory

The LPC2131/32/34/36/38 incorporate a 32 kB, 64 kB, 128 kB, 256 kB and 512 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. When the LPC2131/32/34/36/38 on-chip bootloader is used, 32/64/128/256/500 kB of flash memory is available for user code.

The LPC2131/32/34/36/38 flash memory provides a minimum of 100000 erase/write cycles and 20 years of data-retention.

6.3 On-chip static RAM

On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8-bit, 16-bit, and 32-bit. The LPC2131, LPC2132/34, and LPC2136/38 provide 8 kB, 16 kB and 32 kB of static RAM respectively.

6.5 Interrupt controller

The Vectored Interrupt Controller (VIC) accepts all of the interrupt request inputs and categorizes them as Fast Interrupt reQuest (FIQ), vectored Interrupt ReQuest (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are requesting, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.5.1 Interrupt sources

Table 4 lists the interrupt sources for each peripheral function. Each peripheral device has one interrupt line connected to the Vectored Interrupt Controller, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Table 4. Interrupt sources

Block	Flag(s)	VIC channel #
WDT	Watchdog Interrupt (WDINT)	0
-	Reserved for software interrupts only	1
ARM Core	EmbeddedICE, DbgCommRX	2
ARM Core	EmbeddedICE, DbgCommTX	3
TIMER0	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	4
TIMER1	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	5
UART0	RX Line Status (RLS) Transmit Holding Register empty (THRE) RX Data Available (RDA) Character Time-out Indicator (CTI)	6

6.7.2 Fast I/O features available in LPC213x/01 only

- Fast I/O registers are located on the ARM local bus for the fastest possible I/O timing.
- All GPIO registers are byte addressable.
- Entire port value can be written in one instruction.
- Mask registers allow single instruction to set or clear any number of bits in one port.

6.8 10-bit ADC

The LPC2131/32 contain one and the LPC2134/36/38 contain two ADCs. These converters are single 10-bit successive approximation ADCs with eight multiplexed channels.

6.8.1 Features

- Measurement range of 0 V to 3.3 V.
- Each converter capable of performing more than 400000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal.
- Global Start command for both converters (LPC2134/36/38 only).

6.8.2 ADC features available in LPC213x/01 only

- Every analog input has a dedicated result register to reduce interrupt overhead.
- Every analog input can generate an interrupt once the conversion is completed.

6.9 10-bit DAC

This peripheral is available in the LPC2132/34/36/38 only. The DAC enables the LPC2132/34/36/38 to generate variable analog output.

6.9.1 Features

- 10-bit digital to analog converter.
- Buffered output.
- Power-down mode available.
- Selectable speed versus power.

6.10 UARTs

The LPC2131/32/34/36/38 each contain two UARTs. In addition to standard transmit and receive data lines, the LPC2134/36/38 UART1 also provides a full modem control handshake interface.

6.10.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B

- Built-in baud rate generator.
- Standard modem interface signals included on UART1. (LPC2134/36/38 only)
- The LPC2131/32/34/36/38 transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs and hardware (CTS/RTS) flow control on the LPC2134/36/38 UART1 only.

6.10.2 UART features available in LPC213x/01 only

- Fractional baud rate generator enables standard baud rates such as 115200 to be achieved with any crystal frequency above 2 MHz.
- Auto-bauding.
- Auto-CTS/RTS flow-control fully implemented in hardware (LPC2134/36/38 only).

6.11 I^2C-bus serial I/O controller

The LPC2131/32/34/36/38 each contain two I^2C-bus controllers.

The I^2C-bus is bidirectional, for inter-IC control using only two wires: a Serial Clock Line (SCL), and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver or a transmitter with the capability to both receive and send information (such as memory)). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

This I^2C-bus implementation supports bit rates up to 400 kbit/s (Fast I^2C).

6.11.1 Features

- Standard I^2C compliant bus interface.
- Easy to configure as Master, Slave, or Master/Slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus may be used for test and diagnostic purposes.

6.12 SPI serial I/O controller

The LPC2131/32/34/36/38 each contain one SPI controller. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

- Stop timer on match with optional interrupt generation.
- Reset timer on match with optional interrupt generation.

- Four external outputs per timer/counter corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

6.15 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

6.15.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal pre-scaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

6.16 Real-time clock

The Real-Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.16.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra-low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Can use either the RTC dedicated 32 kHz oscillator input or clock derived from the external crystal/oscillator input at XTAL1. Programmable Reference Clock Divider allows fine adjustment of the RTC.
- Dedicated power supply pin can be connected to a battery or the main 3.3 V.

6.17 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2131/32/34/36/38. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.17.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.

- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.

6.18 System control

6.18.1 Crystal oscillator

On-chip integrated oscillator operates with external crystal in range of 1 MHz to 30 MHz and with external oscillator up to 50 MHz. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.18.2 “PLL” for additional information.

6.18.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μs.

6.18.3 Reset and wake-up timer

Reset has two sources on the LPC2131/32/34/36/38: the $\overline{\text{RESET}}$ pin and watchdog reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the wake-up timer (see wake-up timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The wake-up timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up timer.

The wake-up timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

6.18.4 Brownout detector

The LPC2131/32/34/36/38 include 2-stage monitoring of the voltage on the V_{DD} pins. If this voltage falls below 2.9 V, the BOD asserts an interrupt signal to the Vectored Interrupt Controller. This signal can be enabled for interrupt; if not, software can monitor the signal by reading dedicated register.

The second stage of low-voltage detection asserts reset to inactivate the LPC2131/32/34/36/38 when the voltage on the V_{DD} pins falls below 2.6 V. This reset prevents alteration of the flash as operation of the various elements of the chip would otherwise become unreliable due to low voltage. The BOD circuit maintains this reset down below 1 V, at which point the POR circuitry maintains the overall reset.

Both the 2.9 V and 2.6 V thresholds include some hysteresis. In normal operation, this hysteresis allows the 2.9 V detection to reliably interrupt, or a regularly-executed event loop to sense the condition.

Features available only in LPC213x/01 parts include ability to put the BOD in power-down mode, turn it on or off and to control when the BOD will reset the LPC213x/01 microcontroller. This can be used to further reduce power consumption when a low power mode (such as Power Down) is invoked.

6.18.5 Code security

This feature of the LPC2131/32/34/36/38 allow an application to control whether it can be debugged or protected from observation.

If after reset on-chip bootloader detects a valid checksum in flash and reads 0x8765 4321 from address 0x1FC in flash, debugging will be disabled and thus the code in flash will be protected from observation. Once debugging is disabled, it can be enabled only by performing a full chip erase using the ISP.

6.18.6 External interrupt inputs

The LPC2131/32/34/36/38 include up to nine edge or level sensitive External Interrupt Inputs as selectable pin functions. When the pins are combined, external events can be processed as four independent interrupt signals. The External Interrupt Inputs can optionally be used to wake up the processor from Power-down mode.

6.18.7 Memory Mapping Control

The Memory Mapping Control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

Table 6. Static characteristics *…continued*

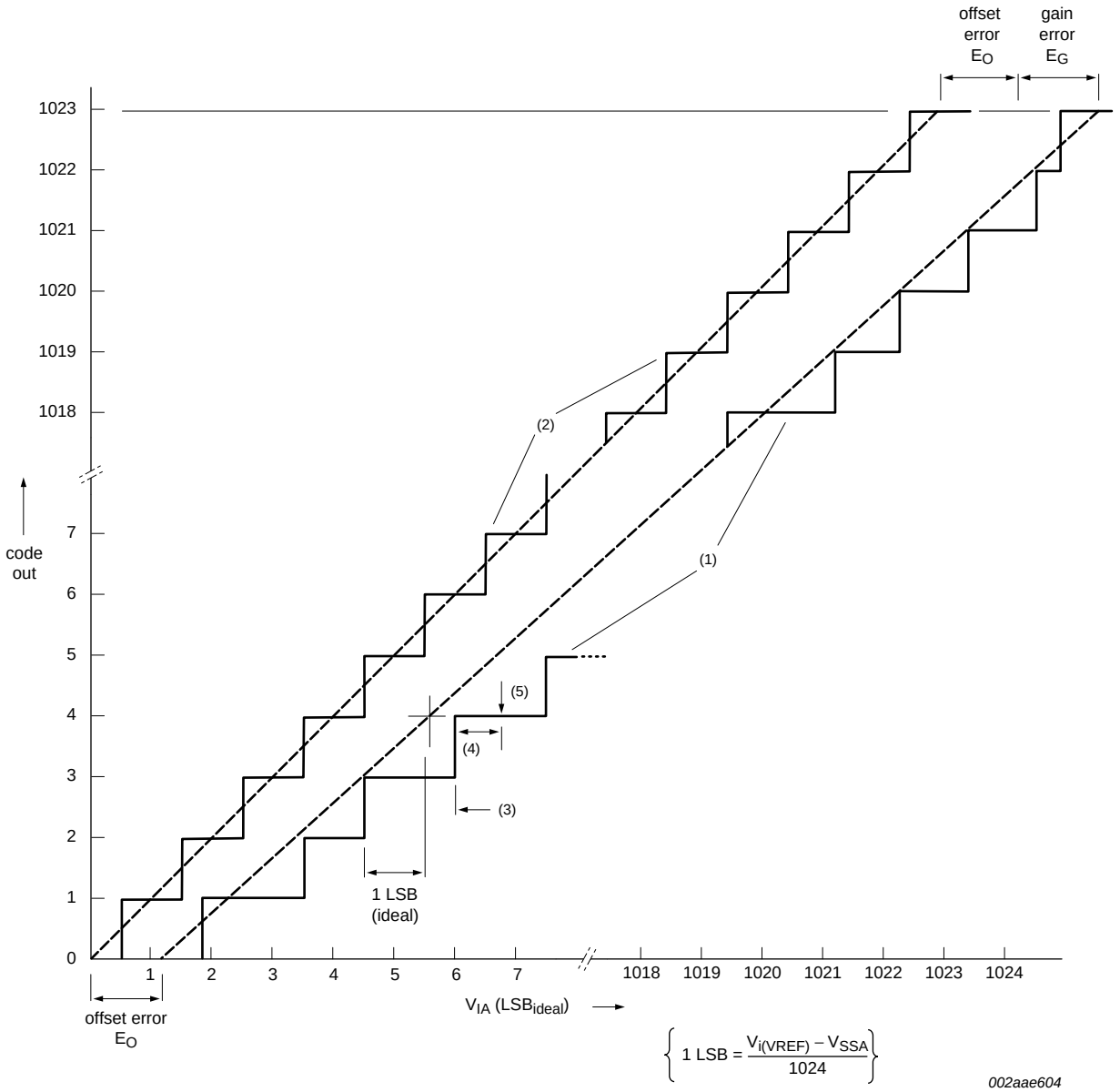
T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{BATpd}	Power-down mode battery supply current	RTC clock = 32 kHz (from RTCXn pins); T_{amb} = 25 °C					
		V_{DD} = 3.0 V; $V_{i(VBAT)}$ = 2.5 V	[11]	-	14	-	μA
		V_{DD} = 3.0 V; $V_{i(VBAT)}$ = 3.0 V		-	16	-	μA
		V_{DD} = 3.3 V; $V_{i(VBAT)}$ = 3.3 V		-	18	-	μA
		V_{DD} = 3.6 V; $V_{i(VBAT)}$ = 3.6 V		-	20	-	μA
I_{BATact}	active mode battery supply current	CCLK = 60 MHz; PCLK = 15 MHz; PCLK enabled to RTCK; RTC clock = 32 kHz (from RTCXn pins); T_{amb} = 25 °C	[11]				
		V_{DD} = 3.0 V; $V_{i(VBAT)}$ = 3.0 V		-	78	-	μA
		V_{DD} = 3.3 V; $V_{i(VBAT)}$ = 3.3 V		-	80	-	μA
		V_{DD} = 3.6 V; $V_{i(VBAT)}$ = 3.6 V		-	82	-	μA
$I_{BATact(opt)}$	optimized active mode battery supply current	PCLK disabled to RTCK in the PCONP register; RTC clock = 32 kHz (from RTCXn pins); T_{amb} = 25 °C; $V_{i(VBAT)}$ = 3.3 V	[11][12]				
		CCLK = 6 MHz		-	21	-	μA
		CCLK = 25 MHz		-	23	-	μA
		CCLK = 50 MHz		-	27	-	μA
		CCLK = 60 MHz		-	30	-	μA
I^2C-bus pins							
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	$0.05V_{DD}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA	[7]	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD}$	[13]	-	2	4	μA
		V_I = 5 V	[13]	-	10	22	μA
Oscillator pins							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			−0.5	1.8	1.95	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			−0.5	1.8	1.95	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1			−0.5	1.8	1.95	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2			−0.5	1.8	1.95	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[3] Including voltage on outputs in 3-state mode.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 11. ADC characteristics

11. DAC electrical characteristics

Table 9. DAC electrical characteristics

V_{DDA} = 3.0 V to 3.6 V; T_{amb} = –40 °C to +85 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
E_D	differential linearity error		-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity		-	±1.5	-	LSB
E_O	offset error		-	0.6	-	%
E_G	gain error		-	0.6	-	%
C_L	load capacitance		-	200	-	pF
R_L	load resistance		1	-	-	kΩ

14. Abbreviations

Table 13. Acronym list

Acronym	Description
A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DCC	Debug Communications Channel
ETM	Embedded Trace Macrocell
FIFO	First In, First Out
GPIO	General Purpose Input/Output
JTAG	Joint Test Action Group
LSB	Least Significant Bit
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulator
RAM	Random Access Memory
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSP	Synchronous Serial Port
UART	Universal Asynchronous Receiver/Transmitter

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2131_32_34_36_38 v.5.1	20110729	Product data sheet	-	LPC2131_32_34_36_38 v.5
Modifications:	• Parameter I_{sink} added in Table 5 “Limiting values”. • Table 6 “Static characteristics”: Updated crystal oscillator specs			
LPC2131_32_34_36_38 v.5	20110202	Product data sheet	-	LPC2131_32_34_36_38 v.4
Modifications:	• Table 3 “Pin description”: Added Table note [9] to RTCX1 and RTCX2 pins. • Table 6 “Static characteristics”, I^2C-bus pins: Changed typical hysteresis voltage from $0.5V_{DD}$ to $0.05V_{DD}$. • Table 6 “Static characteristics”: Removed table note for V_{IH} and V_{IL}. • Changed all occurrences of VPB to APB. • Table 6 “Static characteristics”: Added Table note [6] to V_I. • Table 6 “Static characteristics”, Standard port pins, $\overline{\text{RESET}}$, RTCK: V_{hys} hysteresis voltage (0.4 V) moved from typical to minimum. • Table 6 “Static characteristics”: Changed $V_{i(VREF)}$ minimum voltage from 3.0 V to 2.5 V. • Table 6 “Static characteristics”: Updated min, typical and max values for oscillator pins $V_{i(XTAL1)}$, $V_{o(XTAL2)}$, $V_{i(RTCX1)}$, and $V_{o(RTCX2)}$. • Added Section 11 “DAC electrical characteristics”. • Added Section 12 “Application information”.			
LPC2131_32_34_36_38 v.4	20071016	Product data sheet	-	LPC2131_32_34_36_38 v.3
LPC2131_32_34_36_38 v.3	20060921	Product data sheet	-	LPC2131_32_34_36_38 v.2
LPC2131_32_34_36_38 v.2	20050318	Preliminary data sheet	-	LPC2131_2132_2138 v.1
LPC2131_2132_2138 v.1	20041118	Preliminary data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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