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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	I ² C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	47
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2132fbd64-01-15

- One (LPC2131/32) or two (LPC2134/36/38) 8-channel 10-bit ADCs provide a total of up to 16 analog inputs, with conversion times as low as 2.44 μ s per channel.
- Single 10-bit DAC provides variable analog output (LPC2132/34/36/38).
- Two 32-bit timers/external event counters (with four capture and four compare channels each), PWM unit (six outputs) and watchdog.
- Low power Real-time clock with independent power and dedicated 32 kHz clock input.
- Multiple serial interfaces including two UARTs (16C550), two Fast I²C-bus (400 kbit/s), SPI and SSP with buffering and variable data length capabilities.
- Vectored interrupt controller with configurable priorities and vector addresses.
- Up to forty-seven 5 V tolerant general purpose I/O pins in tiny LQFP64 or HVQFN package.
- Up to nine edge or level sensitive external interrupt pins available.
- 60 MHz maximum CPU clock available from programmable on-chip PLL with settling time of 100 μ s.
- On-chip integrated oscillator operates with external crystal in range of 1 MHz to 30 MHz and with external oscillator up to 50 MHz.
- Power saving modes include Idle and Power-down.
- Individual enable/disable of peripheral functions as well as peripheral clock scaling down for additional power optimization.
- Processor wake-up from Power-down mode via external interrupt or BOD.
- Single power supply chip with POR and BOD circuits:
 - ◆ CPU operating voltage range of 3.0 V to 3.6 V (3.3 V \pm 10 %) with 5 V tolerant I/O pads.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2131FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2132FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2132FHN64/01	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-2
LPC2134FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2136FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2138FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2138FHN64/01	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-2

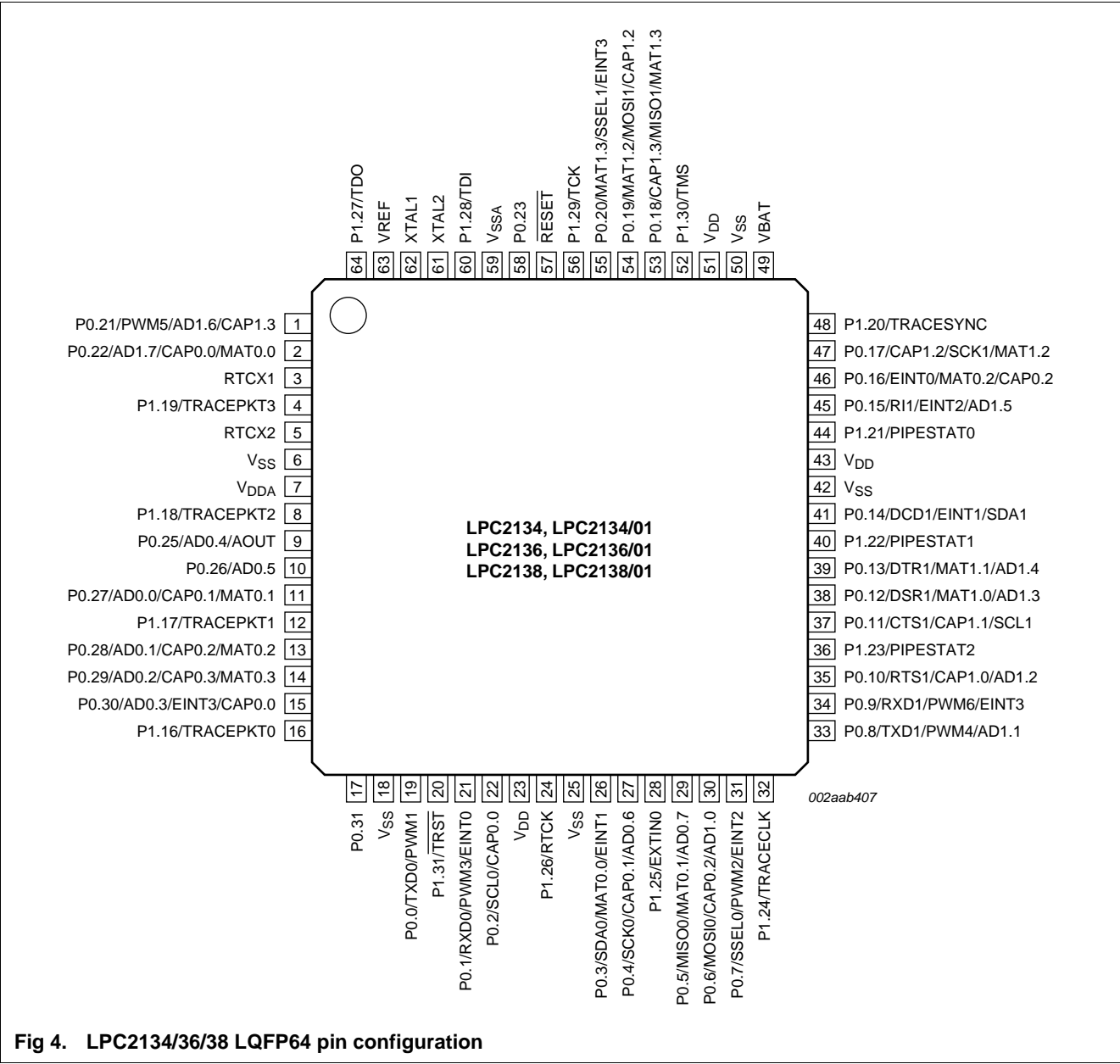
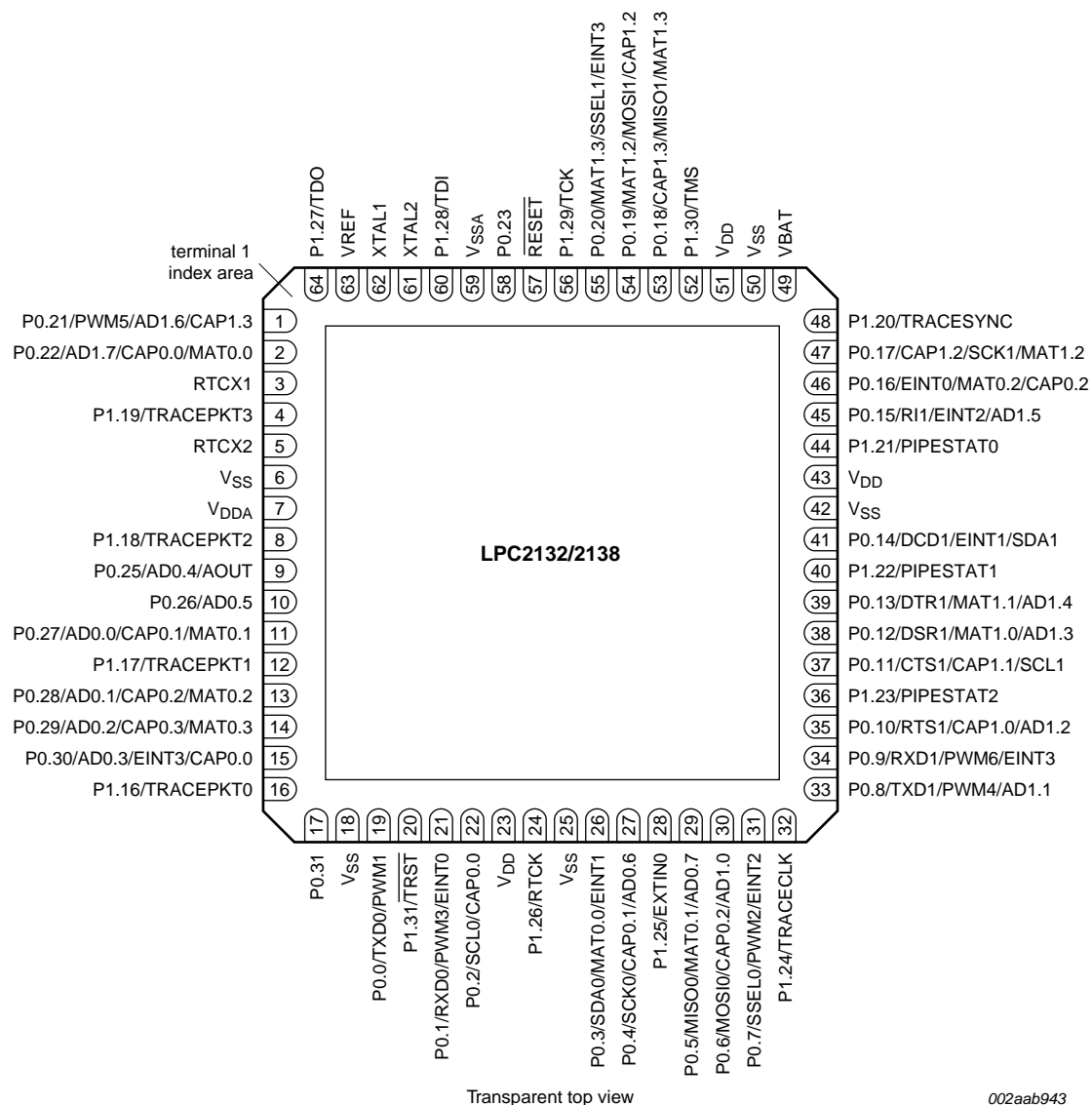


Fig 4. LPC2134/36/38 LQFP64 pin configuration



AD1.7 to AD1.0 only available on LPC2134/36/38.

Fig 5. LPC2132/38 HVQFN64 pin configuration

Table 3. Pin description ...continued

Symbol	Pin	Type	Description
P0.11/CTS1/ CAP1.1/SCL1	37 ^[3]	I	CTS1 — Clear to Send input for UART1. Available in LPC2134/36/38.
		I	CAP1.1 — Capture input for Timer 1, channel 1.
		I/O	SCL1 — I ² C1 clock input/output. Open drain output (for I ² C-bus compliance)
P0.12/DSR1/ MAT1.0/AD1.3	38 ^[4]	I	DSR1 — Data Set Ready input for UART1. Available in LPC2134/36/38.
		O	MAT1.0 — Match output for Timer 1, channel 0.
		I	AD1.3 — ADC 1, input 3. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
P0.13/DTR1/ MAT1.1/AD1.4	39 ^[4]	O	DTR1 — Data Terminal Ready output for UART1. Available in LPC2134/36/38.
		O	MAT1.1 — Match output for Timer 1, channel 1.
		I	AD1.4 — ADC 1, input 4. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
P0.14/DCD1/ EINT1/SDA1	41 ^[3]	I	DCD1 — Data Carrier Detect input for UART1. Available in LPC2134/36/38.
		I	EINT1 — External interrupt 1 input.
		I/O	SDA1 — I ² C1 data input/output. Open drain output (for I ² C-bus compliance).
P0.15/RI1/ EINT2/AD1.5	45 ^[4]	I	RI1 — Ring Indicator input for UART1. Available in LPC2134/36/38.
		I	EINT2 — External interrupt 2 input.
		I	AD1.5 — ADC 1, input 5. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
P0.16/EINT0/ MAT0.2/CAP0.2	46 ^[2]	I	EINT0 — External interrupt 0 input.
		O	MAT0.2 — Match output for Timer 0, channel 2.
		I	CAP0.2 — Capture input for Timer 0, channel 2.
P0.17/CAP1.2/ SCK1/MAT1.2	47 ^[1]	I	CAP1.2 — Capture input for Timer 1, channel 2.
		I/O	SCK1 — Serial Clock for SSP. Clock output from master or input to slave.
		O	MAT1.2 — Match output for Timer 1, channel 2.
P0.18/CAP1.3/ MISO1/MAT1.3	53 ^[1]	I	CAP1.3 — Capture input for Timer 1, channel 3.
		I/O	MISO1 — Master In Slave Out for SSP. Data input to SPI master or data output from SSP slave.
		O	MAT1.3 — Match output for Timer 1, channel 3.
P0.19/MAT1.2/ MOSI1/CAP1.2	54 ^[1]	O	MAT1.2 — Match output for Timer 1, channel 2.
		I/O	MOSI1 — Master Out Slave In for SSP. Data output from SSP master or data input to SSP slave.
		I	CAP1.2 — Capture input for Timer 1, channel 2.
P0.20/MAT1.3/ SSEL1/EINT3	55 ^[2]	O	MAT1.3 — Match output for Timer 1, channel 3.
		I	SSEL1 — Slave Select for SSP. Selects the SSP interface as a slave.
		I	EINT3 — External interrupt 3 input.
P0.21/PWM5/ AD1.6/CAP1.3	1 ^[4]	O	PWM5 — Pulse Width Modulator output 5.
		I	AD1.6 — ADC 1, input 6. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
		I	CAP1.3 — Capture input for Timer 1, channel 3.
P0.22/AD1.7/ CAP0.0/MAT0.0	2 ^[4]	I	AD1.7 — ADC 1, input 7. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
		I	CAP0.0 — Capture input for Timer 0, channel 0.
		O	MAT0.0 — Match output for Timer 0, channel 0.

6.4 Memory map

The LPC2131/32/34/36/38 memory map incorporates several distinct regions, as shown in Figure 6.

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in Section 6.18 “System control”.

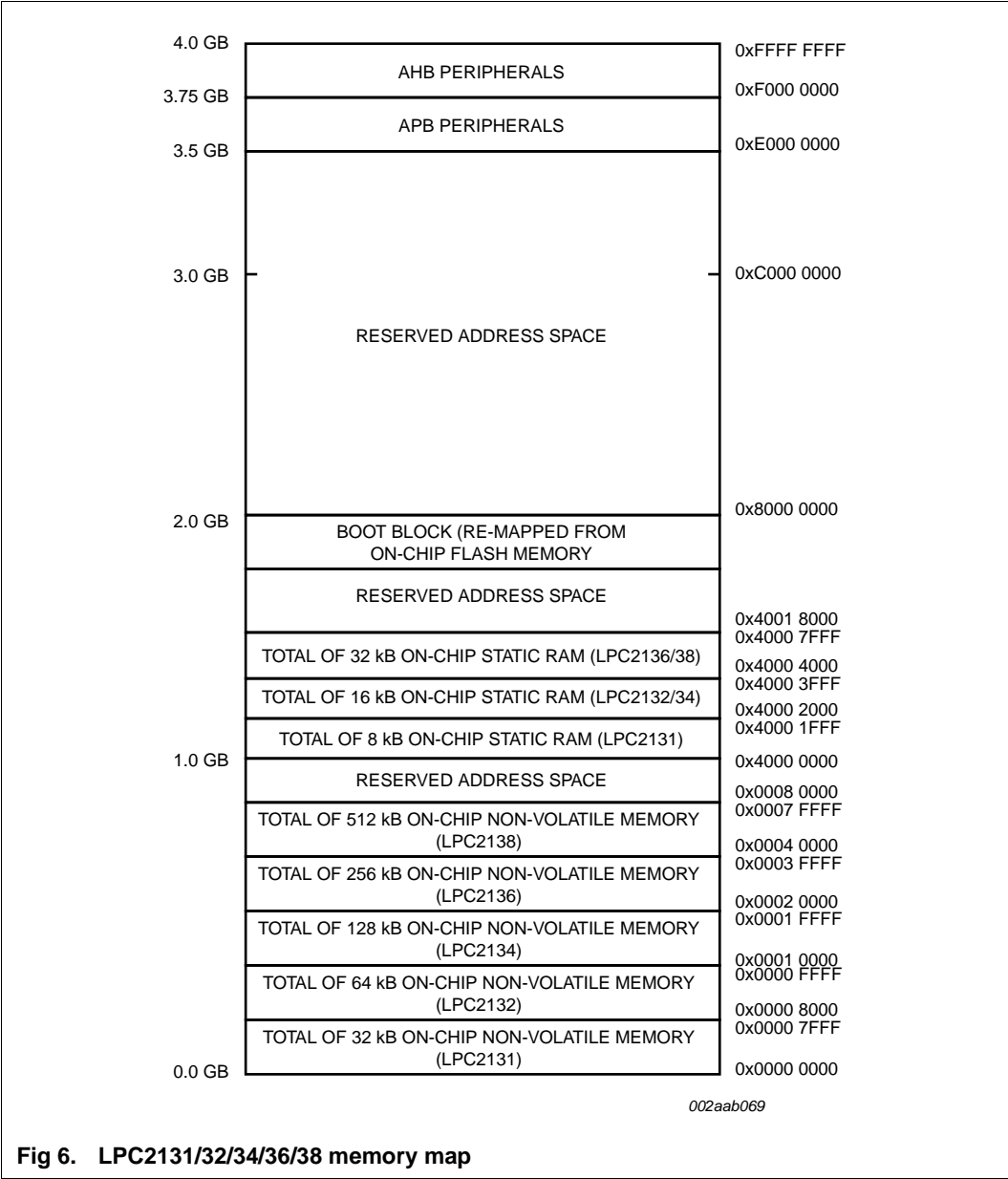


Fig 6. LPC2131/32/34/36/38 memory map

6.5 Interrupt controller

The Vectored Interrupt Controller (VIC) accepts all of the interrupt request inputs and categorizes them as Fast Interrupt reQuest (FIQ), vectored Interrupt ReQuest (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are requesting, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.5.1 Interrupt sources

Table 4 lists the interrupt sources for each peripheral function. Each peripheral device has one interrupt line connected to the Vectored Interrupt Controller, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Table 4. Interrupt sources

Block	Flag(s)	VIC channel #
WDT	Watchdog Interrupt (WDINT)	0
-	Reserved for software interrupts only	1
ARM Core	EmbeddedICE, DbgCommRX	2
ARM Core	EmbeddedICE, DbgCommTX	3
TIMER0	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	4
TIMER1	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	5
UART0	RX Line Status (RLS) Transmit Holding Register empty (THRE) RX Data Available (RDA) Character Time-out Indicator (CTI)	6

Table 4. Interrupt sources ...continued

Block	Flag(s)	VIC channel #
UART1	RX Line Status (RLS)	7
	Transmit Holding Register empty (THRE)	
	RX Data Available (RDA)	
	Character Time-out Indicator (CTI)	
	Modem Status Interrupt (MSI) (Available in LPC2134/36/38 only)	
PWM0	Match 0 to 6 (MR0, MR1, MR2, MR3, MR4, MR5, MR6)	8
	Capture 0 to 3 (CR0, CR1, CR2, CR3)	
I ² C0	SI (state change)	9
SPI0	SPIF, MODF	10
SSP	TX FIFO at least half empty (TXRIS)	11
	RX FIFO at least half full (RXRIS)	
	Receive Timeout (RTRIS)	
	Receive Overrun (RORRIS)	
PLL	PLL Lock (PLOCK)	12
RTC	RTCCIF (Counter Increment), RTCALF (Alarm)	13
System Control	External Interrupt 0 (EINT0)	14
	External Interrupt 1 (EINT1)	15
	External Interrupt 2 (EINT2)	16
	External Interrupt 3 (EINT3)	17
AD0	ADC 0	18
I ² C1	SI (state change)	19
BOD	Brown Out Detect	20
AD1	ADC 1 (Available in LPC2134/36/38 only)	21

6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

6.7 General purpose parallel I/O and Fast I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

6.7.1 Features

- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.12.1 Features

- Compliant with Serial Peripheral Interface (SPI) specification.
- Synchronous, Serial, Full Duplex, Communication.
- Combined SPI master and slave.
- Maximum data bit rate of one eighth of the input clock rate.

6.13 SSP serial I/O controller

The LPC2131/32/34/36/38 each contain one Serial Synchronous Port controller (SSP). The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. However, only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. Often only one of these data flows carries meaningful data.

6.13.1 Features

- Compatible with Motorola SPI, 4-wire TI SSI and National Semiconductor Microwire buses.
- Synchronous Serial Communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- Four bits to 16 bits per frame.

6.14 General purpose timers/external event counters

The Timer/Counter is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock, and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with 'or' and 'and', as well as 'broadcast' functions among them.

At any given time only one of peripheral's capture inputs can be selected as an external event signal source, i.e., timer's clock. The rate of external events that can be successfully counted is limited to PCLK/2. In this configuration, unused capture lines can be selected as regular timer capture inputs.

6.14.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.
- External Event Counter or timer operation.
- Four 32-bit capture channels per timer/counter that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
 - Continuous operation with optional interrupt generation on match.

6.17 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2131/32/34/36/38. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.17.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
 - Continuous operation with optional interrupt generation on match.
 - Stop timer on match with optional interrupt generation.
 - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.

- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must 'release' new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.

6.18 System control

6.18.1 Crystal oscillator

On-chip integrated oscillator operates with external crystal in range of 1 MHz to 30 MHz and with external oscillator up to 50 MHz. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to [Section 6.18.2 "PLL"](#) for additional information.

6.18.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μ s.

6.18.3 Reset and wake-up timer

Reset has two sources on the LPC2131/32/34/36/38: the $\overline{\text{RESET}}$ pin and watchdog reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the wake-up timer (see wake-up timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The wake-up timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up timer.

The wake-up timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

6.18.4 Brownout detector

The LPC2131/32/34/36/38 include 2-stage monitoring of the voltage on the V_{DD} pins. If this voltage falls below 2.9 V, the BOD asserts an interrupt signal to the Vectored Interrupt Controller. This signal can be enabled for interrupt; if not, software can monitor the signal by reading dedicated register.

The second stage of low-voltage detection asserts reset to inactivate the LPC2131/32/34/36/38 when the voltage on the V_{DD} pins falls below 2.6 V. This reset prevents alteration of the flash as operation of the various elements of the chip would otherwise become unreliable due to low voltage. The BOD circuit maintains this reset down below 1 V, at which point the POR circuitry maintains the overall reset.

Both the 2.9 V and 2.6 V thresholds include some hysteresis. In normal operation, this hysteresis allows the 2.9 V detection to reliably interrupt, or a regularly-executed event loop to sense the condition.

Features available only in LPC213x/01 parts include ability to put the BOD in power-down mode, turn it on or off and to control when the BOD will reset the LPC213x/01 microcontroller. This can be used to further reduce power consumption when a low power mode (such as Power Down) is invoked.

6.18.5 Code security

This feature of the LPC2131/32/34/36/38 allow an application to control whether it can be debugged or protected from observation.

If after reset on-chip bootloader detects a valid checksum in flash and reads 0x8765 4321 from address 0x1FC in flash, debugging will be disabled and thus the code in flash will be protected from observation. Once debugging is disabled, it can be enabled only by performing a full chip erase using the ISP.

6.18.6 External interrupt inputs

The LPC2131/32/34/36/38 include up to nine edge or level sensitive External Interrupt Inputs as selectable pin functions. When the pins are combined, external events can be processed as four independent interrupt signals. The External Interrupt Inputs can optionally be used to wake up the processor from Power-down mode.

6.18.7 Memory Mapping Control

The Memory Mapping Control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The debug communication channel is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

6.19.2 Embedded trace

Since the LPC2131/32/34/36/38 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code can not be traced because of this restriction.

6.19.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC, which is present in the EmbeddedICE logic. The LPC2131/32/34/36/38 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

8. Static characteristics

Table 6. Static characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)		3.0	3.3	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage		2.5	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT		^[2] 2.0	3.3	3.6	V
$V_{i(VREF)}$	input voltage on pin VREF		2.5	3.3	3.6	V
Standard port pins, RESET, P1.26/RTCK						
I_{IL}	LOW-level input current	$V_I = 0\text{ V}$; no pull-up	-	-	3	μA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; no pull-down	-	-	3	μA
I_{OZ}	OFF-state output current	$V_O = 0\text{ V}$; $V_O = V_{DD}$; no pull-up/down	-	-	3	μA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125\text{ }^{\circ}\text{C}$	-	-	100	mA
V_I	input voltage	pin configured to provide a digital function	^{[3][4][5][6]} 0	-	5.5	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{hys}	hysteresis voltage		0.4	-	-	V
V_{OH}	HIGH-level output voltage	$I_{OH} = -4\text{ mA}$	^[7] $V_{DD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$I_{OL} = -4\text{ mA}$	^[7] -	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4\text{ V}$	^[7] -4	-	-	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.4\text{ V}$	^[7] 4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	$V_{OH} = 0\text{ V}$	^[8] -	-	-45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DDA}$	^[8] -	-	50	mA
I_{pd}	pull-down current	$V_I = 5\text{ V}$	^[9] 10	50	150	μA
I_{pu}	pull-up current	$V_I = 0\text{ V}$	^[10] -15	-50	-85	μA
		$V_{DD} < V_I < 5\text{ V}$	^[9] 0	0	0	μA
$I_{DD(act)}$	active mode supply current	$V_{DD} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; code				
		<code>while(1){}</code>				
		executed from flash, no active peripherals				
		CCLK = 10 MHz	-	10	-	mA
$I_{DD(pd)}$	Power-down mode supply current	$V_{DD} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	-	60	-	μA
		$V_{DD} = 3.3\text{ V}$; $T_{amb} = 85\text{ }^{\circ}\text{C}$	-	200	500	μA

- [4] V_{DD} supply voltages must be present.
- [5] 3-state outputs go into 3-state mode when V_{DD} is grounded.
- [6] Please also see the errata note mentioned in the errata sheet.
- [7] Accounts for 100 mV voltage drop in all supply lines.
- [8] Only allowed for a short time period.
- [9] Minimum condition for $V_I = 4.5$ V, maximum condition for $V_I = 5.5$ V.
- [10] Applies to P1.16 to P1.25.
- [11] On pin VBAT.
- [12] Optimized for low battery consumption.
- [13] To V_{SS} .

9. Dynamic characteristics

Table 7. Dynamic characteristics

$T_{amb} = -40$ °C to $+85$ °C for commercial applications, V_{DD} over specified ranges.^[1]

Symbol	Parameter	Conditions	Min	Typ ^[2]	Max	Unit
External clock						
f_{osc}	oscillator frequency		10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	100	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0.2 and P0.3)						
$t_{r(o)}$	output rise time		-	10	-	ns
$t_{f(o)}$	output fall time		-	10	-	ns
I²C-bus pins (P0.2 and P0.3)						
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$ ^[3]	-	-	ns

- [1] Parameters are valid over operating temperature range unless otherwise specified.
- [2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.
- [3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

9.1 Timing

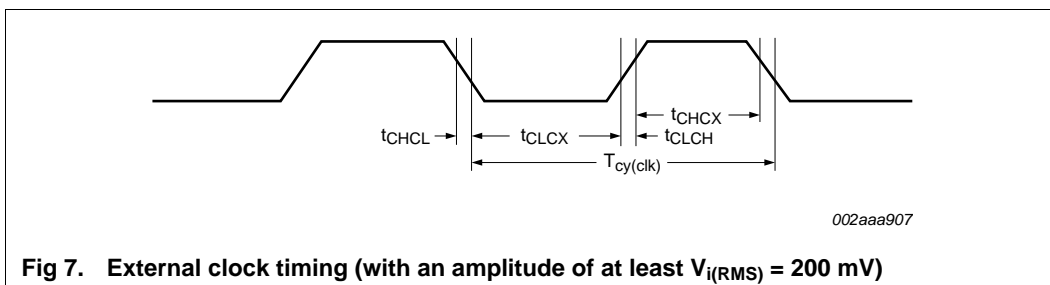
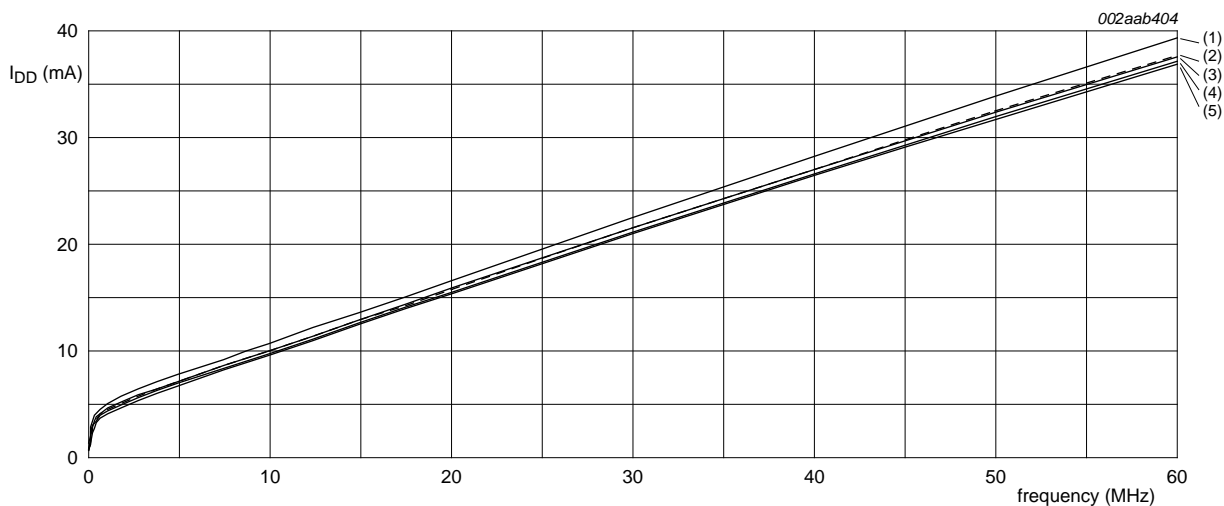


Fig 7. External clock timing (with an amplitude of at least $V_{I(RMS)} = 200$ mV)

9.2 LPC2138 power consumption measurements



Test conditions: code executed from flash; all peripherals are enabled in PCONP register; PCLK = CCLK/4.

- (1) $V_{DD} = 3.6$ V at -60 °C (max)
- (2) $V_{DD} = 3.6$ V at 140 °C
- (3) $V_{DD} = 3.6$ V at 25 °C
- (4) $V_{DD} = 3.3$ V at 25 °C (typical)
- (5) $V_{DD} = 3.3$ V at 95 °C (typical)

Fig 8. $I_{DD(Act)}$ measured at different frequencies (CCLK) and temperatures

10. ADC electrical characteristics

Table 8. ADC static characteristics

$V_{DDA} = 2.5\text{ V to }3.6\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ unless otherwise specified; ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DDA}	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2][3]	-	-	± 1	LSB
$E_{L(adj)}$	integral non-linearity	[1][4]	-	-	± 2	LSB
E_O	offset error	[1][5]	-	-	± 3	LSB
E_G	gain error	[1][6]	-	-	± 0.5	%
E_T	absolute error	[1][7]	-	-	± 4	LSB
R_{vsi}	voltage source interface resistance	[8]	-	-	40	k Ω

[1] Conditions: $V_{SSA} = 0\text{ V}$, $V_{DDA} = 3.3\text{ V}$.

[2] The ADC is monotonic, there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See [Figure 11](#).

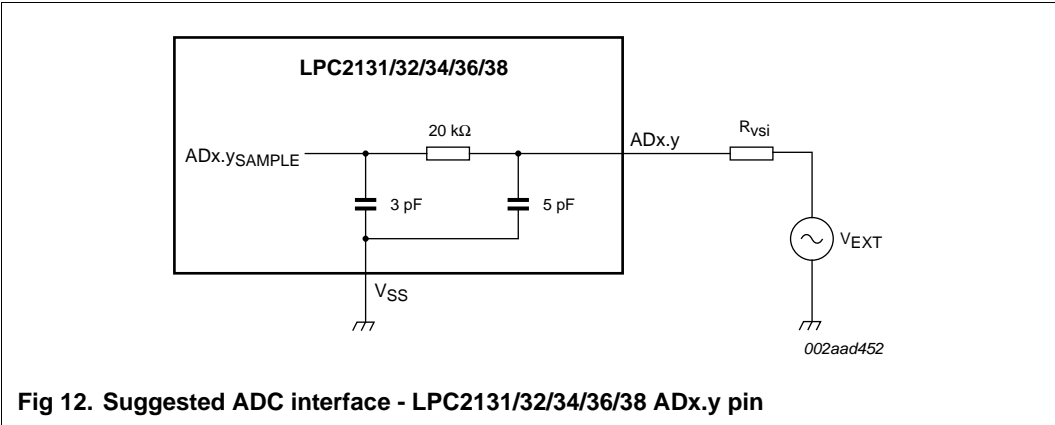
[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See [Figure 11](#).

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See [Figure 11](#).

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See [Figure 11](#).

[7] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See [Figure 11](#).

[8] See [Figure 11](#).

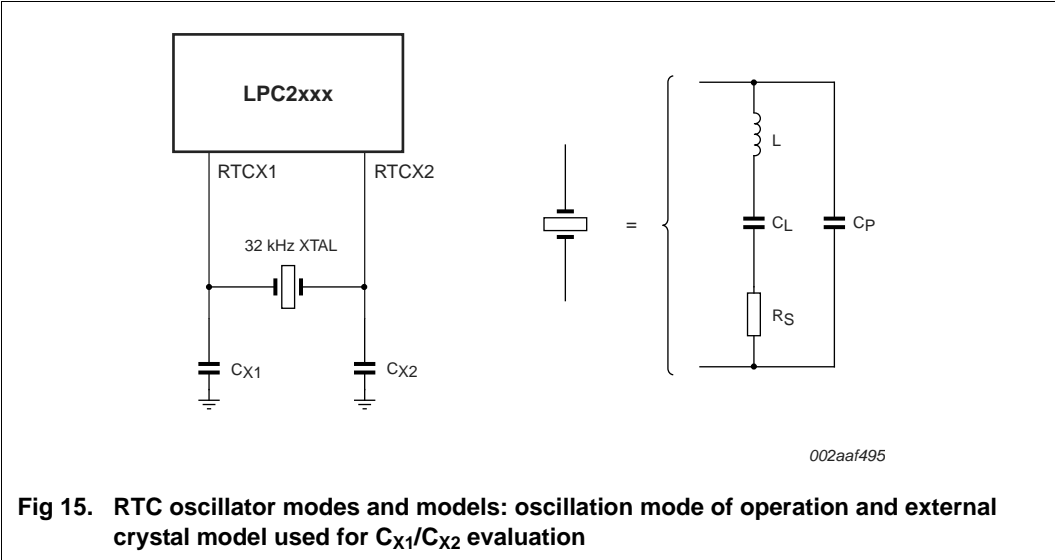


11. DAC electrical characteristics

Table 9. DAC electrical characteristics*V_{DDA} = 3.0 V to 3.6 V; T_{amb} = -40 °C to +85 °C unless otherwise specified*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
E _D	differential linearity error		-	±1	-	LSB
E _{L(adj)}	integral non-linearity		-	±1.5	-	LSB
E _O	offset error		-	0.6	-	%
E _G	gain error		-	0.6	-	%
C _L	load capacitance		-	200	-	pF
R _L	load resistance		1	-	-	kΩ

12.2 RTC 32 kHz oscillator component selection



The RTC external oscillator circuit is shown in [Figure 15](#). Since the feedback resistance is integrated on chip, only a crystal, the capacitances C_{X1} and C_{X2} need to be connected externally to the microcontroller.

[Table 12](#) gives the crystal parameters that should be used. C_L is the typical load capacitance of the crystal and is usually specified by the crystal manufacturer. The actual C_L influences oscillation frequency. When using a crystal that is manufactured for a different load capacitance, the circuit will oscillate at a slightly different frequency (depending on the quality of the crystal) compared to the specified one. Therefore for an accurate time reference it is advised to use the load capacitors as specified in [Table 12](#) that belong to a specific C_L . The value of external capacitances C_{X1} and C_{X2} specified in this table are calculated from the internal parasitic capacitances and the C_L . Parasitics from PCB and package are not taken into account.

Table 12. Recommended values for the RTC external 32 kHz oscillator C_{X1}/C_{X2} components

Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
11 pF	< 100 k Ω	18 pF, 18 pF
13 pF	< 100 k Ω	22 pF, 22 pF
15 pF	< 100 k Ω	27 pF, 27 pF

12.3 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{X1} , C_{X2} , and C_{X3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plane. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{X1} and C_{X2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

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