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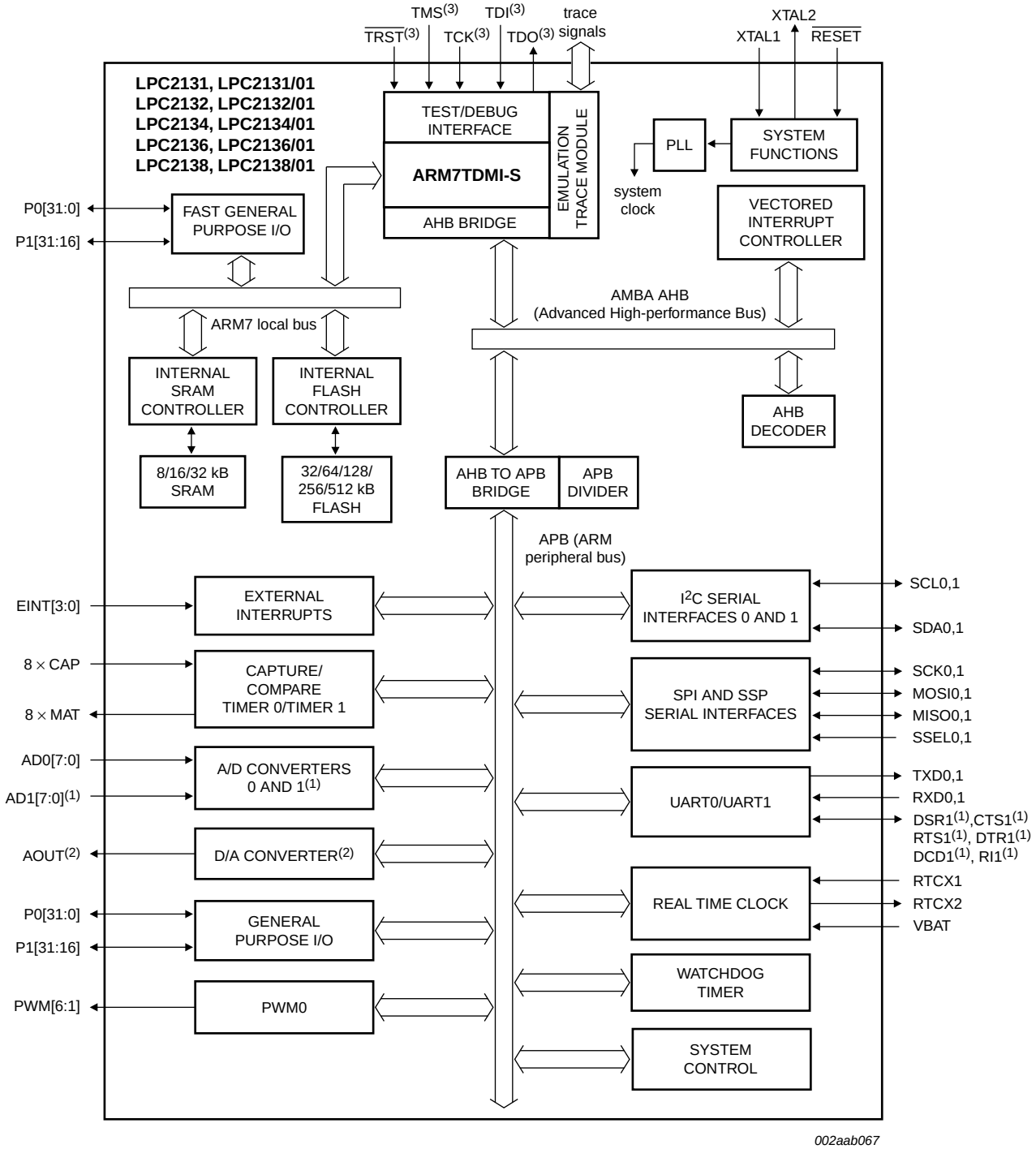
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	47
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2134fbd64-151

4. Block diagram



(1) LPC2134/36/38 only.

(2) LPC2132/34/36/38 only.

(3) Pins shared with GPIO.

Fig 1. Block diagram

5. Pinning information

5.1 Pinning

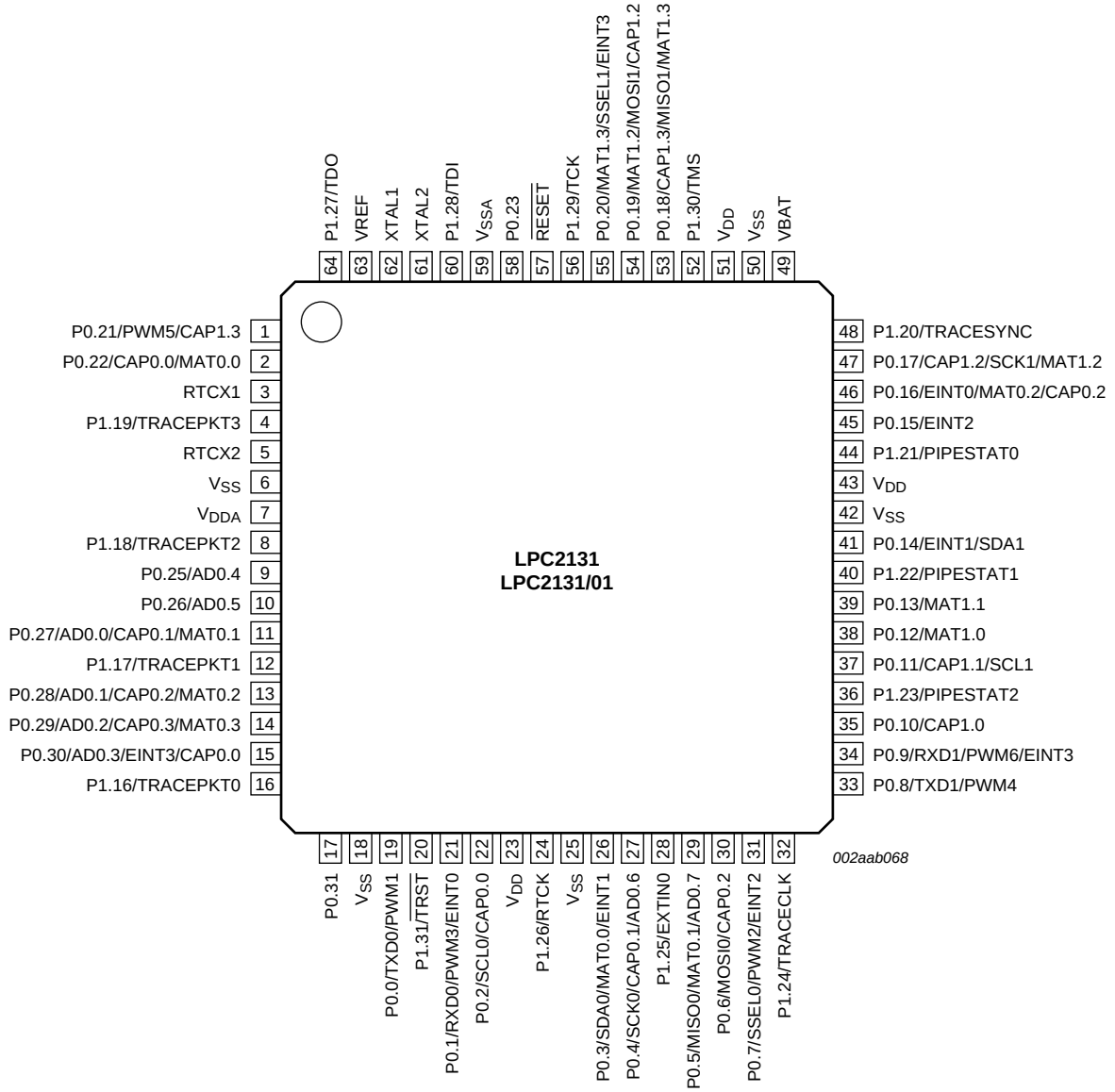


Fig 2. LPC2131 LQFP64 pin configuration

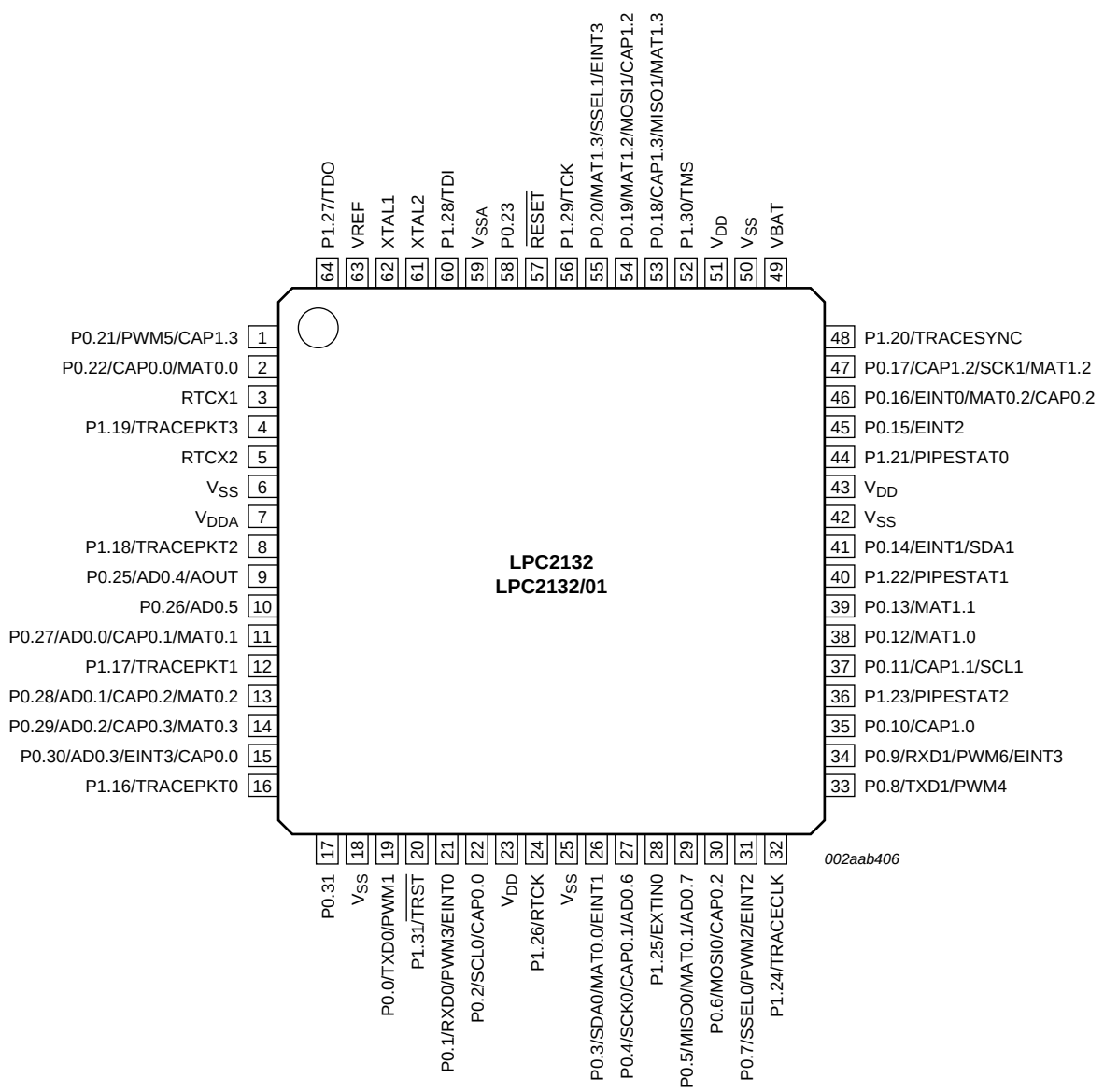


Fig 3. LPC2132 LQFP64 pin configuration

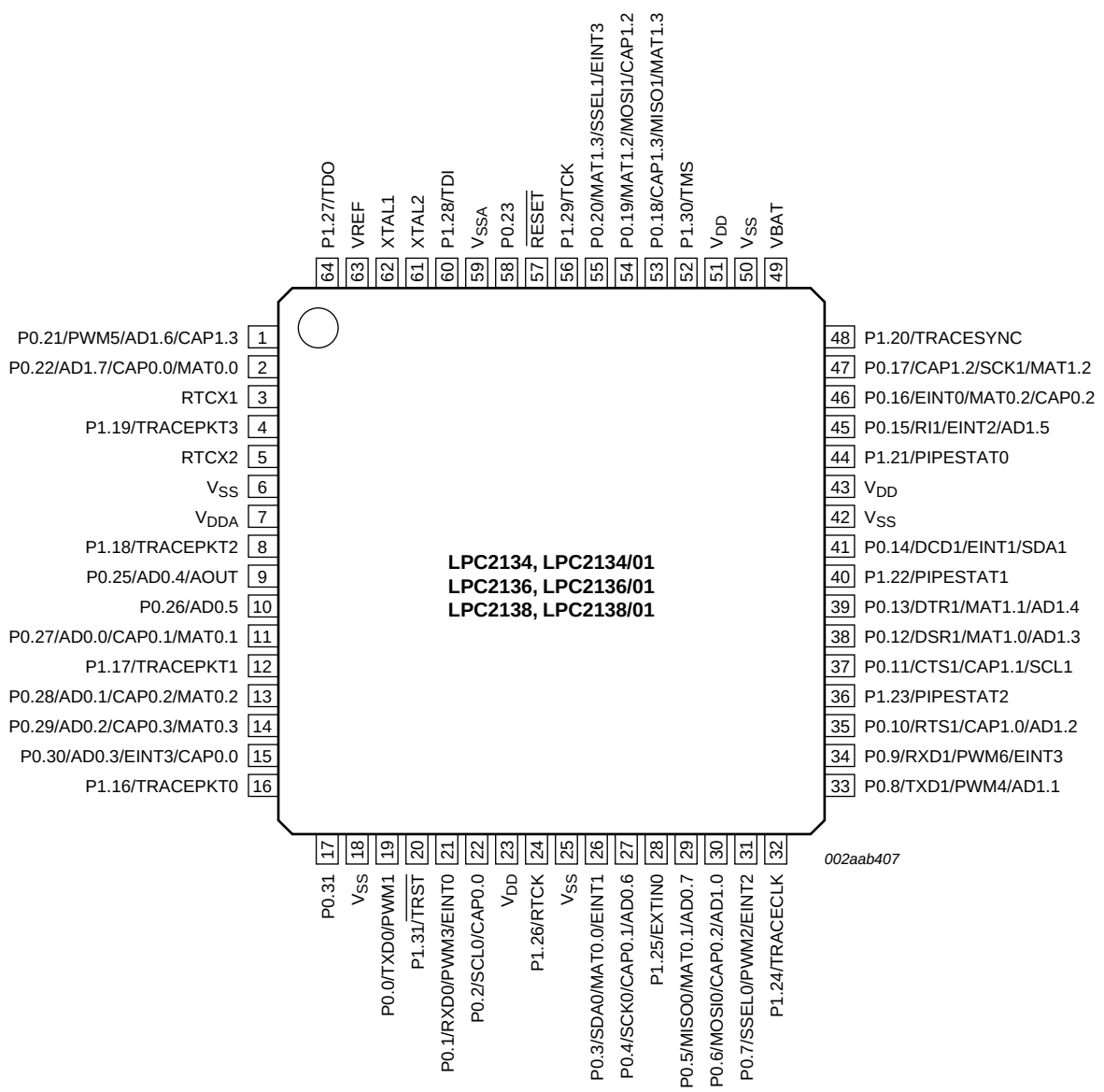


Fig 4. LPC2134/36/38 LQFP64 pin configuration

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
P0.0 to P0.31		I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. Total of 31 pins of the Port 0 can be used as a general purpose bidirectional digital I/Os while P0.31 is output only pin. The operation of port 0 pins depends upon the pin function selected via the pin connect block. Pin P0.24 is not available.
P0.0/TXD0/ PWM1	19[1]	O	**TXD0 —** Transmitter output for UART0.
		O	**PWM1 —** Pulse Width Modulator output 1.
P0.1/RXD0/ PWM3/EINT0	21[2]	I	**RXD0 —** Receiver input for UART0.
		O	**PWM3 —** Pulse Width Modulator output 3.
		I	**EINT0 —** External interrupt 0 input.
P0.2/SCL0/ CAP0.0	22[3]	I/O	**SCL0 —** I^2C0 clock input/output. Open drain output (for I^2C-bus compliance).
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.3/SDA0/ MAT0.0/EINT1	26[3]	I/O	**SDA0 —** I^2C0 data input/output. Open drain output (for I^2C-bus compliance).
		O	**MAT0.0 —** Match output for Timer 0, channel 0.
		I	**EINT1 —** External interrupt 1 input.
P0.4/SCK0/ CAP0.1/AD0.6	27[4]	I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
		I	**CAP0.1 —** Capture input for Timer 0, channel 1.
		I	**AD0.6 —** ADC 0, input 6. This analog input is always connected to its pin.
P0.5/MISO0/ MAT0.1/AD0.7	29[4]	I/O	**MISO0 —** Master In Slave V_{DD} = 3.6 V for SPI0. Data input to SPI master or data output from SPI slave.
		O	**MAT0.1 —** Match output for Timer 0, channel 1.
		I	**AD0.7 —** ADC 0, input 7. This analog input is always connected to its pin.
P0.6/MOSI0/ CAP0.2/AD1.0	30[4]	I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
		I	**AD1.0 —** ADC 1, input 0. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
P0.7/SSEL0/ PWM2/EINT2	31[2]	I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
		O	**PWM2 —** Pulse Width Modulator output 2.
		I	**EINT2 —** External interrupt 2 input.
P0.8/TXD1/ PWM4/AD1.1	33[4]	O	**TXD1 —** Transmitter output for UART1.
		O	**PWM4 —** Pulse Width Modulator output 4.
		I	**AD1.1 —** ADC 1, input 1. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
P0.9/RXD1/ PWM6/EINT3	34[2]	I	**RXD1 —** Receiver input for UART1.
		O	**PWM6 —** Pulse Width Modulator output 6.
		I	**EINT3 —** External interrupt 3 input.
P0.10/RTS1/ CAP1.0/AD1.2	35[4]	O	**RTS1 —** Request to Send output for UART1. Available in LPC2134/36/38.
		I	**CAP1.0 —** Capture input for Timer 1, channel 0.
		I	**AD1.2 —** ADC 1, input 2. This analog input is always connected to its pin. Available in LPC2134/36/38 only.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P0.11/CTS1/ CAP1.1/SCL1	37[3]	I	**CTS1 —** Clear to Send input for UART1. Available in LPC2134/36/38.
		I	**CAP1.1 —** Capture input for Timer 1, channel 1.
		I/O	**SCL1 —** I^2C1 clock input/output. Open drain output (for I^2C-bus compliance)
P0.12/DSR1/ MAT1.0/AD1.3	38[4]	I	**DSR1 —** Data Set Ready input for UART1. Available in LPC2134/36/38.
		O	**MAT1.0 —** Match output for Timer 1, channel 0.
		I	**AD1.3 —** ADC 1, input 3. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
P0.13/DTR1/ MAT1.1/AD1.4	39[4]	O	**DTR1 —** Data Terminal Ready output for UART1. Available in LPC2134/36/38.
		O	**MAT1.1 —** Match output for Timer 1, channel 1.
		I	**AD1.4 —** ADC 1, input 4. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
P0.14/DCD1/ EINT1/SDA1	41[3]	I	**DCD1 —** Data Carrier Detect input for UART1. Available in LPC2134/36/38.
		I	**EINT1 —** External interrupt 1 input.
		I/O	**SDA1 —** I^2C1 data input/output. Open drain output (for I^2C-bus compliance).
P0.15/RI1/ EINT2/AD1.5	45[4]	I	**RI1 —** Ring Indicator input for UART1. Available in LPC2134/36/38.
		I	**EINT2 —** External interrupt 2 input.
		I	**AD1.5 —** ADC 1, input 5. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
P0.16/EINT0/ MAT0.2/CAP0.2	46[2]	I	**EINT0 —** External interrupt 0 input.
		O	**MAT0.2 —** Match output for Timer 0, channel 2.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
P0.17/CAP1.2/ SCK1/MAT1.2	47[1]	I	**CAP1.2 —** Capture input for Timer 1, channel 2.
		I/O	**SCK1 —** Serial Clock for SSP. Clock output from master or input to slave.
		O	**MAT1.2 —** Match output for Timer 1, channel 2.
P0.18/CAP1.3/ MISO1/MAT1.3	53[1]	I	**CAP1.3 —** Capture input for Timer 1, channel 3.
		I/O	**MISO1 —** Master In Slave Out for SSP. Data input to SPI master or data output from SSP slave.
		O	**MAT1.3 —** Match output for Timer 1, channel 3.
P0.19/MAT1.2/ MOSI1/CAP1.2	54[1]	O	**MAT1.2 —** Match output for Timer 1, channel 2.
		I/O	**MOSI1 —** Master Out Slave In for SSP. Data output from SSP master or data input to SSP slave.
		I	**CAP1.2 —** Capture input for Timer 1, channel 2.
P0.20/MAT1.3/ SSEL1/EINT3	55[2]	O	**MAT1.3 —** Match output for Timer 1, channel 3.
		I	**SSEL1 —** Slave Select for SSP. Selects the SSP interface as a slave.
		I	**EINT3 —** External interrupt 3 input.
P0.21/PWM5/ AD1.6/CAP1.3	1[4]	O	**PWM5 —** Pulse Width Modulator output 5.
		I	**AD1.6 —** ADC 1, input 6. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
		I	**CAP1.3 —** Capture input for Timer 1, channel 3.
P0.22/AD1.7/ CAP0.0/MAT0.0	2[4]	I	**AD1.7 —** ADC 1, input 7. This analog input is always connected to its pin. Available in LPC2134/36/38 only.
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
		O	**MAT0.0 —** Match output for Timer 0, channel 0.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P0.23	58[1]	I/O	General purpose digital input/output pin.
P0.25/AD0.4/ AOUT	9[5]	I	**AD0.4 —** ADC 0, input 4. This analog input is always connected to its pin.
		O	**AOUT —** DAC output. Not available in LPC2131.
P0.26/AD0.5	10[4]	I	**AD0.5 —** ADC 0, input 5. This analog input is always connected to its pin.
P0.27/AD0.0/ CAP0.1/MAT0.1	11[4]	I	**AD0.0 —** ADC 0, input 0. This analog input is always connected to its pin.
		I	**CAP0.1 —** Capture input for Timer 0, channel 1.
		O	**MAT0.1 —** Match output for Timer 0, channel 1.
P0.28/AD0.1/ CAP0.2/MAT0.2	13[4]	I	**AD0.1 —** ADC 0, input 1. This analog input is always connected to its pin.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
		O	**MAT0.2 —** Match output for Timer 0, channel 2.
P0.29/AD0.2/ CAP0.3/MAT0.3	14[4]	I	**AD0.2 —** ADC 0, input 2. This analog input is always connected to its pin.
		I	**CAP0.3 —** Capture input for Timer 0, channel 3.
		O	**MAT0.3 —** Match output for Timer 0, channel 3.
P0.30/AD0.3/ EINT3/CAP0.0	15[4]	I	**AD0.3 —** ADC 0, input 3. This analog input is always connected to its pin.
		I	**EINT3 —** External interrupt 3 input.
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.31	17[6]	O	General purpose digital output only pin. **Important:** This pin MUST NOT be externally pulled LOW when $\overline{\text{RESET}}$ pin is LOW or the JTAG port will be disabled.
P1.0 to P1.31		I/O	**Port 1:** Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the pin connect block. Pins 0 through 15 of port 1 are not available.
P1.16/ TRACEPKT0	16[6]	O	**TRACEPKT0 —** Trace Packet, bit 0. Standard I/O port with internal pull-up.
P1.17/ TRACEPKT1	12[6]	O	**TRACEPKT1 —** Trace Packet, bit 1. Standard I/O port with internal pull-up.
P1.18/ TRACEPKT2	8[6]	O	**TRACEPKT2 —** Trace Packet, bit 2. Standard I/O port with internal pull-up.
P1.19/ TRACEPKT3	4[6]	O	**TRACEPKT3 —** Trace Packet, bit 3. Standard I/O port with internal pull-up.
P1.20/ TRACESYNC	48[6]	O	**TRACESYNC —** Trace Synchronization. Standard I/O port with internal pull-up. LOW on TRACESYNC while $\overline{\text{RESET}}$ is LOW enables pins P1.25:16 to operate as Trace port after reset.
P1.21/ PIPESTAT0	44[6]	O	**PIPESTAT0 —** Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P1.22/ PIPESTAT1	40[6]	O	**PIPESTAT1 —** Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P1.23/ PIPESTAT2	36[6]	O	**PIPESTAT2 —** Pipeline Status, bit 2. Standard I/O port with internal pull-up.
P1.24/ TRACECLK	32[6]	O	**TRACECLK —** Trace Clock. Standard I/O port with internal pull-up.
P1.25/EXTIN0	28[6]	I	**EXTIN0 —** External Trigger Input. Standard I/O with internal pull-up.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P1.26/RTCK	24[6]	I/O	**RTCK —** Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. LOW on RTCK while $\overline{\text{RESET}}$ is LOW enables pins P1.31:26 to operate as Debug port after reset.
P1.27/TDO	64[6]	O	**TDO —** Test Data out for JTAG interface.
P1.28/TDI	60[6]	I	**TDI —** Test Data in for JTAG interface.
P1.29/TCK	56[6]	I	**TCK —** Test Clock for JTAG interface.
P1.30/TMS	52[6]	I	**TMS —** Test Mode Select for JTAG interface.
P1.31/$\overline{\text{TRST}}$	20[6]	I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
$\overline{\text{RESET}}$	57[7]	I	**External reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	62[8]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	61[8]	O	Output from the oscillator amplifier.
RTCX1	3[9]	I	Input to the RTC oscillator circuit.
RTCX2	5[9]	O	Output from the RTC oscillator circuit.
V_{SS}	6, 18, 25, 42, 50	I	**Ground:** 0 V reference.
V_{SSA}	59	I	**Analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
V_{DD}	23, 43, 51	I	**3.3 V power supply:** This is the power supply voltage for the core and I/O ports.
V_{DDA}	7	I	**Analog 3.3 V power supply:** This should be nominally the same voltage as V_{DD} but should be isolated to minimize noise and error. This voltage is used to power the on-chip PLL.
VREF	63	I	**ADC reference:** This should be nominally the same voltage as V_{DD} but should be isolated to minimize noise and error. Level on this pin is used as a reference for A/D and D/A convertor(s).
VBAT	49	I	**RTC power supply:** 3.3 V on this pin supplies the power to the RTC.

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control.

[2] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns.

[3] Open drain 5 V tolerant digital I/O I^2C-bus 400 kHz specification compatible pad. It requires external pull-up to provide an output functionality.

[4] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog input function. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns. When configured as an ADC input, digital section of the pad is disabled.

[5] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog output function. When configured as the DAC output, digital section of the pad is disabled.

[6] 5 V tolerant pad with built-in pull-up resistor providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. The pull-up resistor's value ranges from 60 kΩ to 300 kΩ.

[7] 5 V tolerant pad providing digital input (with TTL levels and hysteresis) function only.

[8] Pad provides special analog functionality.

[9] When unused, the RTCX1 pin can be grounded or left floating. For lowest power leave it floating.
The other RTC pin, RTCX2, should be left floating.

6.4 Memory map

The LPC2131/32/34/36/38 memory map incorporates several distinct regions, as shown in Figure 6.

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in Section 6.18 “System control”.

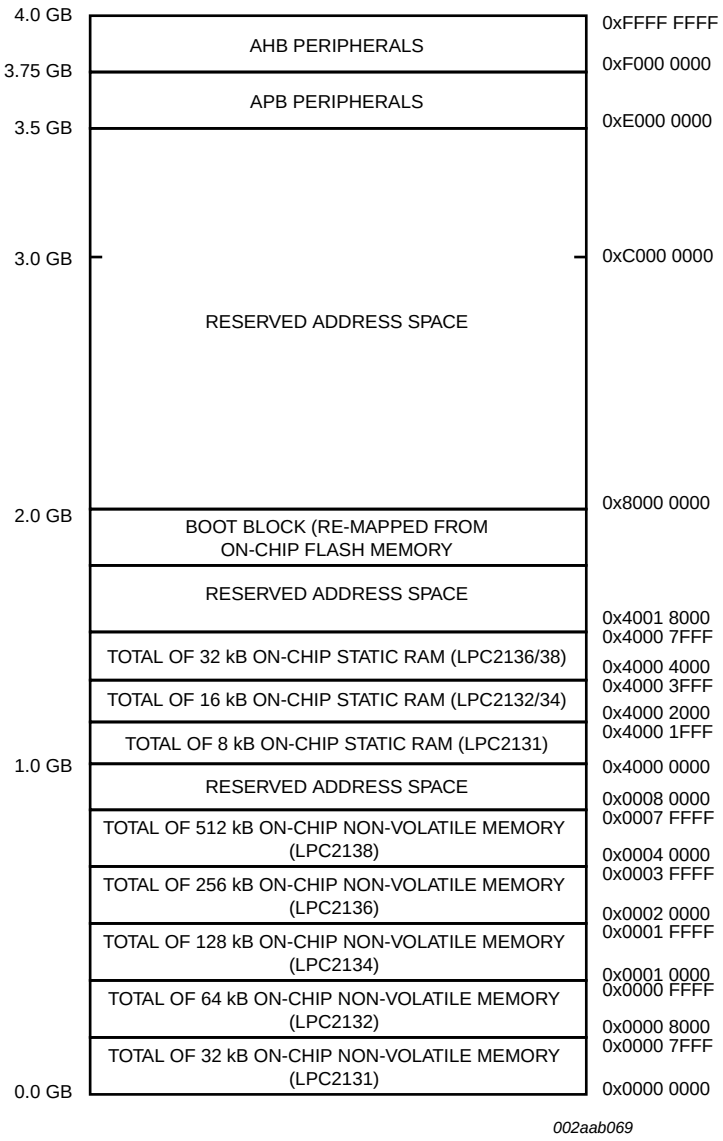


Fig 6. LPC2131/32/34/36/38 memory map

Table 4. Interrupt sources *…continued*

Block	Flag(s)	VIC channel #
UART1	RX Line Status (RLS)	7
	Transmit Holding Register empty (THRE)	
	RX Data Available (RDA)	
	Character Time-out Indicator (CTI)	
	Modem Status Interrupt (MSI) (Available in LPC2134/36/38 only)	
PWM0	Match 0 to 6 (MR0, MR1, MR2, MR3, MR4, MR5, MR6)	8
	Capture 0 to 3 (CR0, CR1, CR2, CR3)	
I^2C0	SI (state change)	9
SPI0	SPIF, MODF	10
SSP	TX FIFO at least half empty (TXRIS)	11
	RX FIFO at least half full (RXRIS)	
	Receive Timeout (RTRIS)	
	Receive Overrun (RORRIS)	
PLL	PLL Lock (PLOCK)	12
RTC	RTCCIF (Counter Increment), RTCALF (Alarm)	13
System Control	External Interrupt 0 (EINT0)	14
	External Interrupt 1 (EINT1)	15
	External Interrupt 2 (EINT2)	16
	External Interrupt 3 (EINT3)	17
AD0	ADC 0	18
I2C1	SI (state change)	19
BOD	Brown Out Detect	20
AD1	ADC 1 (Available in LPC2134/36/38 only)	21

6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

6.7 General purpose parallel I/O and Fast I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

6.7.1 Features

- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.7.2 Fast I/O features available in LPC213x/01 only

- Fast I/O registers are located on the ARM local bus for the fastest possible I/O timing.
- All GPIO registers are byte addressable.
- Entire port value can be written in one instruction.
- Mask registers allow single instruction to set or clear any number of bits in one port.

6.8 10-bit ADC

The LPC2131/32 contain one and the LPC2134/36/38 contain two ADCs. These converters are single 10-bit successive approximation ADCs with eight multiplexed channels.

6.8.1 Features

- Measurement range of 0 V to 3.3 V.
- Each converter capable of performing more than 400000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal.
- Global Start command for both converters (LPC2134/36/38 only).

6.8.2 ADC features available in LPC213x/01 only

- Every analog input has a dedicated result register to reduce interrupt overhead.
- Every analog input can generate an interrupt once the conversion is completed.

6.9 10-bit DAC

This peripheral is available in the LPC2132/34/36/38 only. The DAC enables the LPC2132/34/36/38 to generate variable analog output.

6.9.1 Features

- 10-bit digital to analog converter.
- Buffered output.
- Power-down mode available.
- Selectable speed versus power.

6.10 UARTs

The LPC2131/32/34/36/38 each contain two UARTs. In addition to standard transmit and receive data lines, the LPC2134/36/38 UART1 also provides a full modem control handshake interface.

6.10.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B

- Built-in baud rate generator.
- Standard modem interface signals included on UART1. (LPC2134/36/38 only)
- The LPC2131/32/34/36/38 transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs and hardware (CTS/RTS) flow control on the LPC2134/36/38 UART1 only.

6.10.2 UART features available in LPC213x/01 only

- Fractional baud rate generator enables standard baud rates such as 115200 to be achieved with any crystal frequency above 2 MHz.
- Auto-bauding.
- Auto-CTS/RTS flow-control fully implemented in hardware (LPC2134/36/38 only).

6.11 I^2C-bus serial I/O controller

The LPC2131/32/34/36/38 each contain two I^2C-bus controllers.

The I^2C-bus is bidirectional, for inter-IC control using only two wires: a Serial Clock Line (SCL), and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver or a transmitter with the capability to both receive and send information (such as memory)). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

This I^2C-bus implementation supports bit rates up to 400 kbit/s (Fast I^2C).

6.11.1 Features

- Standard I^2C compliant bus interface.
- Easy to configure as Master, Slave, or Master/Slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus may be used for test and diagnostic purposes.

6.12 SPI serial I/O controller

The LPC2131/32/34/36/38 each contain one SPI controller. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

- Stop timer on match with optional interrupt generation.
- Reset timer on match with optional interrupt generation.

- Four external outputs per timer/counter corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

6.15 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

6.15.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal pre-scaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

6.16 Real-time clock

The Real-Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.16.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra-low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Can use either the RTC dedicated 32 kHz oscillator input or clock derived from the external crystal/oscillator input at XTAL1. Programmable Reference Clock Divider allows fine adjustment of the RTC.
- Dedicated power supply pin can be connected to a battery or the main 3.3 V.

6.18.8 Power Control

The LPC2131/32/34/36/38 support two reduced power modes: Idle mode and Power-down mode.

In Idle mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

In Power-down mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

Selecting an external 32 kHz clock instead of the PCLK as a clock-source for the on-chip RTC will enable the microcontroller to have the RTC active during Power-down mode. Power-down current is increased with RTC active. However, it is significantly lower than in Idle mode.

A Power Control for Peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

6.18.9 APB bus

The APB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The APB divider serves two purposes. The first is to provide peripherals with the desired PCLK via APB bus so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the APB bus may be slowed down to $\frac{1}{2}$ to $\frac{1}{4}$ of the processor clock rate. Because the APB bus must work properly at power-up (and its timing cannot be altered if it does not work since the APB divider control registers reside on the APB bus), the default condition at reset is for the APB bus to run at $\frac{1}{4}$ of the processor clock rate. The second purpose of the APB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the APB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

6.19 Emulation and debugging

The LPC2131/32/34/36/38 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Debugging and trace functions are multiplexed only with GPIOs on Port 1. This means that all communication, timer and interface peripherals residing on Port 0 are available during the development and debugging phase as they are when the application is run in the embedded system itself.

6.19.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. EmbeddedICE protocol convertor converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The debug communication channel is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

6.19.2 Embedded trace

Since the LPC2131/32/34/36/38 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code can not be traced because of this restriction.

6.19.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC, which is present in the EmbeddedICE logic. The LPC2131/32/34/36/38 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

[4] V_{DD} supply voltages must be present.

[5] 3-state outputs go into 3-state mode when V_{DD} is grounded.

[6] Please also see the errata note mentioned in the errata sheet.

[7] Accounts for 100 mV voltage drop in all supply lines.

[8] Only allowed for a short time period.

[9] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

[10] Applies to P1.16 to P1.25.

[11] On pin VBAT.

[12] Optimized for low battery consumption.

[13] To V_{SS}.

9. Dynamic characteristics

Table 7. Dynamic characteristics

T_{amb} = −40 °C to +85 °C for commercial applications, V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
External clock						
f_{osc}	oscillator frequency		10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	100	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0.2 and P0.3)						
$t_{r(o)}$	output rise time		-	10	-	ns
$t_{f(o)}$	output fall time		-	10	-	ns
I^2C-bus pins (P0.2 and P0.3)						
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$[3]	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

11. DAC electrical characteristics

Table 9. DAC electrical characteristics

V_{DDA} = 3.0 V to 3.6 V; T_{amb} = –40 °C to +85 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
E_D	differential linearity error		-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity		-	±1.5	-	LSB
E_O	offset error		-	0.6	-	%
E_G	gain error		-	0.6	-	%
C_L	load capacitance		-	200	-	pF
R_L	load resistance		1	-	-	kΩ

12.2 RTC 32 kHz oscillator component selection

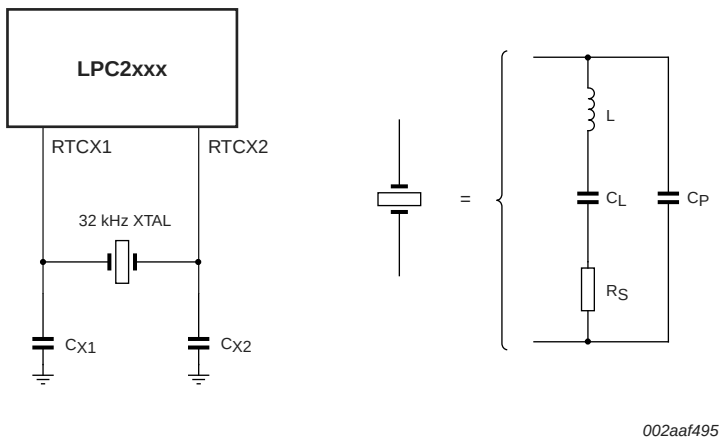


Fig 15. RTC oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

The RTC external oscillator circuit is shown in Figure 15. Since the feedback resistance is integrated on chip, only a crystal, the capacitances C_{X1} and C_{X2} need to be connected externally to the microcontroller.

Table 12 gives the crystal parameters that should be used. C_L is the typical load capacitance of the crystal and is usually specified by the crystal manufacturer. The actual C_L influences oscillation frequency. When using a crystal that is manufactured for a different load capacitance, the circuit will oscillate at a slightly different frequency (depending on the quality of the crystal) compared to the specified one. Therefore for an accurate time reference it is advised to use the load capacitors as specified in Table 12 that belong to a specific C_L. The value of external capacitances C_{X1} and C_{X2} specified in this table are calculated from the internal parasitic capacitances and the C_L. Parasitics from PCB and package are not taken into account.

Table 12. Recommended values for the RTC external 32 kHz oscillator C_{X1}/C_{X2} components

Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
11 pF	< 100 kΩ	18 pF, 18 pF
13 pF	< 100 kΩ	22 pF, 22 pF
15 pF	< 100 kΩ	27 pF, 27 pF

12.3 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plane. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

14. Abbreviations

Table 13. Acronym list

Acronym	Description
A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DCC	Debug Communications Channel
ETM	Embedded Trace Macrocell
FIFO	First In, First Out
GPIO	General Purpose Input/Output
JTAG	Joint Test Action Group
LSB	Least Significant Bit
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulator
RAM	Random Access Memory
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSP	Synchronous Serial Port
UART	Universal Asynchronous Receiver/Transmitter

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2131_32_34_36_38 v.5.1	20110729	Product data sheet	-	LPC2131_32_34_36_38 v.5
Modifications:	• Parameter I_{sink} added in Table 5 “Limiting values”. • Table 6 “Static characteristics”: Updated crystal oscillator specs			
LPC2131_32_34_36_38 v.5	20110202	Product data sheet	-	LPC2131_32_34_36_38 v.4
Modifications:	• Table 3 “Pin description”: Added Table note [9] to RTCX1 and RTCX2 pins. • Table 6 “Static characteristics”, I^2C-bus pins: Changed typical hysteresis voltage from $0.5V_{DD}$ to $0.05V_{DD}$. • Table 6 “Static characteristics”: Removed table note for V_{IH} and V_{IL}. • Changed all occurrences of VPB to APB. • Table 6 “Static characteristics”: Added Table note [6] to V_I. • Table 6 “Static characteristics”, Standard port pins, $\overline{\text{RESET}}$, RTCK: V_{hys} hysteresis voltage (0.4 V) moved from typical to minimum. • Table 6 “Static characteristics”: Changed $V_{i(VREF)}$ minimum voltage from 3.0 V to 2.5 V. • Table 6 “Static characteristics”: Updated min, typical and max values for oscillator pins $V_{i(XTAL1)}$, $V_{o(XTAL2)}$, $V_{i(RTCX1)}$, and $V_{o(RTCX2)}$. • Added Section 11 “DAC electrical characteristics”. • Added Section 12 “Application information”.			
LPC2131_32_34_36_38 v.4	20071016	Product data sheet	-	LPC2131_32_34_36_38 v.3
LPC2131_32_34_36_38 v.3	20060921	Product data sheet	-	LPC2131_32_34_36_38 v.2
LPC2131_32_34_36_38 v.2	20050318	Preliminary data sheet	-	LPC2131_2132_2138 v.1
LPC2131_2132_2138 v.1	20041118	Preliminary data sheet	-	-