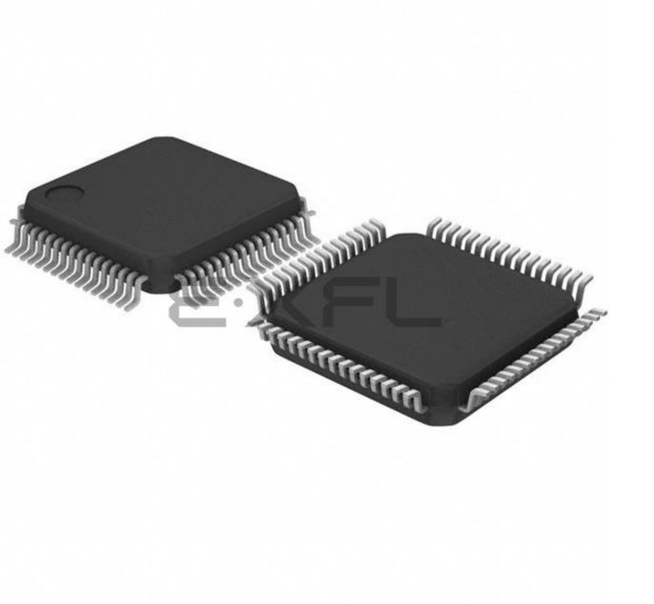

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	47
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2136fbd64-01-15

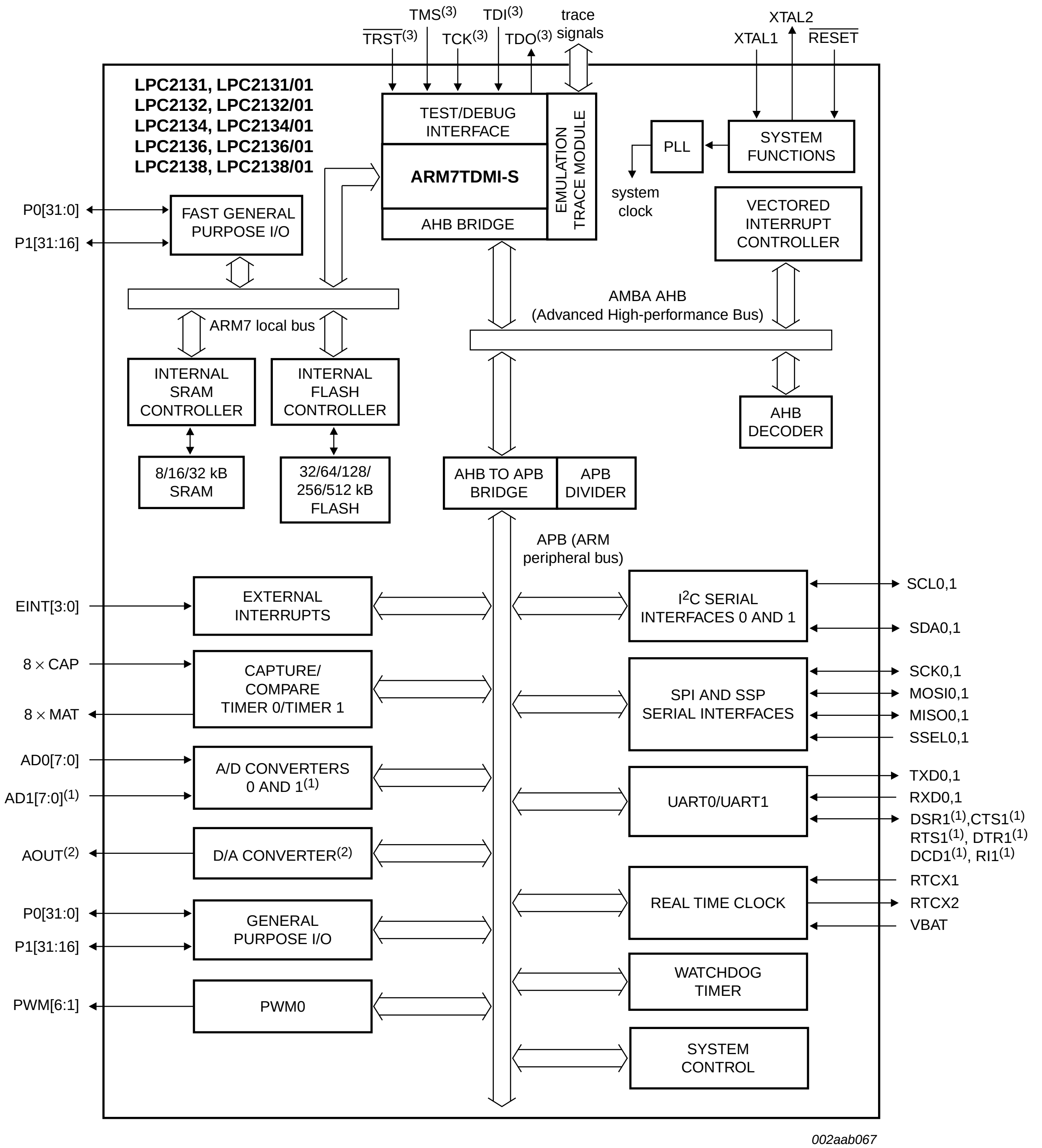
- One (LPC2131/32) or two (LPC2134/36/38) 8-channel 10-bit ADCs provide a total of up to 16 analog inputs, with conversion times as low as 2.44 μs per channel.
- Single 10-bit DAC provides variable analog output (LPC2132/34/36/38).
- Two 32-bit timers/external event counters (with four capture and four compare channels each), PWM unit (six outputs) and watchdog.
- Low power Real-time clock with independent power and dedicated 32 kHz clock input.
- Multiple serial interfaces including two UARTs (16C550), two Fast I^2C-bus (400 kbit/s), SPI and SSP with buffering and variable data length capabilities.
- Vectored interrupt controller with configurable priorities and vector addresses.
- Up to forty-seven 5 V tolerant general purpose I/O pins in tiny LQFP64 or HVQFN package.
- Up to nine edge or level sensitive external interrupt pins available.
- 60 MHz maximum CPU clock available from programmable on-chip PLL with settling time of 100 μs.
- On-chip integrated oscillator operates with external crystal in range of 1 MHz to 30 MHz and with external oscillator up to 50 MHz.
- Power saving modes include Idle and Power-down.
- Individual enable/disable of peripheral functions as well as peripheral clock scaling down for additional power optimization.
- Processor wake-up from Power-down mode via external interrupt or BOD.
- Single power supply chip with POR and BOD circuits:
  - CPU operating voltage range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2131FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2132FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2132FHN64/01	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-2
LPC2134FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2136FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2138FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2138FHN64/01	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-2

4. Block diagram



(1) LPC2134/36/38 only.

(2) LPC2132/34/36/38 only.

(3) Pins shared with GPIO.

Fig 1. Block diagram

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P1.26/RTCK	24[6]	I/O	**RTCK —** Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. LOW on RTCK while $\overline{RESET}$ is LOW enables pins P1.31:26 to operate as Debug port after reset.
P1.27/TDO	64[6]	O	**TDO —** Test Data out for JTAG interface.
P1.28/TDI	60[6]	I	**TDI —** Test Data in for JTAG interface.
P1.29/TCK	56[6]	I	**TCK —** Test Clock for JTAG interface.
P1.30/TMS	52[6]	I	**TMS —** Test Mode Select for JTAG interface.
P1.31/$\overline{TRST}$	20[6]	I	**$\overline{TRST}$ —** Test Reset for JTAG interface.
$\overline{RESET}$	57[7]	I	**External reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	62[8]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	61[8]	O	Output from the oscillator amplifier.
RTCX1	3[9]	I	Input to the RTC oscillator circuit.
RTCX2	5[9]	O	Output from the RTC oscillator circuit.
V_{SS}	6, 18, 25, 42, 50	I	**Ground:** 0 V reference.
V_{SSA}	59	I	**Analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
V_{DD}	23, 43, 51	I	**3.3 V power supply:** This is the power supply voltage for the core and I/O ports.
V_{DDA}	7	I	**Analog 3.3 V power supply:** This should be nominally the same voltage as V_{DD} but should be isolated to minimize noise and error. This voltage is used to power the on-chip PLL.
VREF	63	I	**ADC reference:** This should be nominally the same voltage as V_{DD} but should be isolated to minimize noise and error. Level on this pin is used as a reference for A/D and D/A convertor(s).
VBAT	49	I	**RTC power supply:** 3.3 V on this pin supplies the power to the RTC.

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control.

[2] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns.

[3] Open drain 5 V tolerant digital I/O I^2C-bus 400 kHz specification compatible pad. It requires external pull-up to provide an output functionality.

[4] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog input function. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns. When configured as an ADC input, digital section of the pad is disabled.

[5] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog output function. When configured as the DAC output, digital section of the pad is disabled.

[6] 5 V tolerant pad with built-in pull-up resistor providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. The pull-up resistor's value ranges from 60 kΩ to 300 kΩ.

[7] 5 V tolerant pad providing digital input (with TTL levels and hysteresis) function only.

[8] Pad provides special analog functionality.

[9] When unused, the RTCX1 pin can be grounded or left floating. For lowest power leave it floating.
The other RTC pin, RTCX2, should be left floating.

6. Functional description

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

6.2 On-chip flash program memory

The LPC2131/32/34/36/38 incorporate a 32 kB, 64 kB, 128 kB, 256 kB and 512 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. When the LPC2131/32/34/36/38 on-chip bootloader is used, 32/64/128/256/500 kB of flash memory is available for user code.

The LPC2131/32/34/36/38 flash memory provides a minimum of 100000 erase/write cycles and 20 years of data-retention.

6.3 On-chip static RAM

On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8-bit, 16-bit, and 32-bit. The LPC2131, LPC2132/34, and LPC2136/38 provide 8 kB, 16 kB and 32 kB of static RAM respectively.

6.4 Memory map

The LPC2131/32/34/36/38 memory map incorporates several distinct regions, as shown in Figure 6.

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in Section 6.18 "System control".

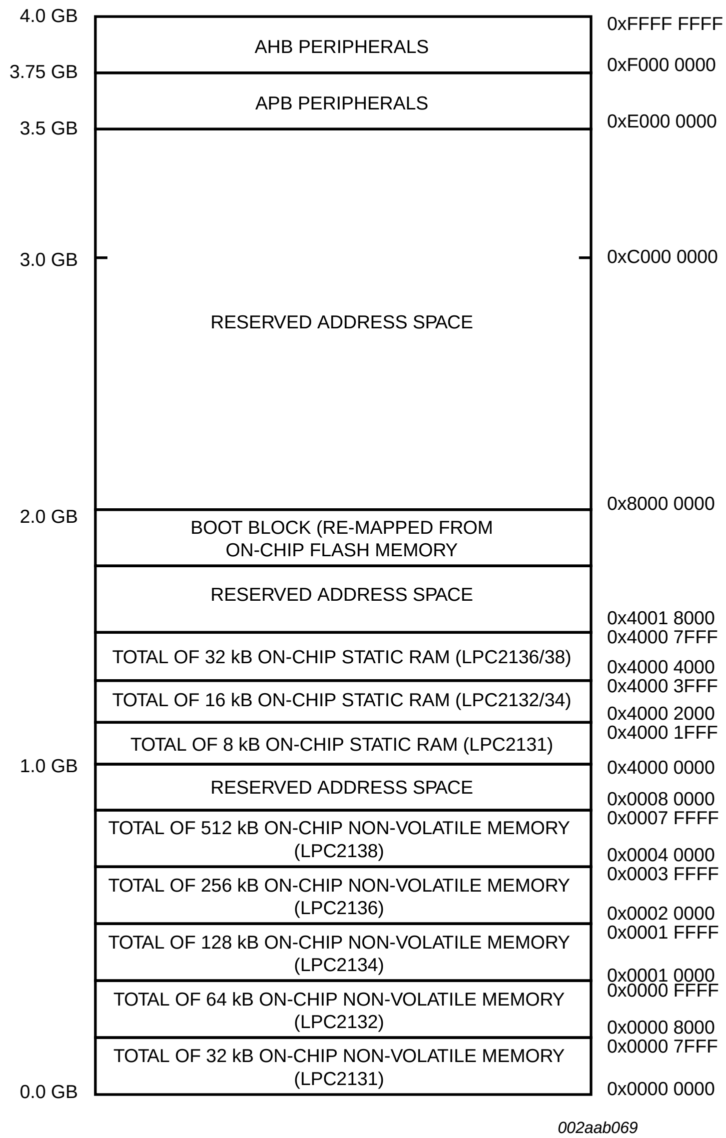


Fig 6. LPC2131/32/34/36/38 memory map

- Built-in baud rate generator.
- Standard modem interface signals included on UART1. (LPC2134/36/38 only)
- The LPC2131/32/34/36/38 transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs and hardware (CTS/RTS) flow control on the LPC2134/36/38 UART1 only.

6.10.2 UART features available in LPC213x/01 only

- Fractional baud rate generator enables standard baud rates such as 115200 to be achieved with any crystal frequency above 2 MHz.
- Auto-bauding.
- Auto-CTS/RTS flow-control fully implemented in hardware (LPC2134/36/38 only).

6.11 I^{2}C-bus serial I/O controller

The LPC2131/32/34/36/38 each contain two I^{2}C-bus controllers.

The I^{2}C-bus is bidirectional, for inter-IC control using only two wires: a Serial Clock Line (SCL), and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver or a transmitter with the capability to both receive and send information (such as memory)). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^{2}C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

This I^{2}C-bus implementation supports bit rates up to 400 kbit/s (Fast I^{2}C).

6.11.1 Features

- Standard I^{2}C compliant bus interface.
- Easy to configure as Master, Slave, or Master/Slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^{2}C-bus may be used for test and diagnostic purposes.

6.12 SPI serial I/O controller

The LPC2131/32/34/36/38 each contain one SPI controller. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

6.12.1 Features

- Compliant with Serial Peripheral Interface (SPI) specification.
- Synchronous, Serial, Full Duplex, Communication.
- Combined SPI master and slave.
- Maximum data bit rate of one eighth of the input clock rate.

6.13 SSP serial I/O controller

The LPC2131/32/34/36/38 each contain one Serial Synchronous Port controller (SSP). The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. However, only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. Often only one of these data flows carries meaningful data.

6.13.1 Features

- Compatible with Motorola SPI, 4-wire TI SSI and National Semiconductor Microwire buses.
- Synchronous Serial Communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- Four bits to 16 bits per frame.

6.14 General purpose timers/external event counters

The Timer/Counter is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock, and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with ‘or’ and ‘and’, as well as ‘broadcast’ functions among them.

At any given time only one of peripheral’s capture inputs can be selected as an external event signal source, i.e., timer’s clock. The rate of external events that can be successfully counted is limited to PCLK/2. In this configuration, unused capture lines can be selected as regular timer capture inputs.

6.14.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.
- External Event Counter or timer operation.
- Four 32-bit capture channels per timer/counter that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.

6.17 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2131/32/34/36/38. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.17.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.

6.18.8 Power Control

The LPC2131/32/34/36/38 support two reduced power modes: Idle mode and Power-down mode.

In Idle mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

In Power-down mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

Selecting an external 32 kHz clock instead of the PCLK as a clock-source for the on-chip RTC will enable the microcontroller to have the RTC active during Power-down mode. Power-down current is increased with RTC active. However, it is significantly lower than in Idle mode.

A Power Control for Peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

6.18.9 APB bus

The APB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The APB divider serves two purposes. The first is to provide peripherals with the desired PCLK via APB bus so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the APB bus may be slowed down to $\frac{1}{2}$ to $\frac{1}{4}$ of the processor clock rate. Because the APB bus must work properly at power-up (and its timing cannot be altered if it does not work since the APB divider control registers reside on the APB bus), the default condition at reset is for the APB bus to run at $\frac{1}{4}$ of the processor clock rate. The second purpose of the APB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the APB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

6.19 Emulation and debugging

The LPC2131/32/34/36/38 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Debugging and trace functions are multiplexed only with GPIOs on Port 1. This means that all communication, timer and interface peripherals residing on Port 0 are available during the development and debugging phase as they are when the application is run in the embedded system itself.

6.19.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. EmbeddedICE protocol convertor converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The debug communication channel is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

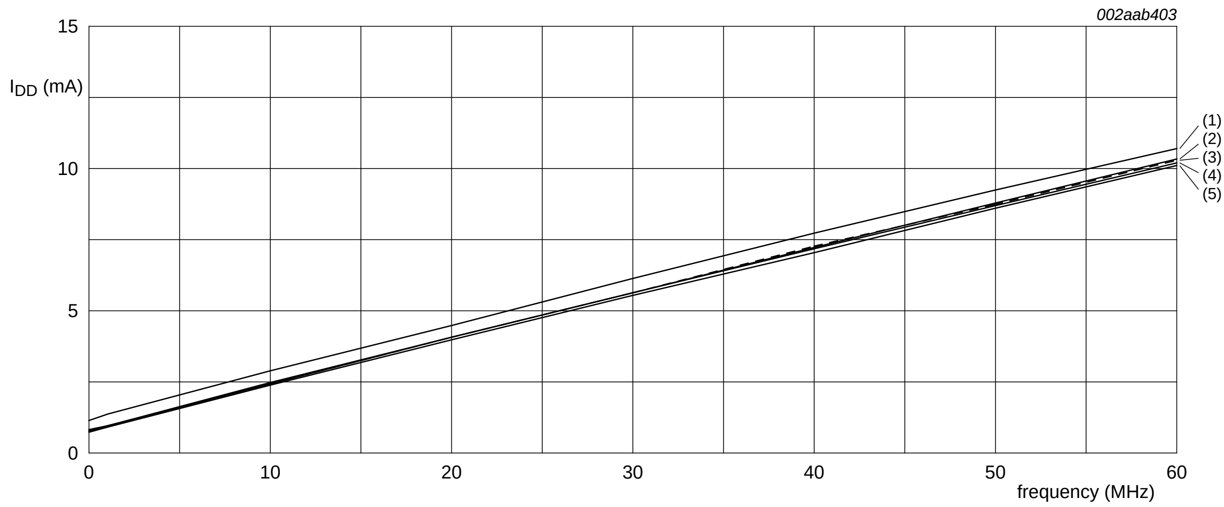
6.19.2 Embedded trace

Since the LPC2131/32/34/36/38 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code can not be traced because of this restriction.

6.19.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC, which is present in the EmbeddedICE logic. The LPC2131/32/34/36/38 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.



Test conditions: Idle mode entered executing code from flash; all peripherals are enabled in PCONP register; PCLK = CCLK/4.

(1) V_{DD} = 3.6 V at 140 °C (max)

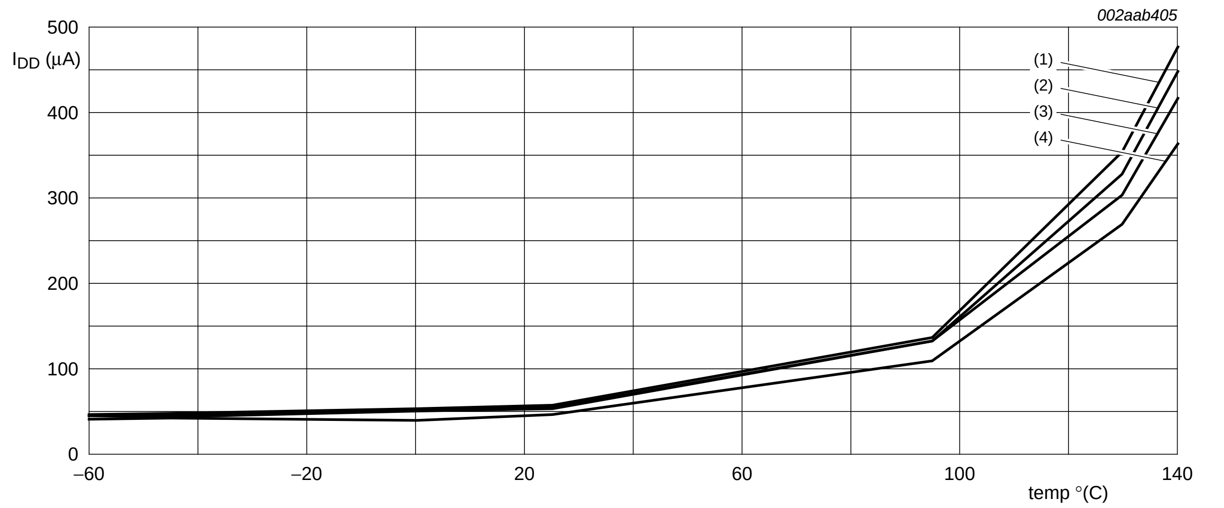
(2) V_{DD} = 3.6 V at −60 °C

(3) V_{DD} = 3.6 V at 25 °C

(4) V_{DD} = 3.3 V at 25 °C (typical)

(5) V_{DD} = 3.3 V at 95 °C (typical)

Fig 9. I_{DD} idle measured at different frequencies (CCLK) and temperatures



Test conditions: Power-down mode entered executing code from flash; all peripherals are enabled in PCONP register.

(1) V_{DD} = 3.6 V

(2) V_{DD} = 3.3 V (max)

(3) V_{DD} = 3.0 V

(4) V_{DD} = 3.3 V (typical)

Fig 10. $I_{DD(pd)}$ measured at different temperatures

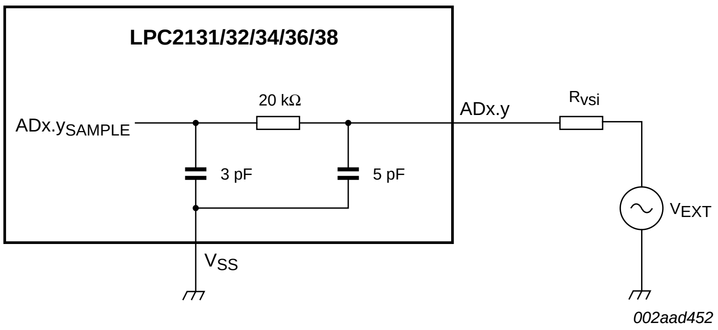


Fig 12. Suggested ADC interface - LPC2131/32/34/36/38 ADx.y pin

11. DAC electrical characteristics

Table 9. DAC electrical characteristics

V_{DDA} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
E_D	differential linearity error		-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity		-	±1.5	-	LSB
E_O	offset error		-	0.6	-	%
E_G	gain error		-	0.6	-	%
C_L	load capacitance		-	200	-	pF
R_L	load resistance		1	-	-	kΩ

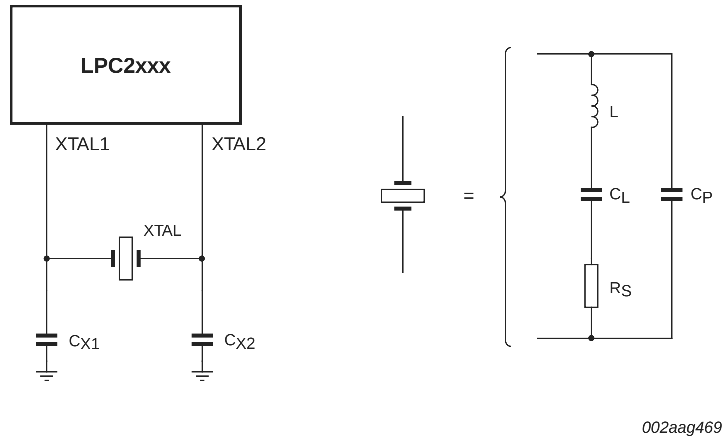


Fig 14. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 10. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 11. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, $_{CX2}$
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

12.2 RTC 32 kHz oscillator component selection

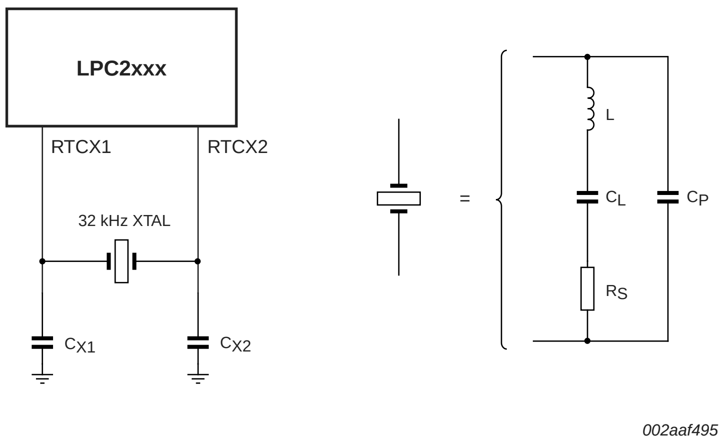


Fig 15. RTC oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

The RTC external oscillator circuit is shown in Figure 15. Since the feedback resistance is integrated on chip, only a crystal, the capacitances C_{X1} and C_{X2} need to be connected externally to the microcontroller.

Table 12 gives the crystal parameters that should be used. C_L is the typical load capacitance of the crystal and is usually specified by the crystal manufacturer. The actual C_L influences oscillation frequency. When using a crystal that is manufactured for a different load capacitance, the circuit will oscillate at a slightly different frequency (depending on the quality of the crystal) compared to the specified one. Therefore for an accurate time reference it is advised to use the load capacitors as specified in Table 12 that belong to a specific C_L. The value of external capacitances C_{X1} and C_{X2} specified in this table are calculated from the internal parasitic capacitances and the C_L. Parasitics from PCB and package are not taken into account.

Table 12. Recommended values for the RTC external 32 kHz oscillator C_{X1}/C_{X2} components

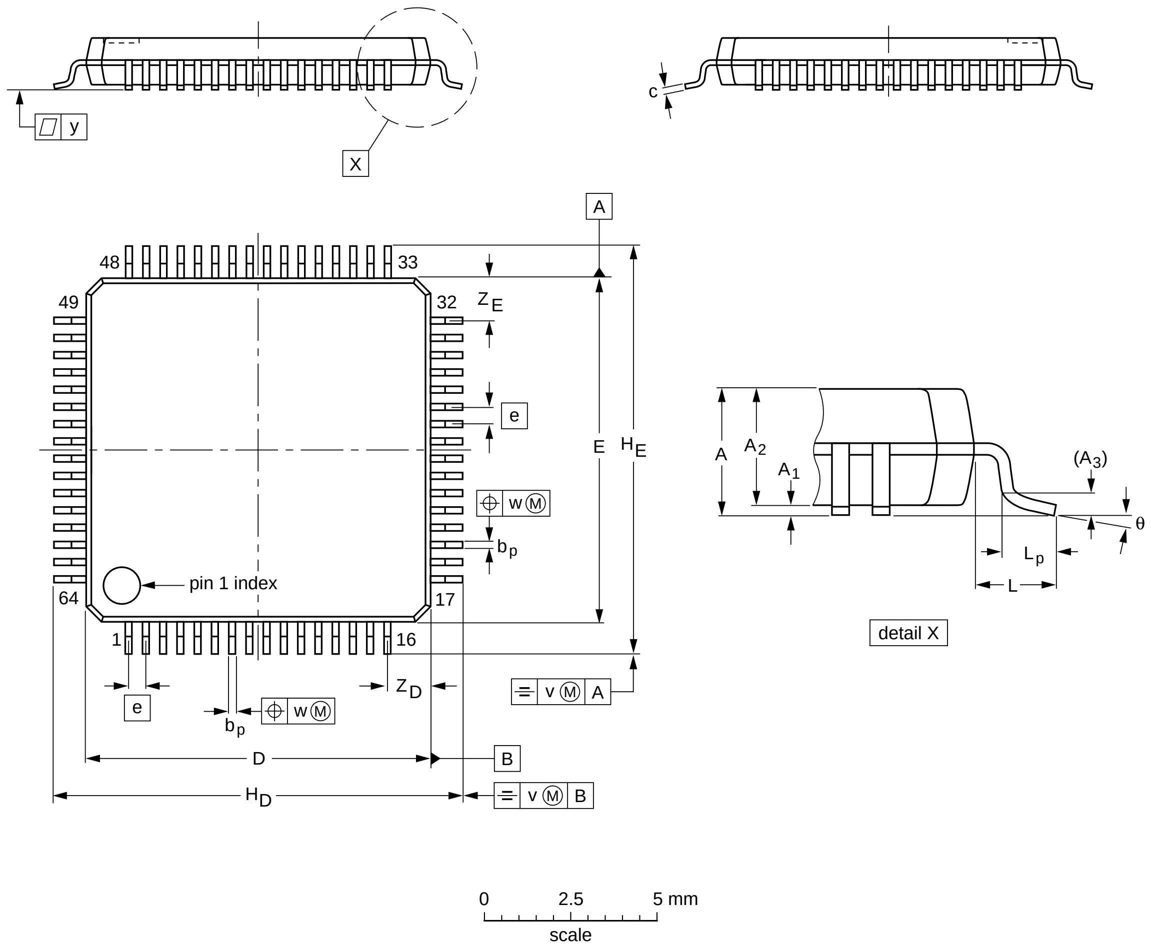
Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
11 pF	< 100 kΩ	18 pF, 18 pF
13 pF	< 100 kΩ	22 pF, 22 pF
15 pF	< 100 kΩ	27 pF, 27 pF

12.3 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plane. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

13. Package outline

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 16. Package outline SOT314-2 (LQFP64)

14. Abbreviations

Table 13. Acronym list

Acronym	Description
A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DCC	Debug Communications Channel
ETM	Embedded Trace Macrocell
FIFO	First In, First Out
GPIO	General Purpose Input/Output
JTAG	Joint Test Action Group
LSB	Least Significant Bit
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulator
RAM	Random Access Memory
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSP	Synchronous Serial Port
UART	Universal Asynchronous Receiver/Transmitter

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2131_32_34_36_38 v.5.1	20110729	Product data sheet	-	LPC2131_32_34_36_38 v.5
Modifications:	• Parameter I_{sink} added in Table 5 "Limiting values". • Table 6 "Static characteristics": Updated crystal oscillator specs			
LPC2131_32_34_36_38 v.5	20110202	Product data sheet	-	LPC2131_32_34_36_38 v.4
Modifications:	• Table 3 "Pin description": Added Table note [9] to RTCX1 and RTCX2 pins. • Table 6 "Static characteristics", I^2C-bus pins: Changed typical hysteresis voltage from $0.5V_{DD}$ to $0.05V_{DD}$. • Table 6 "Static characteristics": Removed table note for V_{IH} and V_{IL}. • Changed all occurrences of VPB to APB. • Table 6 "Static characteristics": Added Table note [6] to V_I. • Table 6 "Static characteristics", Standard port pins, $\overline{RESET}$, RTCK: V_{hys} hysteresis voltage (0.4 V) moved from typical to minimum. • Table 6 "Static characteristics": Changed $V_{i(VREF)}$ minimum voltage from 3.0 V to 2.5 V. • Table 6 "Static characteristics": Updated min, typical and max values for oscillator pins $V_{i(XTAL1)}$, $V_{o(XTAL2)}$, $V_{i(RTCX1)}$, and $V_{o(RTCX2)}$. • Added Section 11 "DAC electrical characteristics". • Added Section 12 "Application information".			
LPC2131_32_34_36_38 v.4	20071016	Product data sheet	-	LPC2131_32_34_36_38 v.3
LPC2131_32_34_36_38 v.3	20060921	Product data sheet	-	LPC2131_32_34_36_38 v.2
LPC2131_32_34_36_38 v.2	20050318	Preliminary data sheet	-	LPC2131_2132_2138 v.1
LPC2131_2132_2138 v.1	20041118	Preliminary data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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