**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | ARM7® |
| Core Size | 16/32-Bit |
| Speed | 60MHz |
| Connectivity | I²C, Microwire, SPI, SSI, SSP, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 47 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 16x10b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2138fbd64-01-11 |

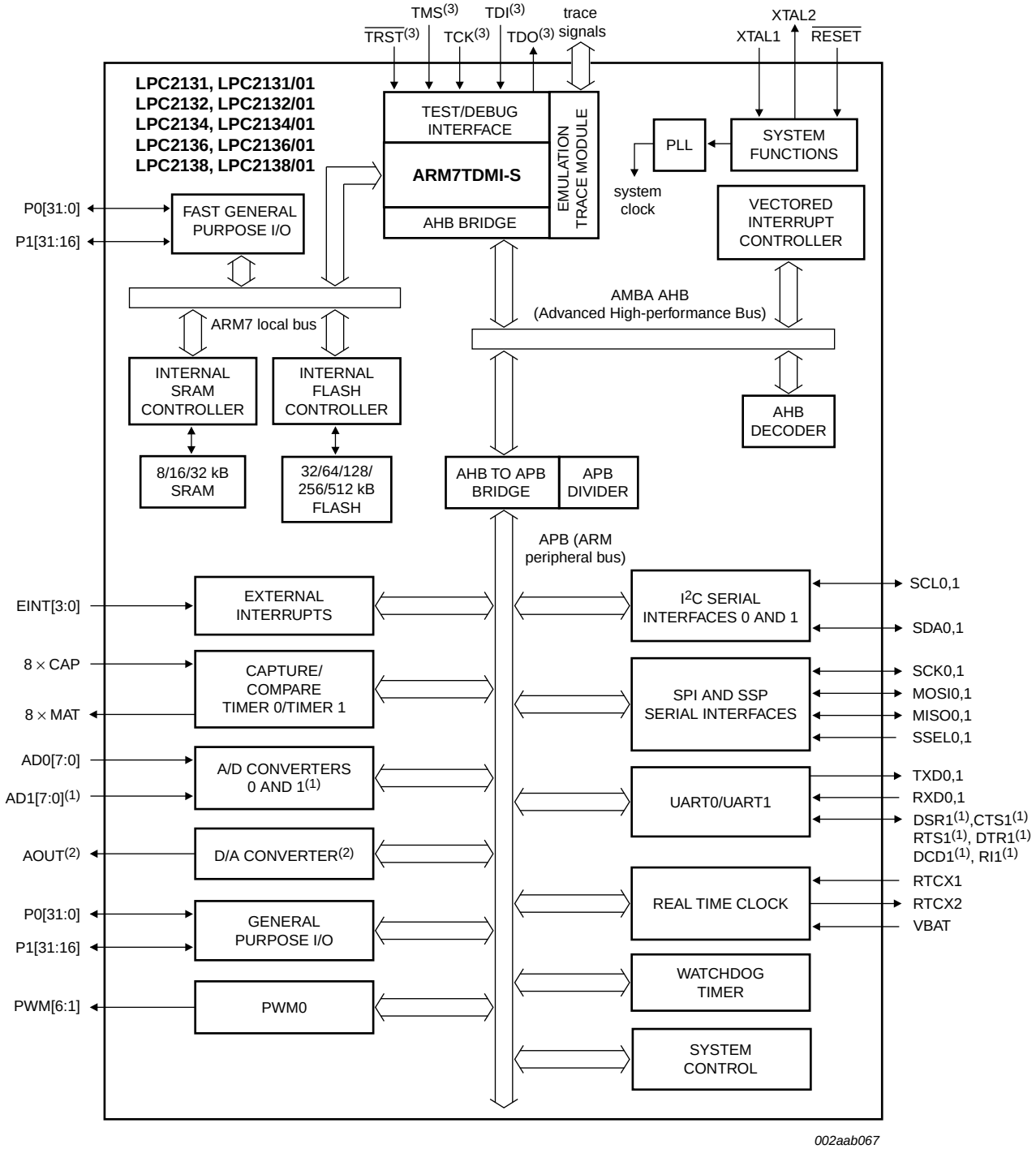
- One (LPC2131/32) or two (LPC2134/36/38) 8-channel 10-bit ADCs provide a total of up to 16 analog inputs, with conversion times as low as 2.44 μs per channel.
- Single 10-bit DAC provides variable analog output (LPC2132/34/36/38).
- Two 32-bit timers/external event counters (with four capture and four compare channels each), PWM unit (six outputs) and watchdog.
- Low power Real-time clock with independent power and dedicated 32 kHz clock input.
- Multiple serial interfaces including two UARTs (16C550), two Fast $I^2C$-bus (400 kbit/s), SPI and SSP with buffering and variable data length capabilities.
- Vectored interrupt controller with configurable priorities and vector addresses.
- Up to forty-seven 5 V tolerant general purpose I/O pins in tiny LQFP64 or HVQFN package.
- Up to nine edge or level sensitive external interrupt pins available.
- 60 MHz maximum CPU clock available from programmable on-chip PLL with settling time of 100 μs.
- On-chip integrated oscillator operates with external crystal in range of 1 MHz to 30 MHz and with external oscillator up to 50 MHz.
- Power saving modes include Idle and Power-down.
- Individual enable/disable of peripheral functions as well as peripheral clock scaling down for additional power optimization.
- Processor wake-up from Power-down mode via external interrupt or BOD.
- Single power supply chip with POR and BOD circuits:
  - CPU operating voltage range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads.

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| LPC2131FBD64/01 | LQFP64 | plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm | SOT314-2 |
| LPC2132FBD64/01 | LQFP64 | plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm | SOT314-2 |
| LPC2132FHN64/01 | HVQFN64 | plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm | SOT804-2 |
| LPC2134FBD64/01 | LQFP64 | plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm | SOT314-2 |
| LPC2136FBD64/01 | LQFP64 | plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm | SOT314-2 |
| LPC2138FBD64/01 | LQFP64 | plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm | SOT314-2 |
| LPC2138FHN64/01 | HVQFN64 | plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm | SOT804-2 |

# 4. Block diagram




(1) LPC2134/36/38 only.

(2) LPC2132/34/36/38 only.

(3) Pins shared with GPIO.

**Fig 1. Block diagram**

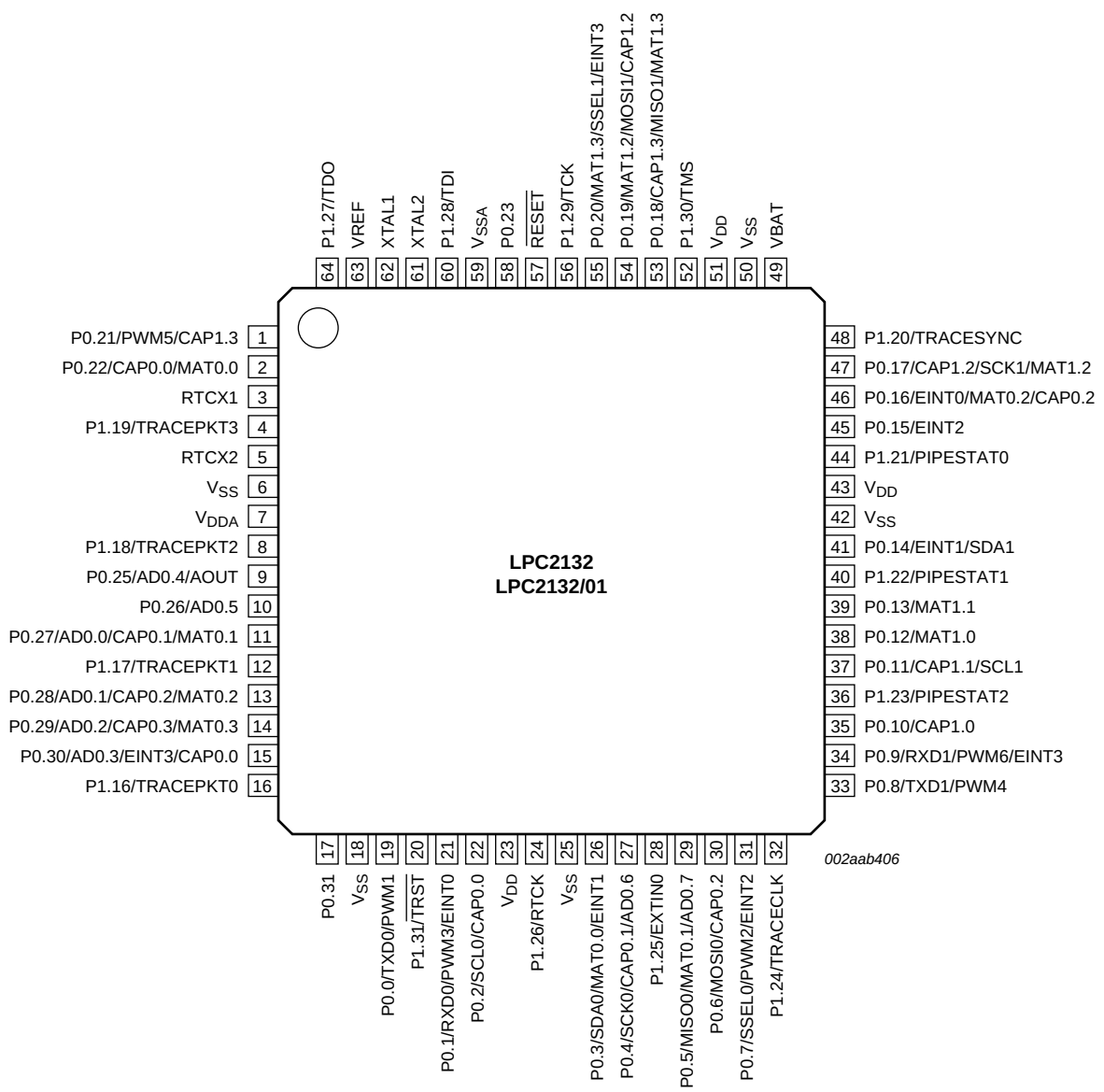



**Fig 3. LPC2132 LQFP64 pin configuration**

**Table 3. Pin description** *…continued*

| Symbol | Pin | Type | Description |
|---|---|---|---|
| P0.11/CTS1/ CAP1.1/SCL1 | 37[3] | I | **CTS1 —** Clear to Send input for UART1. Available in LPC2134/36/38. |
| | | I | **CAP1.1 —** Capture input for Timer 1, channel 1. |
| | | I/O | **SCL1 —** $I^2C1$ clock input/output. Open drain output (for $I^2C$-bus compliance) |
| P0.12/DSR1/ MAT1.0/AD1.3 | 38[4] | I | **DSR1 —** Data Set Ready input for UART1. Available in LPC2134/36/38. |
| | | O | **MAT1.0 —** Match output for Timer 1, channel 0. |
| | | I | **AD1.3 —** ADC 1, input 3. This analog input is always connected to its pin. Available in LPC2134/36/38 only. |
| P0.13/DTR1/ MAT1.1/AD1.4 | 39[4] | O | **DTR1 —** Data Terminal Ready output for UART1. Available in LPC2134/36/38. |
| | | O | **MAT1.1 —** Match output for Timer 1, channel 1. |
| | | I | **AD1.4 —** ADC 1, input 4. This analog input is always connected to its pin. Available in LPC2134/36/38 only. |
| P0.14/DCD1/ EINT1/SDA1 | 41[3] | I | **DCD1 —** Data Carrier Detect input for UART1. Available in LPC2134/36/38. |
| | | I | **EINT1 —** External interrupt 1 input. |
| | | I/O | **SDA1 —** $I^2C1$ data input/output. Open drain output (for $I^2C$-bus compliance). |
| P0.15/RI1/ EINT2/AD1.5 | 45[4] | I | **RI1 —** Ring Indicator input for UART1. Available in LPC2134/36/38. |
| | | I | **EINT2 —** External interrupt 2 input. |
| | | I | **AD1.5 —** ADC 1, input 5. This analog input is always connected to its pin. Available in LPC2134/36/38 only. |
| P0.16/EINT0/ MAT0.2/CAP0.2 | 46[2] | I | **EINT0 —** External interrupt 0 input. |
| | | O | **MAT0.2 —** Match output for Timer 0, channel 2. |
| | | I | **CAP0.2 —** Capture input for Timer 0, channel 2. |
| P0.17/CAP1.2/ SCK1/MAT1.2 | 47[1] | I | **CAP1.2 —** Capture input for Timer 1, channel 2. |
| | | I/O | **SCK1 —** Serial Clock for SSP. Clock output from master or input to slave. |
| | | O | **MAT1.2 —** Match output for Timer 1, channel 2. |
| P0.18/CAP1.3/ MISO1/MAT1.3 | 53[1] | I | **CAP1.3 —** Capture input for Timer 1, channel 3. |
| | | I/O | **MISO1 —** Master In Slave Out for SSP. Data input to SPI master or data output from SSP slave. |
| | | O | **MAT1.3 —** Match output for Timer 1, channel 3. |
| P0.19/MAT1.2/ MOSI1/CAP1.2 | 54[1] | O | **MAT1.2 —** Match output for Timer 1, channel 2. |
| | | I/O | **MOSI1 —** Master Out Slave In for SSP. Data output from SSP master or data input to SSP slave. |
| | | I | **CAP1.2 —** Capture input for Timer 1, channel 2. |
| P0.20/MAT1.3/ SSEL1/EINT3 | 55[2] | O | **MAT1.3 —** Match output for Timer 1, channel 3. |
| | | I | **SSEL1 —** Slave Select for SSP. Selects the SSP interface as a slave. |
| | | I | **EINT3 —** External interrupt 3 input. |
| P0.21/PWM5/ AD1.6/CAP1.3 | 1[4] | O | **PWM5 —** Pulse Width Modulator output 5. |
| | | I | **AD1.6 —** ADC 1, input 6. This analog input is always connected to its pin. Available in LPC2134/36/38 only. |
| | | I | **CAP1.3 —** Capture input for Timer 1, channel 3. |
| P0.22/AD1.7/ CAP0.0/MAT0.0 | 2[4] | I | **AD1.7 —** ADC 1, input 7. This analog input is always connected to its pin. Available in LPC2134/36/38 only. |
| | | I | **CAP0.0 —** Capture input for Timer 0, channel 0. |
| | | O | **MAT0.0 —** Match output for Timer 0, channel 0. |

**Table 3. Pin description** *…continued*

| Symbol | Pin | Type | Description |
|---|---|---|---|
| P1.26/RTCK | 24[6] | I/O | **RTCK —** Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. LOW on RTCK while $\overline{\text{RESET}}$ is LOW enables pins P1.31:26 to operate as Debug port after reset. |
| P1.27/TDO | 64[6] | O | **TDO —** Test Data out for JTAG interface. |
| P1.28/TDI | 60[6] | I | **TDI —** Test Data in for JTAG interface. |
| P1.29/TCK | 56[6] | I | **TCK —** Test Clock for JTAG interface. |
| P1.30/TMS | 52[6] | I | **TMS —** Test Mode Select for JTAG interface. |
| P1.31/$\overline{\text{TRST}}$ | 20[6] | I | **$\overline{\text{TRST}}$ —** Test Reset for JTAG interface. |
| $\overline{\text{RESET}}$ | 57[7] | I | **External reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant. |
| XTAL1 | 62[8] | I | Input to the oscillator circuit and internal clock generator circuits. |
| XTAL2 | 61[8] | O | Output from the oscillator amplifier. |
| RTCX1 | 3[9] | I | Input to the RTC oscillator circuit. |
| RTCX2 | 5[9] | O | Output from the RTC oscillator circuit. |
| $V_{SS}$ | 6, 18, 25, 42, 50 | I | **Ground:** 0 V reference. |
| $V_{SSA}$ | 59 | I | **Analog ground:** 0 V reference. This should nominally be the same voltage as $V_{SS}$, but should be isolated to minimize noise and error. |
| $V_{DD}$ | 23, 43, 51 | I | **3.3 V power supply:** This is the power supply voltage for the core and I/O ports. |
| $V_{DDA}$ | 7 | I | **Analog 3.3 V power supply:** This should be nominally the same voltage as $V_{DD}$ but should be isolated to minimize noise and error. This voltage is used to power the on-chip PLL. |
| VREF | 63 | I | **ADC reference:** This should be nominally the same voltage as $V_{DD}$ but should be isolated to minimize noise and error. Level on this pin is used as a reference for A/D and D/A convertor(s). |
| VBAT | 49 | I | **RTC power supply:** 3.3 V on this pin supplies the power to the RTC. |

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control.

[2] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns.

[3] Open drain 5 V tolerant digital I/O $I^2C$-bus 400 kHz specification compatible pad. It requires external pull-up to provide an output functionality.

[4] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog input function. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns. When configured as an ADC input, digital section of the pad is disabled.

[5] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog output function. When configured as the DAC output, digital section of the pad is disabled.

[6] 5 V tolerant pad with built-in pull-up resistor providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. The pull-up resistor's value ranges from 60 kΩ to 300 kΩ.

[7] 5 V tolerant pad providing digital input (with TTL levels and hysteresis) function only.

[8] Pad provides special analog functionality.

[9] When unused, the RTCX1 pin can be grounded or left floating. For lowest power leave it floating.
The other RTC pin, RTCX2, should be left floating.

**Table 4. Interrupt sources** *…continued*

| Block | Flag(s) | VIC channel # |
|---|---|---|
| UART1 | RX Line Status (RLS) | 7 |
| | Transmit Holding Register empty (THRE) | |
| | RX Data Available (RDA) | |
| | Character Time-out Indicator (CTI) | |
| | Modem Status Interrupt (MSI) (Available in LPC2134/36/38 only) | |
| PWM0 | Match 0 to 6 (MR0, MR1, MR2, MR3, MR4, MR5, MR6) | 8 |
| | Capture 0 to 3 (CR0, CR1, CR2, CR3) | |
| $I^2C0$ | SI (state change) | 9 |
| SPI0 | SPIF, MODF | 10 |
| SSP | TX FIFO at least half empty (TXRIS) | 11 |
| | RX FIFO at least half full (RXRIS) | |
| | Receive Timeout (RTRIS) | |
| | Receive Overrun (RORRIS) | |
| PLL | PLL Lock (PLOCK) | 12 |
| RTC | RTCCIF (Counter Increment), RTCALF (Alarm) | 13 |
| System Control | External Interrupt 0 (EINT0) | 14 |
| | External Interrupt 1 (EINT1) | 15 |
| | External Interrupt 2 (EINT2) | 16 |
| | External Interrupt 3 (EINT3) | 17 |
| AD0 | ADC 0 | 18 |
| I2C1 | SI (state change) | 19 |
| BOD | Brown Out Detect | 20 |
| AD1 | ADC 1 (Available in LPC2134/36/38 only) | 21 |

## 6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

## 6.7 General purpose parallel I/O and Fast I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

### 6.7.1 Features

- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

### 6.7.2 Fast I/O features available in LPC213x/01 only

- Fast I/O registers are located on the ARM local bus for the fastest possible I/O timing.
- All GPIO registers are byte addressable.
- Entire port value can be written in one instruction.
- Mask registers allow single instruction to set or clear any number of bits in one port.

## 6.8 10-bit ADC

The LPC2131/32 contain one and the LPC2134/36/38 contain two ADCs. These converters are single 10-bit successive approximation ADCs with eight multiplexed channels.

### 6.8.1 Features

- Measurement range of 0 V to 3.3 V.
- Each converter capable of performing more than 400000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal.
- Global Start command for both converters (LPC2134/36/38 only).

### 6.8.2 ADC features available in LPC213x/01 only

- Every analog input has a dedicated result register to reduce interrupt overhead.
- Every analog input can generate an interrupt once the conversion is completed.

## 6.9 10-bit DAC

This peripheral is available in the LPC2132/34/36/38 only. The DAC enables the LPC2132/34/36/38 to generate variable analog output.

### 6.9.1 Features

- 10-bit digital to analog converter.
- Buffered output.
- Power-down mode available.
- Selectable speed versus power.

## 6.10 UARTs

The LPC2131/32/34/36/38 each contain two UARTs. In addition to standard transmit and receive data lines, the LPC2134/36/38 UART1 also provides a full modem control handshake interface.

### 6.10.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B

- Built-in baud rate generator.
- Standard modem interface signals included on UART1. (LPC2134/36/38 only)
- The LPC2131/32/34/36/38 transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs and hardware (CTS/RTS) flow control on the LPC2134/36/38 UART1 only.

### 6.10.2 UART features available in LPC213x/01 only

- Fractional baud rate generator enables standard baud rates such as 115200 to be achieved with any crystal frequency above 2 MHz.
- Auto-bauding.
- Auto-CTS/RTS flow-control fully implemented in hardware (LPC2134/36/38 only).

## 6.11 $I^2C$-bus serial I/O controller

The LPC2131/32/34/36/38 each contain two $I^2C$-bus controllers.

The $I^2C$-bus is bidirectional, for inter-IC control using only two wires: a Serial Clock Line (SCL), and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver or a transmitter with the capability to both receive and send information (such as memory)). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The $I^2C$-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

This $I^2C$-bus implementation supports bit rates up to 400 kbit/s (Fast $I^2C$).

### 6.11.1 Features

- Standard $I^2C$ compliant bus interface.
- Easy to configure as Master, Slave, or Master/Slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The $I^2C$-bus may be used for test and diagnostic purposes.

## 6.12 SPI serial I/O controller

The LPC2131/32/34/36/38 each contain one SPI controller. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

- Stop timer on match with optional interrupt generation.
- Reset timer on match with optional interrupt generation.

- Four external outputs per timer/counter corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

## 6.15 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

### 6.15.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal pre-scaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

## 6.16 Real-time clock

The Real-Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

### 6.16.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra-low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Can use either the RTC dedicated 32 kHz oscillator input or clock derived from the external crystal/oscillator input at XTAL1. Programmable Reference Clock Divider allows fine adjustment of the RTC.
- Dedicated power supply pin can be connected to a battery or the main 3.3 V.

## 6.17 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2131/32/34/36/38. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

### 6.17.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.

- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.

## 6.18 System control

### 6.18.1 Crystal oscillator

On-chip integrated oscillator operates with external crystal in range of 1 MHz to 30 MHz and with external oscillator up to 50 MHz. The oscillator output frequency is called $f_{osc}$ and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. $f_{osc}$ and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.18.2 “PLL” for additional information.

### 6.18.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μs.

### 6.18.3 Reset and wake-up timer

Reset has two sources on the LPC2131/32/34/36/38: the $\overline{\text{RESET}}$ pin and watchdog reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the wake-up timer (see wake-up timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The wake-up timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up timer.

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The debug communication channel is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

### 6.19.2 Embedded trace

Since the LPC2131/32/34/36/38 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code can not be traced because of this restriction.

### 6.19.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC, which is present in the EmbeddedICE logic. The LPC2131/32/34/36/38 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

**Table 6. Static characteristics** *…continued*

*$T_{amb}$ = −40 °C to +85 °C for commercial applications, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{BATpd}$ | Power-down mode battery supply current | RTC clock = 32 kHz (from RTCXn pins); $T_{amb}$ = 25 °C | | | | | |
| | | $V_{DD}$ = 3.0 V; $V_{i(VBAT)}$ = 2.5 V | [11] | - | 14 | - | μA |
| | | $V_{DD}$ = 3.0 V; $V_{i(VBAT)}$ = 3.0 V | | - | 16 | - | μA |
| | | $V_{DD}$ = 3.3 V; $V_{i(VBAT)}$ = 3.3 V | | - | 18 | - | μA |
| | | $V_{DD}$ = 3.6 V; $V_{i(VBAT)}$ = 3.6 V | | - | 20 | - | μA |
| $I_{BATact}$ | active mode battery supply current | CCLK = 60 MHz; PCLK = 15 MHz; PCLK enabled to RTCK; RTC clock = 32 kHz (from RTCXn pins); $T_{amb}$ = 25 °C | [11] | | | | |
| | | $V_{DD}$ = 3.0 V; $V_{i(VBAT)}$ = 3.0 V | | - | 78 | - | μA |
| | | $V_{DD}$ = 3.3 V; $V_{i(VBAT)}$ = 3.3 V | | - | 80 | - | μA |
| | | $V_{DD}$ = 3.6 V; $V_{i(VBAT)}$ = 3.6 V | | - | 82 | - | μA |
| $I_{BATact(opt)}$ | optimized active mode battery supply current | PCLK disabled to RTCK in the PCONP register; RTC clock = 32 kHz (from RTCXn pins); $T_{amb}$ = 25 °C; $V_{i(VBAT)}$ = 3.3 V | [11][12] | | | | |
| | | CCLK = 6 MHz | | - | 21 | - | μA |
| | | CCLK = 25 MHz | | - | 23 | - | μA |
| | | CCLK = 50 MHz | | - | 27 | - | μA |
| | | CCLK = 60 MHz | | - | 30 | - | μA |
| **$I^2C$-bus pins** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | | $0.7V_{DD}$ | - | - | V |
| $V_{IL}$ | LOW-level input voltage | | | - | - | $0.3V_{DD}$ | V |
| $V_{hys}$ | hysteresis voltage | | | - | $0.05V_{DD}$ | - | V |
| $V_{OL}$ | LOW-level output voltage | $I_{OLS}$ = 3 mA | [7] | - | - | 0.4 | V |
| $I_{LI}$ | input leakage current | $V_I = V_{DD}$ | [13] | - | 2 | 4 | μA |
| | | $V_I$ = 5 V | [13] | - | 10 | 22 | μA |
| **Oscillator pins** | | | | | | | |
| $V_{i(XTAL1)}$ | input voltage on pin XTAL1 | | | −0.5 | 1.8 | 1.95 | V |
| $V_{o(XTAL2)}$ | output voltage on pin XTAL2 | | | −0.5 | 1.8 | 1.95 | V |
| $V_{i(RTCX1)}$ | input voltage on pin RTCX1 | | | −0.5 | 1.8 | 1.95 | V |
| $V_{o(RTCX2)}$ | output voltage on pin RTCX2 | | | −0.5 | 1.8 | 1.95 | V |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[3] Including voltage on outputs in 3-state mode.

[4] $V_{DD}$ supply voltages must be present.

[5] 3-state outputs go into 3-state mode when $V_{DD}$ is grounded.

[6] Please also see the errata note mentioned in the errata sheet.

[7] Accounts for 100 mV voltage drop in all supply lines.

[8] Only allowed for a short time period.

[9] Minimum condition for $V_I$ = 4.5 V, maximum condition for $V_I$ = 5.5 V.

[10] Applies to P1.16 to P1.25.

[11] On pin VBAT.

[12] Optimized for low battery consumption.

[13] To $V_{SS}$.

# 9. Dynamic characteristics

**Table 7. Dynamic characteristics**

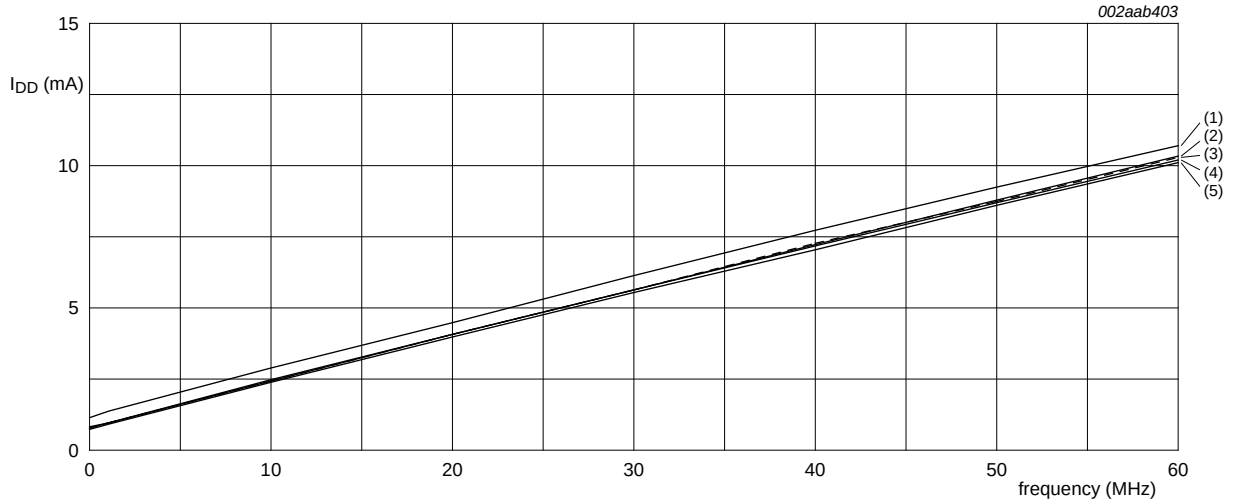
*$T_{amb}$ = −40 °C to +85 °C for commercial applications, $V_{DD}$ over specified ranges.*[1]

| Symbol | Parameter | Conditions | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|---|
| **External clock** | | | | | | |
| $f_{osc}$ | oscillator frequency | | 10 | - | 25 | MHz |
| $T_{cy(clk)}$ | clock cycle time | | 40 | - | 100 | ns |
| $t_{CHCX}$ | clock HIGH time | | $T_{cy(clk)} \times 0.4$ | - | - | ns |
| $t_{CLCX}$ | clock LOW time | | $T_{cy(clk)} \times 0.4$ | - | - | ns |
| $t_{CLCH}$ | clock rise time | | - | - | 5 | ns |
| $t_{CHCL}$ | clock fall time | | - | - | 5 | ns |
| **Port pins (except P0.2 and P0.3)** | | | | | | |
| $t_{r(o)}$ | output rise time | | - | 10 | - | ns |
| $t_{f(o)}$ | output fall time | | - | 10 | - | ns |
| **$I^2C$-bus pins (P0.2 and P0.3)** | | | | | | |
| $t_{f(o)}$ | output fall time | $V_{IH}$ to $V_{IL}$ | $20 + 0.1 \times C_b$[3] | - | - | ns |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance $C_b$ in pF, from 10 pF to 400 pF.




Test conditions: Idle mode entered executing code from flash; all peripherals are enabled in PCONP register; PCLK = CCLK/4.

(1) $V_{DD}$ = 3.6 V at 140 °C (max)

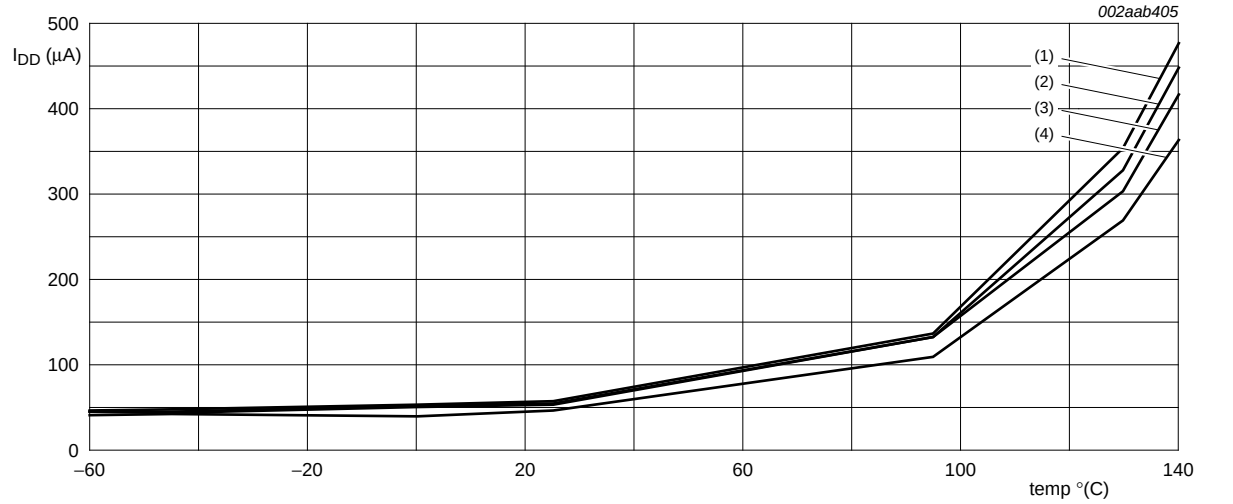
(2) $V_{DD}$ = 3.6 V at −60 °C

(3) $V_{DD}$ = 3.6 V at 25 °C

(4) $V_{DD}$ = 3.3 V at 25 °C (typical)

(5) $V_{DD}$ = 3.3 V at 95 °C (typical)

**Fig 9. $I_{DD}$ idle measured at different frequencies (CCLK) and temperatures**




Test conditions: Power-down mode entered executing code from flash; all peripherals are enabled in PCONP register.

(1) $V_{DD}$ = 3.6 V

(2) $V_{DD}$ = 3.3 V (max)

(3) $V_{DD}$ = 3.0 V

(4) $V_{DD}$ = 3.3 V (typical)

**Fig 10. $I_{DD(pd)}$ measured at different temperatures**

# 10. ADC electrical characteristics

**Table 8. ADC static characteristics**

*$V_{DDA}$ = 2.5 V to 3.6 V; $T_{amb}$ = –40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IA}$ | analog input voltage | | | 0 | - | $V_{DDA}$ | V |
| $C_{ia}$ | analog input capacitance | | | - | - | 1 | pF |
| $E_D$ | differential linearity error | | [1][2][3] | - | - | ±1 | LSB |
| $E_{L(adj)}$ | integral non-linearity | | [1][4] | - | - | ±2 | LSB |
| $E_O$ | offset error | | [1][5] | - | - | ±3 | LSB |
| $E_G$ | gain error | | [1][6] | - | - | ±0.5 | % |
| $E_T$ | absolute error | | [1][7] | - | - | ±4 | LSB |
| $R_{vsi}$ | voltage source interface resistance | | [8] | - | - | 40 | kΩ |

[1] Conditions: $V_{SSA}$ = 0 V, $V_{DDA}$ = 3.3 V.

[2] The ADC is monotonic, there are no missing codes.

[3] The differential linearity error ($E_D$) is the difference between the actual step width and the ideal step width. See Figure 11.

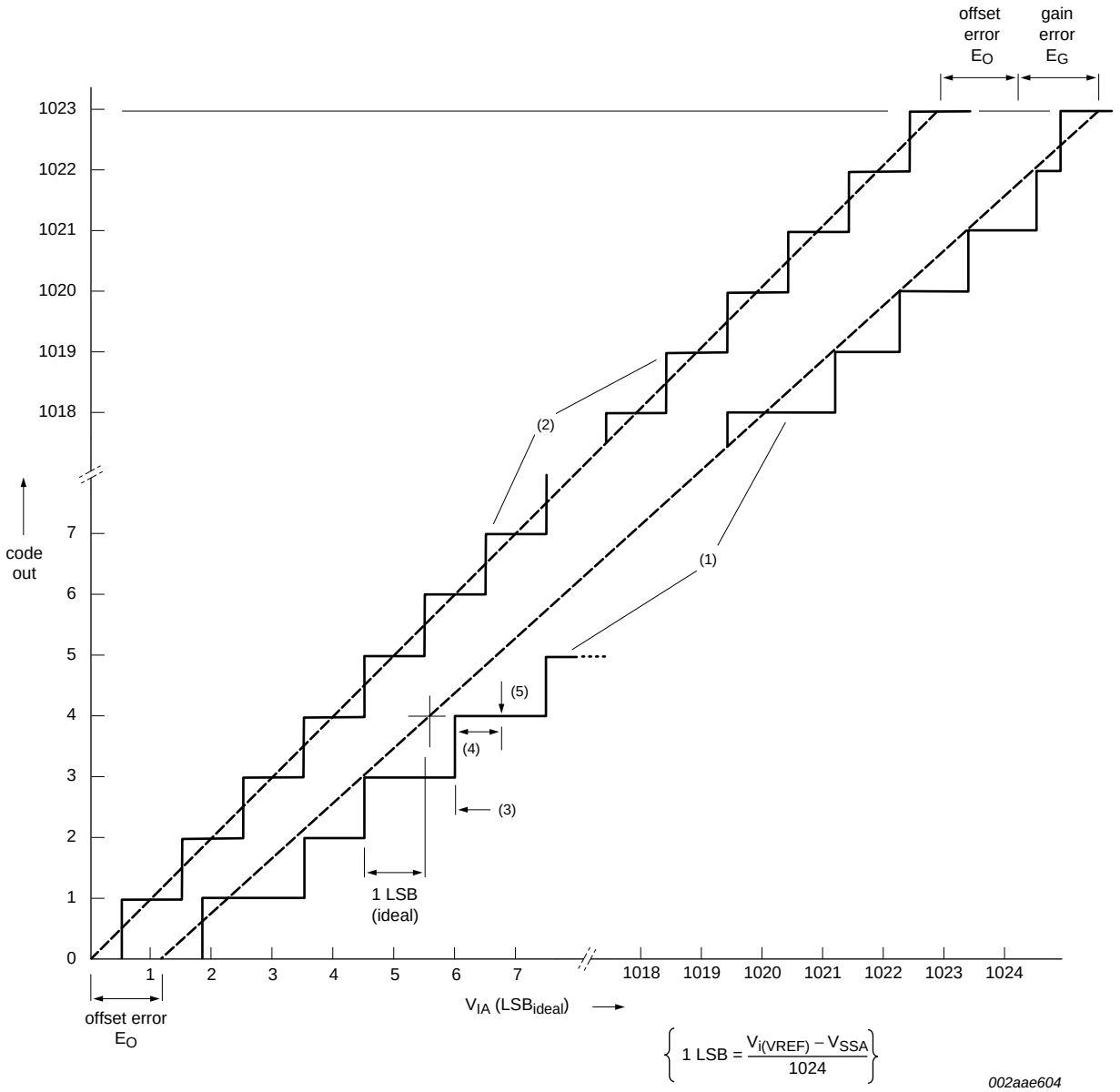
[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 11.

[5] The offset error ($E_O$) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 11.

[6] The gain error ($E_G$) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 11.

[7] The absolute error ($E_T$) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 11.

[8] See Figure 11.




(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error ($E_D$).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

**Fig 11. ADC characteristics**

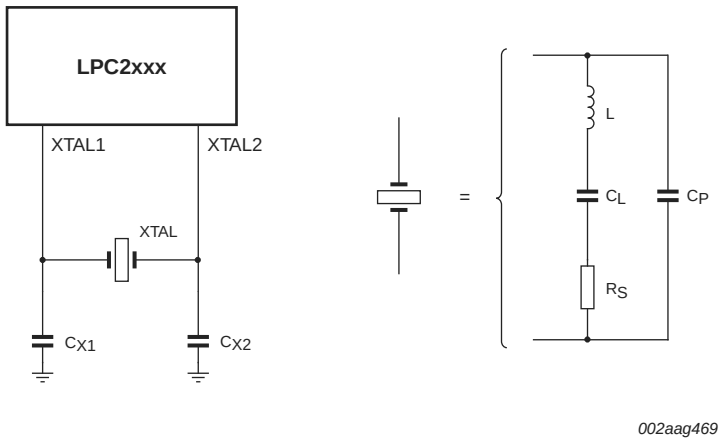



**Fig 14. Oscillator modes and models: oscillation mode of operation and external crystal model used for $C_{X1}/C_{X2}$ evaluation**

**Table 10. Recommended values for $C_{X1}/C_{X2}$ in oscillation mode (crystal and external components parameters): low frequency mode**

| Fundamental oscillation frequency $F_{OSC}$ | Crystal load capacitance $C_L$ | Maximum crystal series resistance $R_S$ | External load capacitors $C_{X1}/C_{X2}$ |
|---|---|---|---|
| 1 MHz to 5 MHz | 10 pF | < 300 Ω | 18 pF, 18 pF |
| | 20 pF | < 300 Ω | 39 pF, 39 pF |
| | 30 pF | < 300 Ω | 57 pF, 57 pF |
| 5 MHz to 10 MHz | 10 pF | < 300 Ω | 18 pF, 18 pF |
| | 20 pF | < 200 Ω | 39 pF, 39 pF |
| | 30 pF | < 100 Ω | 57 pF, 57 pF |
| 10 MHz to 15 MHz | 10 pF | < 160 Ω | 18 pF, 18 pF |
| | 20 pF | < 60 Ω | 39 pF, 39 pF |
| 15 MHz to 20 MHz | 10 pF | < 80 Ω | 18 pF, 18 pF |

**Table 11. Recommended values for $C_{X1}/C_{X2}$ in oscillation mode (crystal and external components parameters): high frequency mode**

| Fundamental oscillation frequency $F_{OSC}$ | Crystal load capacitance $C_L$ | Maximum crystal series resistance $R_S$ | External load capacitors $C_{X1}$, $C_{X2}$ |
|---|---|---|---|
| 15 MHz to 20 MHz | 10 pF | < 180 Ω | 18 pF, 18 pF |
| | 20 pF | < 100 Ω | 39 pF, 39 pF |
| 20 MHz to 25 MHz | 10 pF | < 160 Ω | 18 pF, 18 pF |
| | 20 pF | < 80 Ω | 39 pF, 39 pF |

# 14. Abbreviations

**Table 13. Acronym list**

| Acronym | Description |
|---|---|
| A/D | Analog-to-Digital |
| ADC | Analog-to-Digital Converter |
| AHB | Advanced High-performance Bus |
| AMBA | Advanced Microcontroller Bus Architecture |
| APB | Advanced Peripheral Bus |
| BOD | BrownOut Detection |
| CPU | Central Processing Unit |
| DAC | Digital-to-Analog Converter |
| DCC | Debug Communications Channel |
| ETM | Embedded Trace Macrocell |
| FIFO | First In, First Out |
| GPIO | General Purpose Input/Output |
| JTAG | Joint Test Action Group |
| LSB | Least Significant Bit |
| PLL | Phase-Locked Loop |
| POR | Power-On Reset |
| PWM | Pulse Width Modulator |
| RAM | Random Access Memory |
| SPI | Serial Peripheral Interface |
| SRAM | Static Random Access Memory |
| SSP | Synchronous Serial Port |
| UART | Universal Asynchronous Receiver/Transmitter |

# 18. Contents





For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 29 July 2011**
**Document identifier: LPC2131_32_34_36_38**