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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	I ² C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	45
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30800safp-bl-u5

1.4 Product Information

Table 1.2 lists the product information. Figure 1.2 shows the product numbering system.

Table 1.2 M32C/80 Group

As of November, 2005

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30800SAGP	PLQP0100KB-A (100P6Q-A)	—	8K	ROMless
M30800SAFP	PRQP0100JB-A (100P6S-A)			
M30800SAGP-BL	PLQP0100KB-A (100P6Q-A)			ROMless with on-chip boot loader
M30800SAFP-BL	PRQP0100JB-A (100P6S-A)			

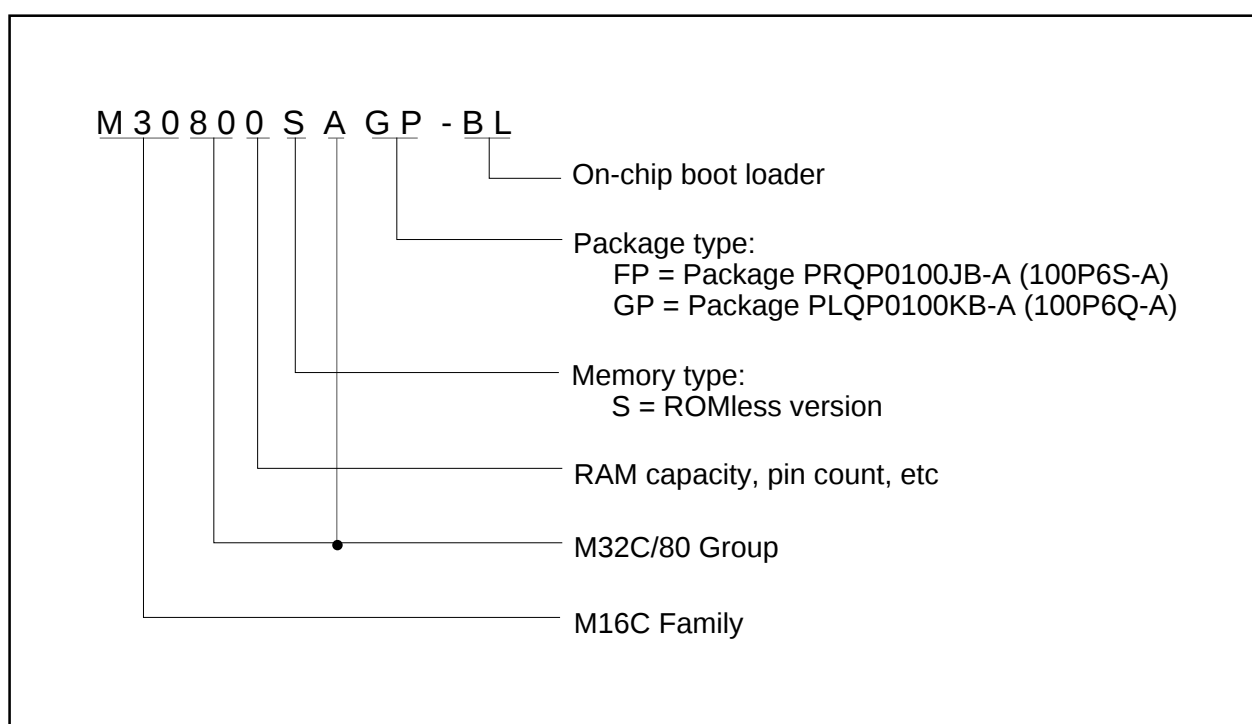


Figure 1.2 Product Numbering System

1.5 Pin Assignment

Figures 1.3 and 1.4 show pin assignments (top view).

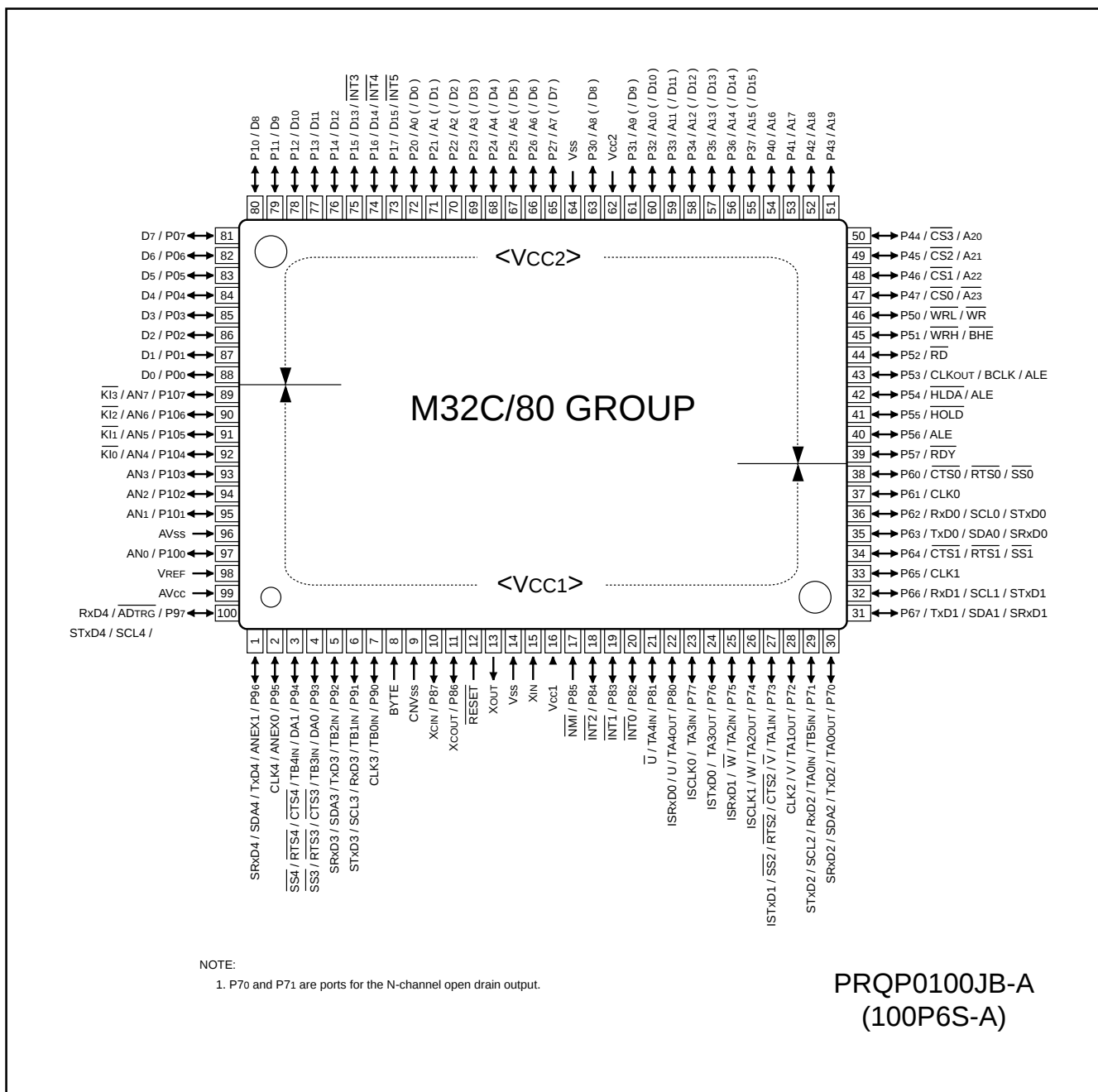


Figure 1.3 Pin Assignment

Table 1.3 Pin Characteristics (Continued)

Package pin No		Control pins	Port	Interrupt pins	Timer pins	UART pins	Analog pins	Bus control pins	Intelligent I/O pins
FP	GP								
51	49		P43					A19	
52	50		P42					A18	
53	51		P41					A17	
54	52		P40					A16	
55	53		P37					A15(/D15)	
56	54		P36					A14(/D14)	
57	55		P35					A13(/D13)	
58	56		P34					A12(/D12)	
59	57		P33					A11(/D11)	
60	58		P32					A10(/D10)	
61	59		P31					A9(/D9)	
62	60	VCC2							
63	61		P30					A8(/D8)	
64	62	VSS							
65	63		P27					A7(/D7)	
66	64		P26					A6(/D6)	
67	65		P25					A5(/D5)	
68	66		P24					A4(/D4)	
69	67		P23					A3(/D3)	
70	68		P22					A2(/D2)	
71	69		P21					A1(/D1)	
72	70		P20					A0(/D0)	
73	71		P17	INT5				D15	
74	72		P16	INT4				D14	
75	73		P15	INT3				D13	
76	74		P14					D12	
77	75		P13					D11	
78	76		P12					D10	
79	77		P11					D9	
80	78		P10					D8	
81	79		P07					D7	
82	80		P06					D6	
83	81		P05					D5	
84	82		P04					D4	
85	83		P03					D3	
86	84		P02					D2	
87	85		P01					D1	
88	86		P00					D0	
89	87		P107	KI3			AN7		
90	88		P106	KI2			AN6		
91	89		P105	KI1			AN5		
92	90		P104	KI0			AN4		
93	91		P103				AN3		
94	92		P102				AN2		
95	93		P101				AN1		
96	94	AVSS							
97	95		P100				AN0		
98	96						VREF		
99	97	AVCC							
100	98		P97			RxD4/SCL4/STxD4	ADTRG		

2.1 General Registers

2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R3.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

2.1.5 Program Counter (PC)

PC, 24 bits wide, indicates the address of an instruction to be executed.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating the starting address of an relocatable interrupt vector table.

2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are 24 bits wide each. The U flag is used to switch between USP and ISP. Refer to **2.1.8 Flag Register (FLG)** for details on the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating a CPU state.

2.1.8.1 Carry Flag (C)

The C flag indicates whether carry or borrow has occurred after executing an instruction.

2.1.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.1.8.3 Zero Flag (Z)

The Z flag is set to "1" when the value of zero is obtained from an arithmetic operation; otherwise "0".

2.1.8.4 Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic operation; otherwise "0".

4. Special Function Registers (SFRs)

Address	Register	Symbol	Value after RESET
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor Mode Register ⁽¹⁾	PM0	0000 0011 ₂ (CNVss pin ="H")
0005 ₁₆	Processor Mode Register 1	PM1	00 ₁₆
0006 ₁₆	System Clock Control Register 0	CM0	0000 1000 ₂
0007 ₁₆	System Clock Control Register 1	CM1	0010 0000 ₂
0008 ₁₆			
0009 ₁₆	Address Match Interrupt Enable Register	AIER	00 ₁₆
000A ₁₆	Protect Register	PRCR	XXXX 0000 ₂
000B ₁₆	External Data Bus Width Control Register	DS	XXXX 1000 ₂ (BYTE pin ="L") XXXX 0000 ₂ (BYTE pin ="H")
000C ₁₆	Main Clock Division Register	MCD	XXX0 1000 ₂
000D ₁₆	Oscillation Stop Detection Register	CM2	00 ₁₆
000E ₁₆	Watchdog Timer Start Register	WDTS	XX ₁₆
000F ₁₆	Watchdog Timer Control Register	WDC	000X XXXX ₂
0010 ₁₆			
0011 ₁₆	Address Match Interrupt Register 0	RMAD0	000000 ₁₆
0012 ₁₆			
0013 ₁₆	Processor Mode Register 2	PM2	00 ₁₆
0014 ₁₆	Address Match Interrupt Register 1	RMAD1	000000 ₁₆
0015 ₁₆			
0016 ₁₆			
0017 ₁₆			
0018 ₁₆	Address Match Interrupt Register 2	RMAD2	000000 ₁₆
0019 ₁₆			
001A ₁₆			
001B ₁₆			
001C ₁₆	Address Match Interrupt Register 3	RMAD3	000000 ₁₆
001D ₁₆			
001E ₁₆			
001F ₁₆			
0020 ₁₆			
0021 ₁₆			
0022 ₁₆			
0023 ₁₆			
0024 ₁₆			
0025 ₁₆			
0026 ₁₆	PLL Control Register 0	PLC0	0001 X010 ₂
0027 ₁₆	PLL Control Register 1	PLC1	000X 0000 ₂
0028 ₁₆	Address Match Interrupt Register 4	RMAD4	000000 ₁₆
0029 ₁₆			
002A ₁₆			
002B ₁₆			
002C ₁₆	Address Match Interrupt Register 5	RMAD5	000000 ₁₆
002D ₁₆			
002E ₁₆			
002F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTE:

1. The PM01 and PM00 bits in the PM0 register maintain values set before reset, even after software reset or watchdog timer reset has been performed.

Address	Register	Symbol	Value after RESET
0090 ₁₆	UART0 Transmit /NACK Interrupt Control Register	S0TIC	XXXX X000 ₂
0091 ₁₆	UART1/UART4 Bus Conflict Detect Interrupt Control Register	BCN1IC/BCN4IC	XXXX X000 ₂
0092 ₁₆	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X000 ₂
0093 ₁₆	Key Input Interrupt Control Register	KUPIC	XXXX X000 ₂
0094 ₁₆	Timer B0 Interrupt Control Register	TB0IC	XXXX X000 ₂
0095 ₁₆	Intelligent I/O Interrupt Control Register 1	IIO1IC	XXXX X000 ₂
0096 ₁₆	Timer B2 Interrupt Control Register	TB2IC	XXXX X000 ₂
0097 ₁₆	Intelligent I/O Interrupt Control Register 3	IIO3IC	XXXX X000 ₂
0098 ₁₆	Timer B4 Interrupt Control Register	TB4IC	XXXX X000 ₂
0099 ₁₆			
009A ₁₆	INT4 Interrupt Control Register	INT4IC	XX00 X000 ₂
009B ₁₆			
009C ₁₆	INT2 Interrupt Control Register	INT2IC	XX00 X000 ₂
009D ₁₆			
009E ₁₆	INT0 Interrupt Control Register	INT0IC	XX00 X000 ₂
009F ₁₆	Exit Priority Control Register	RLVL	XXXX 0000 ₂
00A0 ₁₆	Interrupt Request Register 0	IIO0IR	0000 000X ₂
00A1 ₁₆	Interrupt Request Register 1	IIO1IR	0000 000X ₂
00A2 ₁₆	Interrupt Request Register 2	IIO2IR	0000 000X ₂
00A3 ₁₆	Interrupt Request Register 3	IIO3IR	0000 000X ₂
00A4 ₁₆	Interrupt Request Register 4	IIO4IR	0000 000X ₂
00A5 ₁₆			
00A6 ₁₆			
00A7 ₁₆			
00A8 ₁₆			
00A9 ₁₆			
00AA ₁₆			
00AB ₁₆			
00AC ₁₆			
00AD ₁₆			
00AE ₁₆			
00AF ₁₆			
00B0 ₁₆	Interrupt Enable Register 0	IIO0IE	00 ₁₆
00B1 ₁₆	Interrupt Enable Register 1	IIO1IE	00 ₁₆
00B2 ₁₆	Interrupt Enable Register 2	IIO2IE	00 ₁₆
00B3 ₁₆	Interrupt Enable Register 3	IIO3IE	00 ₁₆
00B4 ₁₆	Interrupt Enable Register 4	IIO4IE	00 ₁₆
00B5 ₁₆			
00B6 ₁₆			
00B7 ₁₆			
00B8 ₁₆			
00B9 ₁₆			
00BA ₁₆			
00BB ₁₆			
00BC ₁₆			
00BD ₁₆			
00BE ₁₆			
00BF ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00C0 ₁₆			
00C1 ₁₆			
00C2 ₁₆			
00C3 ₁₆			
00C4 ₁₆			
00C5 ₁₆			
00C6 ₁₆			
00C7 ₁₆			
00C8 ₁₆			
00C9 ₁₆			
00CA ₁₆			
00CB ₁₆			
00CC ₁₆			
00CD ₁₆			
00CE ₁₆			
00CF ₁₆			
00D0 ₁₆			
00D1 ₁₆			
00D2 ₁₆			
00D3 ₁₆			
00D4 ₁₆			
00D5 ₁₆			
00D6 ₁₆			
00D7 ₁₆			
00D8 ₁₆			
00D9 ₁₆			
00DA ₁₆			
00DB ₁₆			
00DC ₁₆			
00DD ₁₆			
00DE ₁₆			
00DF ₁₆			
00E0 ₁₆			
00E1 ₁₆			
00E2 ₁₆			
00E3 ₁₆			
00E4 ₁₆			
00E5 ₁₆			
00E6 ₁₆			
00E7 ₁₆			
00E8 ₁₆ 00E9 ₁₆	SI/O Receive Buffer Register 0	G0RB	XXXX XXXX ₂ XXX0 XXXX ₂
00EA ₁₆ 00EB ₁₆	Transmit Buffer/Receive Data Register 0	G0TB/G0DR	XX ₁₆
00EC ₁₆	Receive Input Register 0	G0RI	XX ₁₆
00ED ₁₆	SI/O Communication Mode Register 0	G0MR	00 ₁₆
00EE ₁₆	Transmit Output Register 0	G0TO	XX ₁₆
00EF ₁₆	SI/O Communication Control Register 0	G0CR	0000 X011 ₂

X: Indeterminate

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Address	Register	Symbol	Value after RESET
02E0 ₁₆	X/Y Control Register	XYC	XXXX XX00 ₂
02E1 ₁₆			
02E2 ₁₆			
02E3 ₁₆			
02E4 ₁₆	UART1 Special Mode Register 4	U1SMR4	00 ₁₆
02E5 ₁₆	UART1 Special Mode Register 3	U1SMR3	00 ₁₆
02E6 ₁₆	UART1 Special Mode Register 2	U1SMR2	00 ₁₆
02E7 ₁₆	UART1 Special Mode Register	U1SMR	00 ₁₆
02E8 ₁₆	UART1 Transmit/Receive Mode Register	U1MR	00 ₁₆
02E9 ₁₆	UART1 Bit Rate Register	U1BRG	XX ₁₆
02EA ₁₆	UART1 Transmit Buffer Register	U1TB	XX ₁₆
02EB ₁₆			XX ₁₆
02EC ₁₆	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000 ₂
02ED ₁₆	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010 ₂
02EE ₁₆	UART1 Receive Buffer Register	U1RB	XX ₁₆
02EF ₁₆			XX ₁₆
02F0 ₁₆			
02F1 ₁₆			
02F2 ₁₆			
02F3 ₁₆			
02F4 ₁₆	UART4 Special Mode Register 4	U4SMR4	00 ₁₆
02F5 ₁₆	UART4 Special Mode Register 3	U4SMR3	00 ₁₆
02F6 ₁₆	UART4 Special Mode Register 2	U4SMR2	00 ₁₆
02F7 ₁₆	UART4 Special Mode Register	U4SMR	00 ₁₆
02F8 ₁₆	UART4 Transmit/Receive Mode Register	U4MR	00 ₁₆
02F9 ₁₆	UART4 Bit Rate Register	U4BRG	XX ₁₆
02FA ₁₆	UART4 Transmit Buffer Register	U4TB	XX ₁₆
02FB ₁₆			XX ₁₆
02FC ₁₆	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000 ₂
02FD ₁₆	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010 ₂
02FE ₁₆	UART4 Receive Buffer Register	U4RB	XX ₁₆
02FF ₁₆			XX ₁₆
0300 ₁₆	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX ₂
0301 ₁₆			
0302 ₁₆	Timer A1-1 Register	TA11	XX ₁₆
0303 ₁₆			XX ₁₆
0304 ₁₆	Timer A2-1 Register	TA21	XX ₁₆
0305 ₁₆			XX ₁₆
0306 ₁₆	Timer A4-1 Register	TA41	XX ₁₆
0307 ₁₆			XX ₁₆
0308 ₁₆	Three-Phase PWM Control Register 0	INVC0	00 ₁₆
0309 ₁₆	Three-Phase PWM Control Register 1	INVC1	00 ₁₆
030A ₁₆	Three-Phase Output Buffer Register 0	IDB0	XX11 1111 ₂
030B ₁₆	Three-Phase Output Buffer Register 1	IDB1	XX11 1111 ₂
030C ₁₆	Dead Time Timer	DTT	XX ₁₆
030D ₁₆	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XX ₁₆
030E ₁₆			
030F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0310 ₁₆ 0311 ₁₆	Timer B3 Register	TB3	XX ₁₆ XX ₁₆
0312 ₁₆ 0313 ₁₆	Timer B4 Register	TB4	XX ₁₆ XX ₁₆
0314 ₁₆ 0315 ₁₆	Timer B5 Register	TB5	XX ₁₆ XX ₁₆
0316 ₁₆			
0317 ₁₆			
0318 ₁₆			
0319 ₁₆			
031A ₁₆			
031B ₁₆	Timer B3 Mode Register	TB3MR	00XX 0000 ₂
031C ₁₆	Timer B4 Mode Register	TB4MR	00XX 0000 ₂
031D ₁₆	Timer B5 Mode Register	TB5MR	00XX 0000 ₂
031E ₁₆			
031F ₁₆	External Interrupt Request Source Select Register	IFSR	00 ₁₆
0320 ₁₆			
0321 ₁₆			
0322 ₁₆			
0323 ₁₆			
0324 ₁₆	UART3 Special Mode Register 4	U3SMR4	00 ₁₆
0325 ₁₆	UART3 Special Mode Register 3	U3SMR3	00 ₁₆
0326 ₁₆	UART3 Special Mode Register 2	U3SMR2	00 ₁₆
0327 ₁₆	UART3 Special Mode Register	U3SMR	00 ₁₆
0328 ₁₆	UART3 Transmit/Receive Mode Register	U3MR	00 ₁₆
0329 ₁₆	UART3 Bit Rate Register	U3BRG	XX ₁₆
032A ₁₆ 032B ₁₆	UART3 Transmit Buffer Register	U3TB	XX ₁₆ XX ₁₆
032C ₁₆	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000 ₂
032D ₁₆	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010 ₂
032E ₁₆ 032F ₁₆	UART3 Receive Buffer Register	U3RB	XX ₁₆ XX ₁₆
0330 ₁₆			
0331 ₁₆			
0332 ₁₆			
0333 ₁₆			
0334 ₁₆	UART2 Special Mode Register 4	U2SMR4	00 ₁₆
0335 ₁₆	UART2 Special Mode Register 3	U2SMR3	00 ₁₆
0336 ₁₆	UART2 Special Mode Register 2	U2SMR2	00 ₁₆
0337 ₁₆	UART2 Special Mode Register	U2SMR	00 ₁₆
0338 ₁₆	UART2 Transmit/Receive Mode Register	U2MR	00 ₁₆
0339 ₁₆	UART2 Bit Rate Register	U2BRG	XX ₁₆
033A ₁₆ 033B ₁₆	UART2 Transmit Buffer Register	U2TB	XX ₁₆ XX ₁₆
033C ₁₆	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000 ₂
033D ₁₆	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010 ₂
033E ₁₆ 033F ₁₆	UART2 Receive Buffer Register	U2RB	XX ₁₆ XX ₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0340 ₁₆	Count Start Flag	TABSR	00 ₁₆
0341 ₁₆	Clock Prescaler Reset Flag	CPSRF	0XXX XXXX ₂
0342 ₁₆	One-Shot Start Flag	ONSF	00 ₁₆
0343 ₁₆	Trigger Select Register	TRGSR	00 ₁₆
0344 ₁₆	Up/Down Flag	UDF	00 ₁₆
0345 ₁₆			
0346 ₁₆ 0347 ₁₆	Timer A0 Register	TA0	XX ₁₆ XX ₁₆
0348 ₁₆ 0349 ₁₆	Timer A1 Register	TA1	XX ₁₆ XX ₁₆
034A ₁₆ 034B ₁₆	Timer A2 Register	TA2	XX ₁₆ XX ₁₆
034C ₁₆ 034D ₁₆	Timer A3 Register	TA3	XX ₁₆ XX ₁₆
034E ₁₆ 034F ₁₆	Timer A4 Register	TA4	XX ₁₆ XX ₁₆
0350 ₁₆ 0351 ₁₆	Timer B0 Register	TB0	XX ₁₆ XX ₁₆
0352 ₁₆ 0353 ₁₆	Timer B1 Register	TB1	XX ₁₆ XX ₁₆
0354 ₁₆ 0355 ₁₆	Timer B2 Register	TB2	XX ₁₆ XX ₁₆
0356 ₁₆	Timer A0 Mode Register	TA0MR	00 ₁₆
0357 ₁₆	Timer A1 Mode Register	TA1MR	00 ₁₆
0358 ₁₆	Timer A2 Mode Register	TA2MR	00 ₁₆
0359 ₁₆	Timer A3 Mode Register	TA3MR	00 ₁₆
035A ₁₆	Timer A4 Mode Register	TA4MR	00 ₁₆
035B ₁₆	Timer B0 Mode Register	TB0MR	00XX 0000 ₂
035C ₁₆	Timer B1 Mode Register	TB1MR	00XX 0000 ₂
035D ₁₆	Timer B2 Mode Register	TB2MR	00XX 0000 ₂
035E ₁₆	Timer B2 Special Mode Register	TB2SC	XXXX XXX0 ₂
035F ₁₆	Count Source Prescaler Register ⁽¹⁾	TCSPPR	0XXX 0000 ₂
0360 ₁₆			
0361 ₁₆			
0362 ₁₆			
0363 ₁₆			
0364 ₁₆	UART0 Special Mode Register 4	U0SMR4	00 ₁₆
0365 ₁₆	UART0 Special Mode Register 3	U0SMR3	00 ₁₆
0366 ₁₆	UART0 Special Mode Register 2	U0SMR2	00 ₁₆
0367 ₁₆	UART0 Special Mode Register	U0SMR	00 ₁₆
0368 ₁₆	UART0 Transmit/Receive Mode Register	U0MR	00 ₁₆
0369 ₁₆	UART0 Bit Rate Register	U0BRG	XX ₁₆
036A ₁₆ 036B ₁₆	UART0 Transmit Buffer Register	U0TB	XX ₁₆ XX ₁₆
036C ₁₆	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000 ₂
036D ₁₆	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010 ₂
036E ₁₆ 036F ₁₆	UART0 Receive Buffer Register	U0RB	XX ₁₆ XX ₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTE:

1. The TCSPPR register maintains values set before reset, even after software reset or watchdog timer reset has been performed.

Address	Register	Symbol	Value after RESET
0370 ₁₆			
0371 ₁₆			
0372 ₁₆			
0373 ₁₆			
0374 ₁₆			
0375 ₁₆			
0376 ₁₆			
0377 ₁₆			
0378 ₁₆	DMA0 Request Source Select Register	DM0SL	0X00 0000 ₂
0379 ₁₆	DMA1 Request Source Select Register	DM1SL	0X00 0000 ₂
037A ₁₆	DMA2 Request Source Select Register	DM2SL	0X00 0000 ₂
037B ₁₆	DMA3 Request Source Select Register	DM3SL	0X00 0000 ₂
037C ₁₆	CRC Data Register	CRCD	XX ₁₆
037D ₁₆			XX ₁₆
037E ₁₆	CRC Input Register	CRCIN	XX ₁₆
037F ₁₆			
0380 ₁₆	A/D0 Register 0	AD00	XXXX XXXX ₂
0381 ₁₆			0000 0000 ₂
0382 ₁₆	A/D0 Register 1	AD01	XX ₁₆
0383 ₁₆			XX ₁₆
0384 ₁₆	A/D0 Register 2	AD02	XX ₁₆
0385 ₁₆			XX ₁₆
0386 ₁₆	A/D0 Register 3	AD03	XX ₁₆
0387 ₁₆			XX ₁₆
0388 ₁₆	A/D0 Register 4	AD04	XX ₁₆
0389 ₁₆			XX ₁₆
038A ₁₆	A/D0 Register 5	AD05	XX ₁₆
038B ₁₆			XX ₁₆
038C ₁₆	A/D0 Register 6	AD06	XX ₁₆
038D ₁₆			XX ₁₆
038E ₁₆	A/D0 Register 7	AD07	XX ₁₆
038F ₁₆			XX ₁₆
0390 ₁₆			
0391 ₁₆			
0392 ₁₆			
0393 ₁₆			
0394 ₁₆	A/D0 Control Register 2	AD0CON2	XX0X XXX0 ₂
0395 ₁₆	A/D0 Control Register 3	AD0CON3	XXXX X000 ₂
0396 ₁₆	A/D0 Control Register 0	AD0CON0	00 ₁₆
0397 ₁₆	A/D0 Control Register 1	AD0CON1	00 ₁₆
0398 ₁₆	D/A Register 0	DA0	XX ₁₆
0399 ₁₆			
039A ₁₆	D/A Register 1	DA1	XX ₁₆
039B ₁₆			
039C ₁₆	D/A Control Register	DACON	XXXX XX00 ₂
039D ₁₆			
039E ₁₆			
039F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Table 5.2 Recommended Operating Conditions
(V_{CC1}= V_{CC2}=3.0V to 5.5V at Topr=– 20 to 85°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V _{CC1} , V _{CC2}	Supply Voltage (V _{CC1} ≥ V _{CC2})		3.0	5.0	5.5	V
AV _{CC}	Analog Supply Voltage			V _{CC1}		V
V _{SS}	Supply Voltage			0		V
AV _{SS}	Analog Supply Voltage			0		V
V _{IH}	Input High ("H") Voltage	P20-P27, P30-P37, P40-P47, P50-P57	0.8V _{CC2}		V _{CC2}	V
		P60-P67, P72-P77, P80-P87 ⁽³⁾ , P90-P97, P100-P107, X _{IN} , RESET, CNV _{SS} , BYTE	0.8V _{CC1}		V _{CC1}	
		P70, P71	0.8V _{CC1}		6.0	
		P00-P07, P10-P17 (in single-chip mode)	0.8V _{CC2}		V _{CC2}	
		P00-P07, P10-P17 (in memory expansion mode and microprocessor mode)	0.5V _{CC2}		V _{CC2}	
V _{IL}	Input Low ("L") Voltage	P20-P27, P30-P37, P40-P47, P50-P57	0		0.2V _{CC2}	V
		P60-P67, P70-P77, P80-P87 ⁽³⁾ , P90-P97, P100-P107, X _{IN} , RESET, CNV _{SS} , BYTE	0		0.2V _{CC1}	
		P00-P07, P10-P17 (in single-chip mode)	0		0.2V _{CC2}	
		P00-P07, P10-P17 (in memory expansion mode and microprocessor mode)	0		0.16V _{CC2}	
I _{OH(peak)}	Peak Output High ("H") Current ⁽²⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107			-10.0	mA
I _{OH(avg)}	Average Output High ("H") Current ⁽¹⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107			-5.0	mA
I _{OL(peak)}	Peak Output Low ("L") Current ⁽²⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107			10.0	mA
I _{OL(avg)}	Average Output Low ("L") Current ⁽¹⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107			5.0	mA

NOTES:

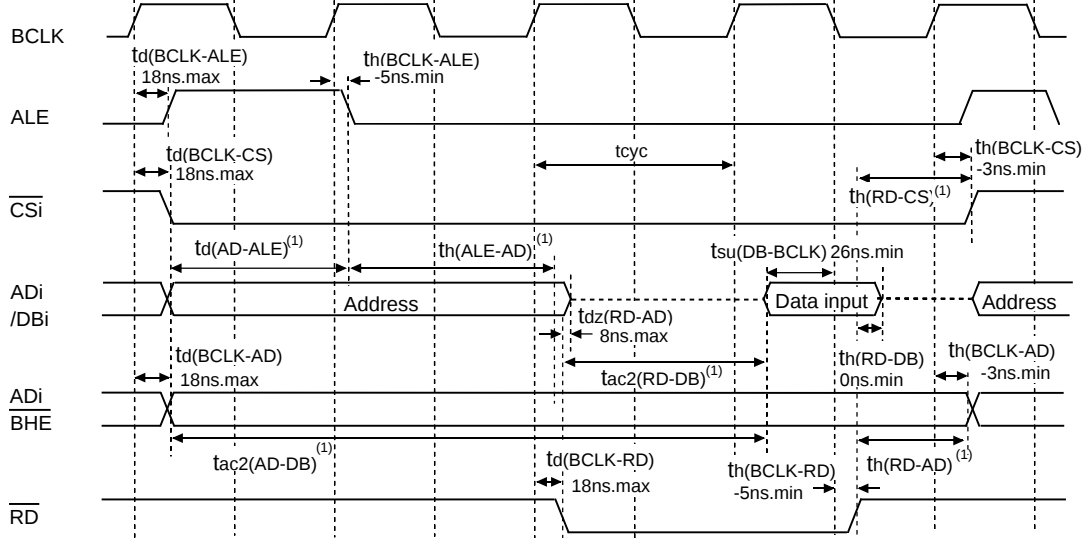
- Typical values when average output current is 100 ms.
- Total I_{OL(peak)} for P0, P1, P2, P86, P87, P9, and P10 must be 80 mA or less.
 Total I_{OL(peak)} for P3, P4, P5, P6, P7, and P80 to P84 must be 80 mA or less.
 Total I_{OH(peak)} for P0, P1, and P2 must be -40 mA or less.
 Total I_{OH(peak)} for P86, P87, P9, and P10 must be -40 mA or less.
 Total I_{OH(peak)} for P3, P4, and P5 must be -40 mA or less.
 Total I_{OH(peak)} for P6, P7, and P80 to P84 must be -40 mA or less.
- V_{IH} and V_{IL} reference for P87 applies when P87 is used as a programmable input port.
 It does not apply when P87 is used as X_{CIN}.

Memory Expansion Mode and Microprocessor Mode

(when accessing an external memory space with the multiplexed bus)

V_{CC1}=V_{CC2}=5V

[Read Timing] (2φ + 2φ Bus Cycle)



NOTE:

1. Varies with operation frequency:

$t_d(\text{AD-ALE}) = (t_{cyc}/2 \times n - 20)\text{ns.min}$ (if external bus cycle is $a\phi + b\phi$, $n=a$)

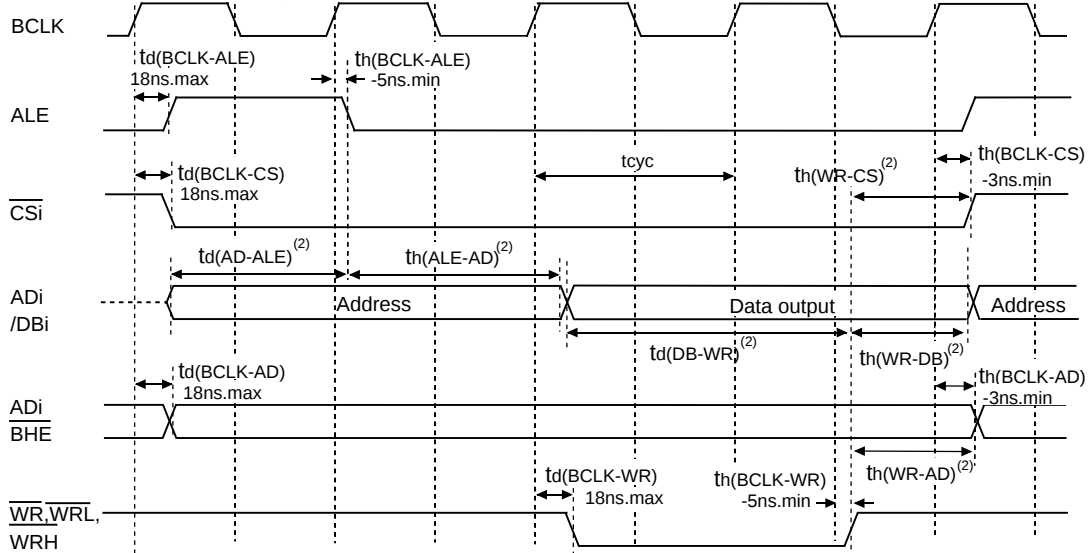
$t_h(\text{ALE-AD}) = (t_{cyc}/2 \times n - 10)\text{ns.min}$ (if external bus cycle is $a\phi + b\phi$, $n=a$)

$t_h(\text{RD-AD}) = (t_{cyc}/2 - 10)\text{ns.min}$, $t_h(\text{RD-CS}) = (t_{cyc}/2 - 10)\text{ns.min}$

$t_{ac2}(\text{RD-DB}) = (t_{cyc}/2 \times m - 35)\text{ns.max}$ (if external bus cycle is $a\phi + b\phi$, $m=(b \times 2) - 1$)

$t_{ac2}(\text{AD-DB}) = (t_{cyc}/2 \times p - 35)\text{ns.max}$ (if external bus cycle is $a\phi + b\phi$, $p=\{(a+b-1) \times 2\} + 1$)

[Write Timing] (2φ + 2φ Bus Cycle)



NOTE:

2. Varies with operation frequency:

$t_d(\text{AD-ALE}) = (t_{cyc}/2 \times n - 20)\text{ns.min}$

(if external bus cycle is $a\phi + b\phi$, $n=a$)

$t_h(\text{ALE-AD}) = (t_{cyc}/2 \times n - 10)\text{ns.min}$

(if external bus cycle is $a\phi + b\phi$, $n=a$)

$t_h(\text{WR-AD}) = (t_{cyc}/2 - 10)\text{ns.min}$,

$t_h(\text{WR-CS}) = (t_{cyc}/2 - 10)\text{ns.min}$, $t_h(\text{WR-DB}) = (t_{cyc}/2 - 10)\text{ns.min}$

$t_d(\text{DB-WR}) = (t_{cyc}/2 \times m - 25)\text{ns.min}$

(if external bus cycle is $a\phi + b\phi$, $m=(b \times 2) - 1$)

Measurement Conditions:

• V_{CC1}=V_{CC2}=4.2 to 5.5V

• Input high and low voltage:

V_{IH}=2.5V, V_{IL}=0.8V

• Output high and low voltage:

V_{OH}=2.0V, V_{OL}=0.8V

$t_{cyc} = \frac{10^9}{f(\text{BCLK})}$

Figure 5.3 V_{CC1}=V_{CC2}=5V Timing Diagram (2)

$$V_{CC1}=V_{CC2}=3.3V$$

Table 5.22 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}=3.0$ to $3.6V$, $V_{SS}=AV_{SS}=0V$ at $T_{opr} = -20$ to $85^{\circ}C$, $f(BCLK) = 24MHz$ unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
-	Resolution		$V_{REF}=V_{CC1}$			10	Bits
INL	Integral Nonlinearity Error	No S&H (8-bit)	$V_{CC1}=V_{CC2}=V_{REF}=3.3V$			± 2	LSB
DNL	Differential Nonlinearity Error	No S&H (8-bit)				± 1	LSB
-	Offset Error	No S&H (8-bit)				± 2	LSB
-	Gain Error	No S&H (8-bit)				± 2	LSB
RLADDER	Resistor Ladder		$V_{REF}=V_{CC1}$	8.0		40	k Ω
tCONV	8-bit Conversion Time ^(1, 2)			6.1			μs
VREF	Reference Voltage			3.3		V_{CC1}	V
VIA	Analog Input Voltage			0		V_{REF}	V

S&H: Sample and Hold

NOTES:

1. Divide $f(X_{IN})$, if exceeding 10 MHz, to keep ϕAD frequency at 10 MHz or less.
2. S&H not available.

Table 5.23 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}=3.0$ to $3.6V$, $V_{SS}=AV_{SS}=0V$ at $T_{opr} = -20$ to $85^{\circ}C$, $f(BCLK) = 24MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
tsu	Setup Time				3	μs
Ro	Output Resistance		4	10	20	k Ω
IvREF	Reference Power Supply Input Current	(Note 1)			1.0	mA

NOTE:

1. Measurement results when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00₁₆". The resistor ladder in the A/D converter is excluded.
IvREF flows even if the VCUT bit in the AD0CON1 register is set to "0" (no VREF connection).

$$V_{CC1}=V_{CC2}=3.3V$$

Timing Requirements

($V_{CC1}=V_{CC2}=3.0$ to $3.6V$, $V_{SS}=0V$ at $T_{opr}=-20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.31 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{W(TBH)}$	TBiIN Input High ("H") Width (counted on one edge)	40		ns
$t_{W(TBL)}$	TBiIN Input Low ("L") Width (counted on one edge)	40		ns
$t_{C(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{W(TBH)}$	TBiIN Input High ("H") Width (counted on both edges)	80		ns
$t_{W(TBL)}$	TBiIN Input Low ("L") Width (counted on both edges)	80		ns

Table 5.32 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{W(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{W(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 5.33 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{W(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{W(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 5.34 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(AD)}$	$\overline{AD_{TRG}}$ Input Cycle Time (required for trigger)	1000		ns
$t_{W(ADL)}$	$\overline{AD_{TRG}}$ Input Low ("L") Width	125		ns

Table 5.35 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(CK)}$	CLKi Input Cycle Time	200		ns
$t_{W(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{W(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.36 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{W(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

$$V_{CC1}=V_{CC2}=3.3V$$

Switching Characteristics

($V_{CC1}=V_{CC2}=3.0$ to $3.6V$, $V_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.37 Memory Expansion Mode and Microprocessor Mode
(when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.1		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-3		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 2)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

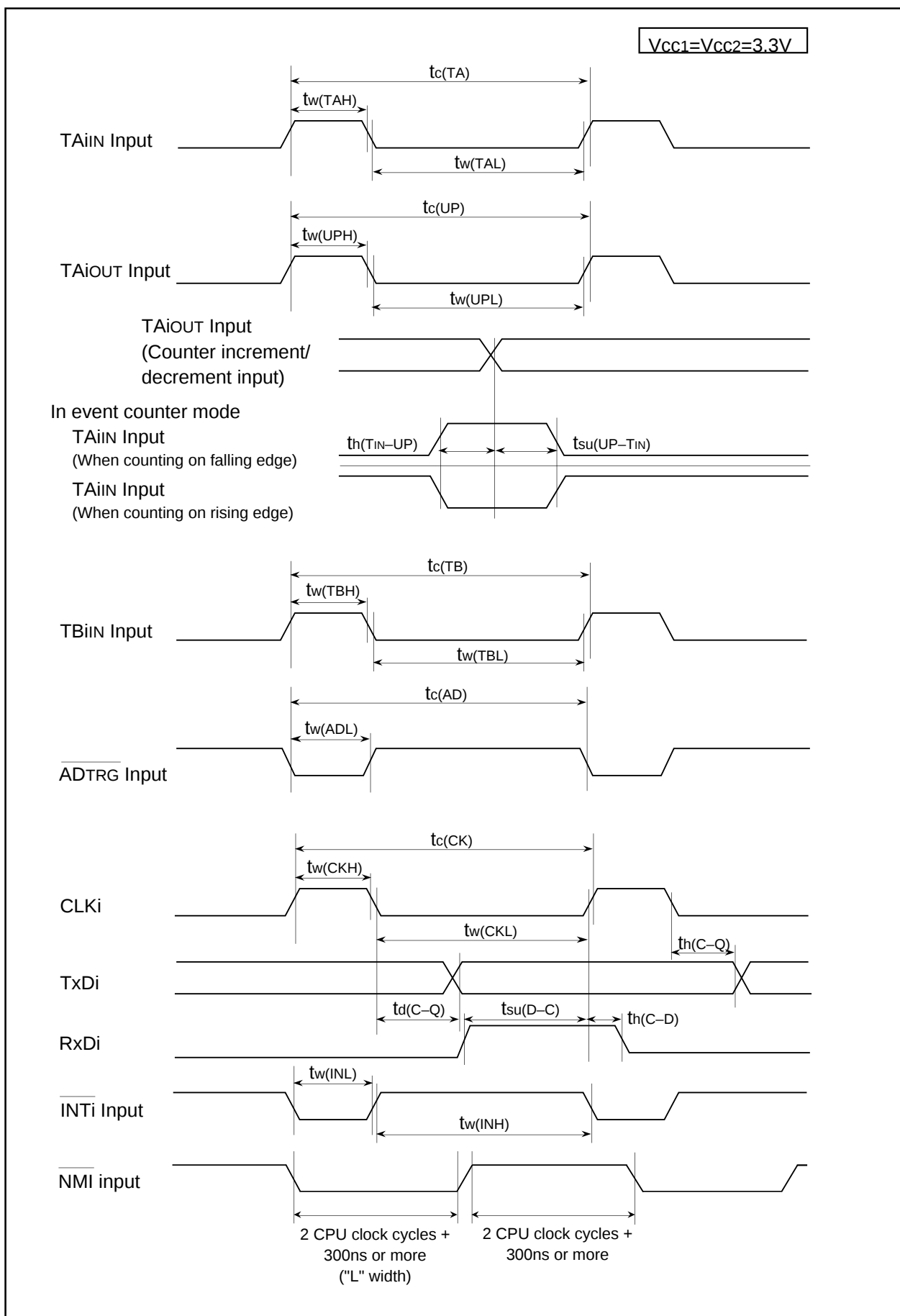
$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

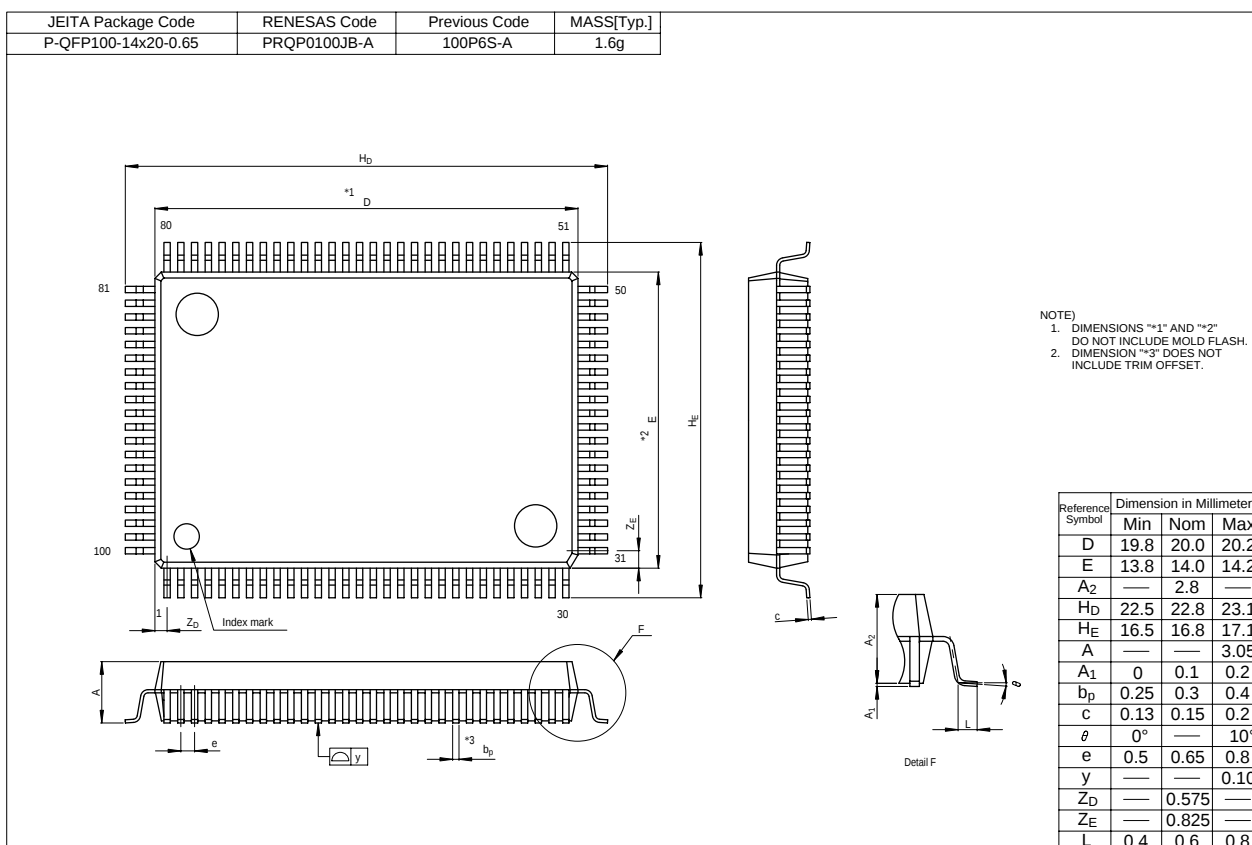
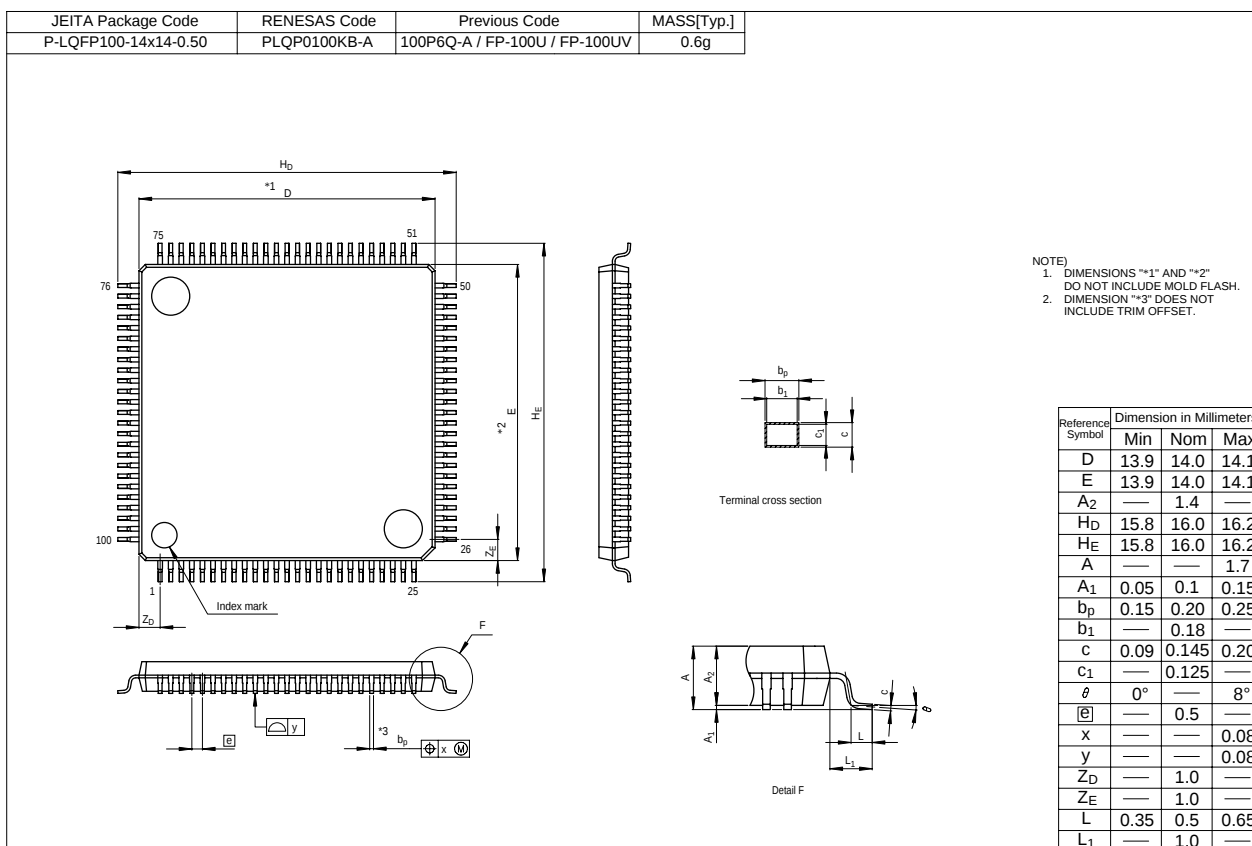
2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n=(b \times 2)-1)$$

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, m=b)$$

Figure 5.8 $V_{CC1}=V_{CC2}=3.3V$ Timing Diagram (3)

Package Dimensions



REVISION HISTORY	M32C/80 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.10	Sep., 02	–	New Document
0.11	Sep., 02	3	Table 1.1.1 "CAN" deleted
0.12	Nov., 02	3	Table 1.1.1 "4.2 to 5.5V" --> "3.0 to 5.5V" "3.0 to 3.6V (f(XIN)=20MHz without software wait)" deleted "26mA (f(XIN)=20MHz without software wait,Vcc=3.3V)" deleted
0.30	Aug., 02	–	1. Overview 1.2 Performance Outline 1.3 Block Diagram 1.5 Pin Assignments Table 1.3 Pin Characteristics for 100-Pin Package 1.6 Pin Description 2. Central Processing Unit (CPU) 3. Memory 4. Special Function Registers (SFR) changed changed added changed changed added added added added
0.40	Jun., 04	All pages	Words standardized: On-chip oscillator, A/D converter and D/A converter
1.00	Nov., 04	2, 3 4 5 11 23 16- 16 29	Overview • Table 1.1 and 1.2 M32C/80 Group Performance "When using 16-bit bus" added to I/O ports "Option" deleted from Serial I/O, I²C bus, and IEBus "Voltage Detection Circuit" added Value added to "Power Consumption" "Flash Memory" added • 1.3 Block Diagram Description deleted • Figure 1.2 ROM/RAM Capacity deleted • Table 1.3 M32C/85 Group Note1 deleted • Table 1.5 Pin Description Note 1 added to I/O ports Memory • Chapter Description modified • Figure 3.1 Memory Map modified SFR • "X: Nothing is assigned" modified to "X: Indeterminate" • "?: Indeterminate" modified to "X: Indeterminate" • "Users cannot use any symbols with *" deleted • Register names, symbols, value after RESET of addresses 0017₁₆, 001B₁₆, 001F₁₆, 002B₁₆, 002F₁₆, 004C₁₆, and 004D₁₆ deleted • Value after RESET in the PM0 register revised • Note 3 deleted • Note 1 added to addresses 03E0₁₆ to 03EB₁₆

