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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	25MHz
Connectivity	I²C, Serial I/O, UART/USART
Peripherals	LCD, PWM, WDT
Number of I/O	70
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f809spf-g-jne1

FUJITSU MICROELECTRONICS
DATA SHEET

DS07-13733-6E

16-bit Microcontroller

CMOS

F²MC-16LX MB90800 Series

MB90803/803S/F803/F803S/F804-101/ MB90F804-201/F809/F809S/V800

■ DESCRIPTION

The MB90800 series is a general-purpose 16-bit microcontroller that has been developed for high-speed real-time processing required for industrial and office automation equipment and process control, etc. The LCD controller of 48 segment four common is built into.

Instruction set has taken over the same AT architecture as in the F²MC-8L and F²MC-16L, and is further enhanced to support high level languages, extend addressing mode, enhanced divide/multiply instructions with sign and enrichment of bit processing. In addition, long word processing is now available by introducing a 32-bit accumulator.

Note: F²MC is the abbreviation of Fujitsu Flexible Microcontroller.

■ FEATURES

- **Clock**
  - Built-in PLL clock frequency multiplication circuit
  - Operating clock (PLL clock) : divided-by-2 of oscillation (at oscillation of 6.25 MHz) or 1 to 4 times the oscillation (at oscillation of 6.25 MHz to 25 MHz).
  - Minimum instruction execution time of 40.0 ns (at oscillation of 6.25 MHz, four times the PLL clock, operation at Vcc = 3.3 V)
- **The maximum memory space:16 Mbytes**
  - 24-bit internal addressing
  - Bank addressing

(Continued)

For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

2009.9

■ PRODUCT LINEUP

Item \ Part number	MB90V800-101/201	MB90F804-101/201	MB90803/MB90803S	MB90F803/MB90F803S	MB90F809/MB90F809S
Type	Evaluation product	Flash memory products	Mask ROM products	Flash memory products	
System clock	On-chip PLL clock multiplication method(× 1, × 2, × 3, × 4, 1/2 when PLL stops) Minimum instruction execution time of 40.0 ns (at oscillation of 6.25 MHz, four times the PLL clock)				
Sub clock	With sub clock: 201 option Without sub clock: 101 option		With sub clock: Part number of products without "S" suffix Without sub clock: Part number of products with "S" suffix		
ROM capacity	No	256 Kbytes	128 Kbytes	128 Kbytes dual operation	192 Kbytes
RAM capacity	28 Kbytes	16 Kbytes	4 Kbytes	4 Kbytes	10 Kbytes
CPU functions	Number of basic instructions : 351 Minimum instruction execution time : 40.0 ns/6.25 MHz oscillator (When four times is used : machine clock 25 MHz, Power supply voltage : 3.3 V ± 0.3 V) Addressing type : 23 types Program Patch Function : 2 address pointers The maximum memory space : 16 Mbytes				
Ports	I/O port (CMOS) 68 ports (shared with resources), (70 ports when the subclock is not used)				
LCD controller/driver	Segment driver that can drive the LCD panel (liquid crystal display) directly, and common driver 48 SEG × 4 COM				
16-bit input/output timer — 16-bit free-run timer	1 channel Overflow interrupt				
16-bit input/output timer — Output compare (OCU)	2 channels Pin input factor: matching of the compare register				
16-bit input/output timer — Input capture (ICU)	2 channels Rewriting a register value upon a pin input (rising edge, falling edge, or both edges)				
16-bit Reload Timer	16-bit reload timer operation (toggle output, single shot output selectable) The event count function is optional. The event count function is optional. Three channels are built in.				
16-bit PPG timer	Output pin × 2 ports Operating clock frequency : fcp, fcp/22, fcp/24, fcp/26 Two channels are built in.				
Time-base timer	1 channel				
Watchdog timer	1 channel				
Timer clock output circuit	Clock with a frequency of external input clock divided by 16/32/64/128 can be output externally.				
I^2C bus	I^2C Interface. 1 channel is built-in.				

(Continued)

Pin No.	Pin Name	I/O Circuit Type*	Status/function at reset	Function
7	SEG38	E	Port input (High-Z)	A segment output terminal of the LCD controller/ driver.
	P32			General purpose input/output port.
	SI3			Serial data input pin of serial I/O ch.3. This pin may be used during serial I/O ch.3 in input mode, so it cannot use as other pin function.
8	SEG39	E		A segment output terminal of the LCD controller/ driver.
	P33			General purpose input/output port.
	TMCK			Timer clock output pin. It is effective when permitting the power output.
9, 10	SEG40, SEG41	E		A segment output terminal of the LCD controller/ driver.
	P34, P35			General purpose input/output port.
	IC0, IC1			External trigger input pin of input capture ch.0/ch.1.
11, 12	SEG42, SEG43	E		A segment output terminal of the LCD controller/ driver.
	P36, P37			General purpose input/output port.
	OCU0, OCU1			Output terminal for the output compares ch.0/ch.1.
17 to 21	LED0 to LED4	F		It is a output terminal for LED (I_{OL} = 15 mA).
	P40 to P44			General purpose input/output port.
22 to 24	LED5 to LED7	F		It is a output terminal for LED (I_{OL} = 15 mA).
	P45 to P47			General purpose input/output port.
	TOT0 to TOT2			External event output pin of reload timer ch.0 to ch.2. It is effective when permitting the external event output.
25, 26	SEG44, SEG45	E		A segment output terminal of the LCD controller/ driver.
	P50, P51			General purpose input/output port.
	TIN0, TIN1			External clock input pin of reload timer ch.0, ch.1. It is effective when permitting the external clock input.

(Continued)

5. Treatment of power supply pins (V_{CC}/V_{SS})

In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect all power supply pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between V_{CC} and V_{SS} near this device.

6. About Crystal oscillators circuit

Noise near the X0/X1 pins and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1 pins and X0A/X1A pins, the crystal oscillator (or the ceramic oscillator) and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended to design the PC board artwork with the X0/X1 pins and X0A/X1A pins surrounded by ground plane because stable operation can be expected with such a layout.

Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

7. Caution on Operations during PLL Clock Mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Fujitsu will not guarantee results of operations if such failure occurs.

8. Stabilization of Supply Power Supply

A sudden change in the supply voltage may cause the device to malfunction even within the V_{CC} supply voltage operating range.Therefore, the V_{CC} supply voltage should be stabilized. For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak- to-peak values) at commercial frequencies (50 Hz/60 Hz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

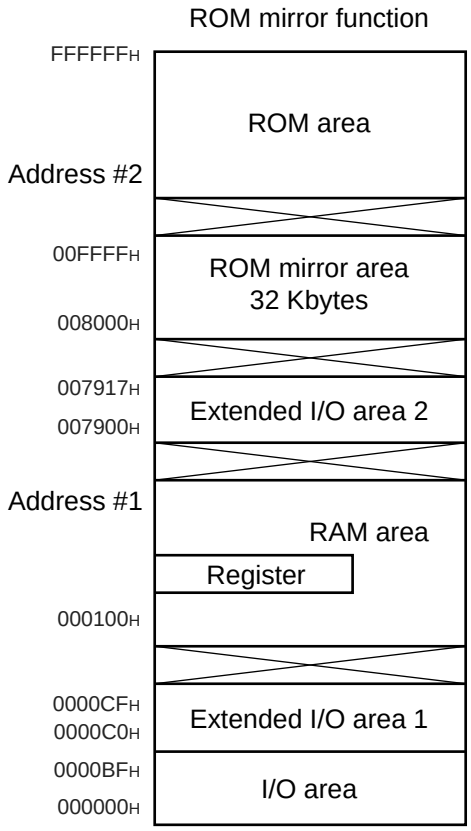
9. Note on Using the two-subsystem product as one-subsystem product

If you are using only one subsystem of the MB90800 series that come in one two-subsystem product, use it with X0A = V_{SS} and X1A = OPEN.

10. Write to FLASH

Ensure that you must write to FLASH at the operating voltage V_{CC} = 3.0 V to 3.6 V.

■ MEMORY MAP



Part number	Address #1	Address #2
MB90803/S, MB90F803/S	0010FFH	FE0000H
MB90F809/S	0028FFH	FD0000H
MB90F804-101/201	0040FFH	FC0000H
MB90V800-101/201	0070FFH	F80000H*

* : ROM is not built into MB90V800.
F80000H is ROM decipherment region on the tool side.

Memory Map of MB90800 Series

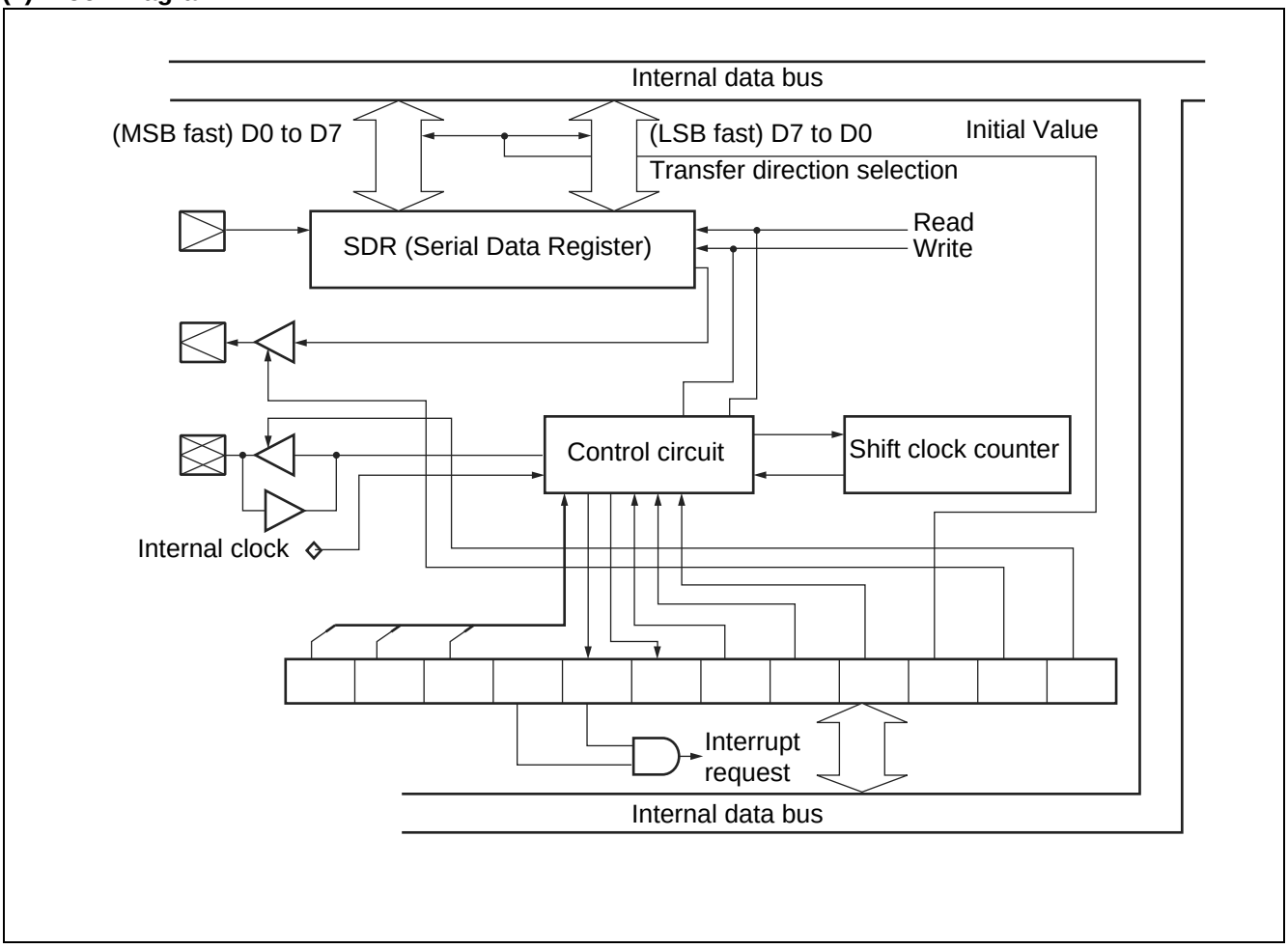
Notes :
- When the ROM mirror function register has been set, the mirror image data at higher addresses (“FF4000H to FFFFFFH”) of bank FF is visible from the higher addresses (“008000H to 00FFFFH”) of bank 00.
- The ROM mirror function is for using the C compiler small model.
- The lower 16-bit addresses of bank FF are equivalent to those of bank 00. Note that because the ROM area of bank FF exceeds.
  32 Kbytes, all data in the ROM area cannot be shown in mirror image in bank 00.
- When the C compiler small model is used, the data table can be shown as mirror image at “008000H to 00FFFFH ”by storing the data table at “FF8000H to FFFFFFH”. Therefore, data tables in the ROM area can be referenced without declaring the far addressing with the pointer.

■ I/O MAP

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000000H	PDR0	Port 0 data register	R/W	Port 0	XXXXXXXXB
000001H	PDR1	Port 1 data register	R/W	Port 1	XXXXXXXXB
000002H	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXXB
000003H	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXXB
000004H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXXB
000005H	PDR5	Port 5 data register	R/W	Port 5	XXXXXXXXB
000006H	PDR6	Port 6 data register	R/W	Port 6	XXXXXXXXB
000007H	PDR7	Port 7 data register	R/W	Port 7	- XXXXXXXB
000008H	PDR8	Port 8 data register	R/W	Port 8	- - - XXXXXB
000009H	PDR9	Port 9 data register	R/W	Port 9	- - - - - - XXB
00000AH to 00000FH	Prohibited				
000010H	DDR0	Port 0 direction register	R/W	Port 0	0 0 0 0 0 0 0 0B
000011H	DDR1	Port 1 direction register	R/W	Port 1	0 0 0 0 0 0 0 0B
000012H	DDR2	Port 2 direction register	R/W	Port 2	0 0 0 0 0 0 0 0B
000013H	DDR3	Port 3 direction register	R/W	Port 3	0 0 0 0 0 0 0 0B
000014H	DDR4	Port 4 direction register	R/W	Port 4	0 0 0 0 0 0 0 0B
000015H	DDR5	Port 5 direction register	R/W	Port 5	0 0 0 0 0 0 0 0B
000016H	DDR6	Port 6 direction register	R/W	Port 6	0 0 0 0 0 0 0 0B
000017H	DDR7	Port 7 direction register	R/W	Port 7	- 0 0 0 0 0 0 0B
000018H	DDR8	Port 8 direction register	R/W	Port 8	- - - 0 0 0 0 0B
000019H	DDR9	Port 9 direction register	R/W	Port 9	- - - - - - 0 0B
00001AH to 00001DH	Prohibited				
00001EH	ADER0	Analog input enable 0 register	R/W	Port 6, A/D	1 1 1 1 1 1 1 1B
00001FH	ADER1	Analog input enable 1 register	R/W	Port 7, A/D	- - - - 1 1 1 1B
000020H	SMR0	Serial mode register	R/W	UART0	0 0 0 0 0 - 0 0B
000021H	SCR0	Serial control register	R/W		0 0 0 0 0 1 0 0B
000022H	SIDR0/ SODR0	Serial input/output register	R/W		XXXXXXXXB
000023H	SSR0	Serial data register	R/W		0 0 0 0 1 0 0 0B
000024H	Prohibited				
000025H	CDCR0	Communication prescaler control register	R/W	Prescaler 0	0 0 - - 0 0 0 0B
000026H	Prohibited				
000027H					

(Continued)

(2) Block Diagram



6. 16 bits PPG

The PPG timer consists of the following:
- Prescaler
- 16-bit down-counter: 1
- 16-bit data register with a cycle setting buffer
- 16-bit compare register with a duty setting buffer
- Pin control unit

The PPG timer can output pulses synchronized to the software trigger.

The output pulse can be changed to any cycle and duty freely by updating the PCSRL, PCSRH/PDUTL, PDUTH registers.

- PWM function

The PPG timer can output pulses programmably by updating the PCSR and PDUT registers described above in synchronization to the trigger.

Can also be used as a D/A converter by an external circuit.

- Single shot function

By detecting an edge of the trigger input, a single pulse can be output.

- 16-bit down counter

The counter operation clock comes from eight kinds optional. There are eight kinds of internal clocks.

(ϕ, ϕ2, ϕ4, ϕ8, ϕ16, ϕ32, ϕ64, ϕ128) ϕ : machine clock

The counter can be initialized to “$FFFF_H$” at a reset or counter borrow.

- Interrupt request

The PPG timer generates an interrupt request when :
- Timer start-up
- Counter borrow occurrence (cycle match)
- Duty match occurrence

7. Delay interrupt generator module

The delayed interrupt generation module outputs an interrupt request for task switching. The hardware interrupt request can be generated by software.

(1) Register list

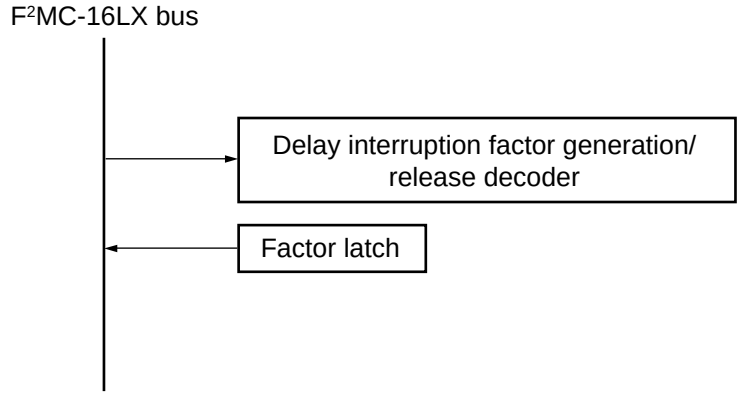
Delayed Interrupt/release register(DIRR)

DIRR Address : 00009F$_H$

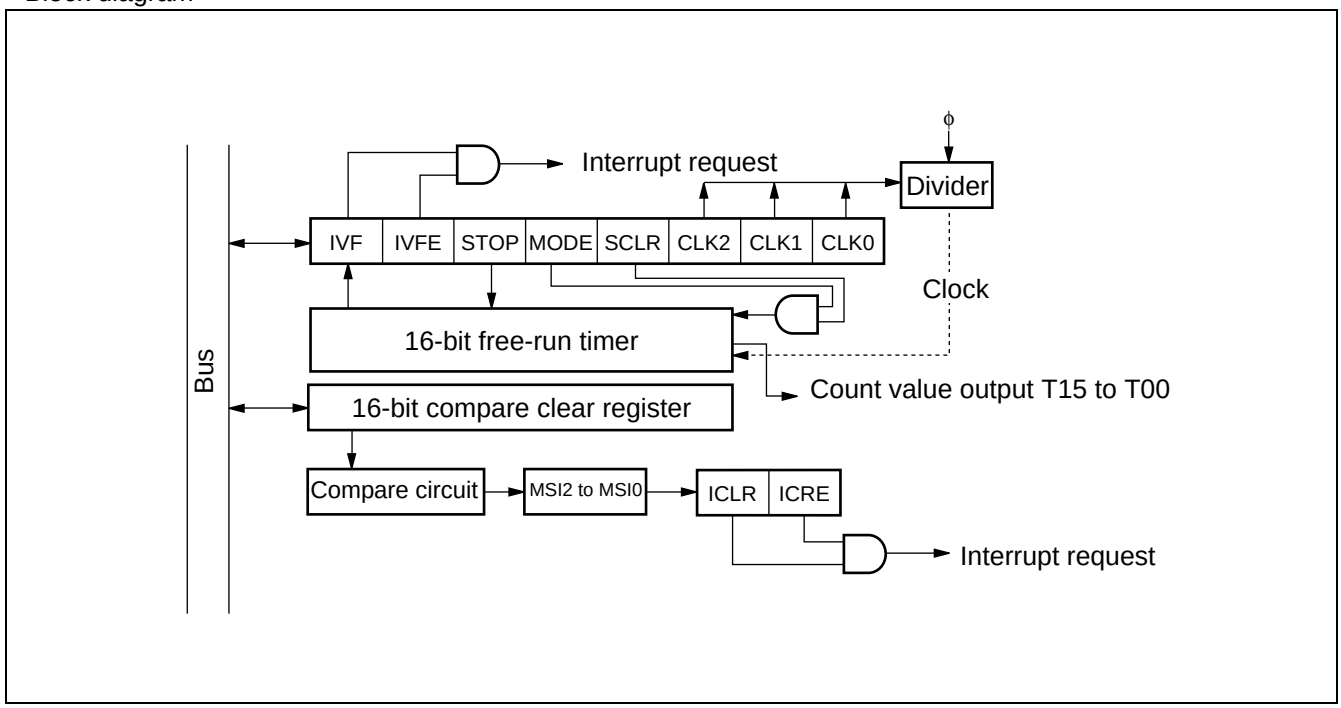
bit	15	14	13	12	11	10	9	8	Initial Value
	—	—	—	—	—	—	—	R0	- - - - - - - 0$_B$
	—	—	—	—	—	—	—	R/W	Read/Write

- : Unused

(2) Block diagram



• Block diagram



(2) Output compare

The output compare consists of 16-bit compare registers, compare output pin part and a control register. It can reverse the output level for the pin and at the same time, generate an interrupt when the 16-bit free-run timer value matches a value set in one of the 16-bit compare registers of this module.

- It has a total of six compare registers that can operate independently. In addition, the output can be set to be controlled by using two compare registers.
- An interrupt can be set by a comparing match.

• Register list

Compare register (OCCP0, OCCP1)

bit	15	14	13	12	11	10	9	8	Initial Value
00004B$_H$ 00004D$_H$	OP15	OP14	OP13	OP12	OP11	OP10	OP09	OP08	00000000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

bit	7	6	5	4	3	2	1	0	Initial Value
00004A$_H$ 00004C$_H$	OP07	OP06	OP05	OP04	OP03	OP02	OP01	C00	00000000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

Control register (OCSH)

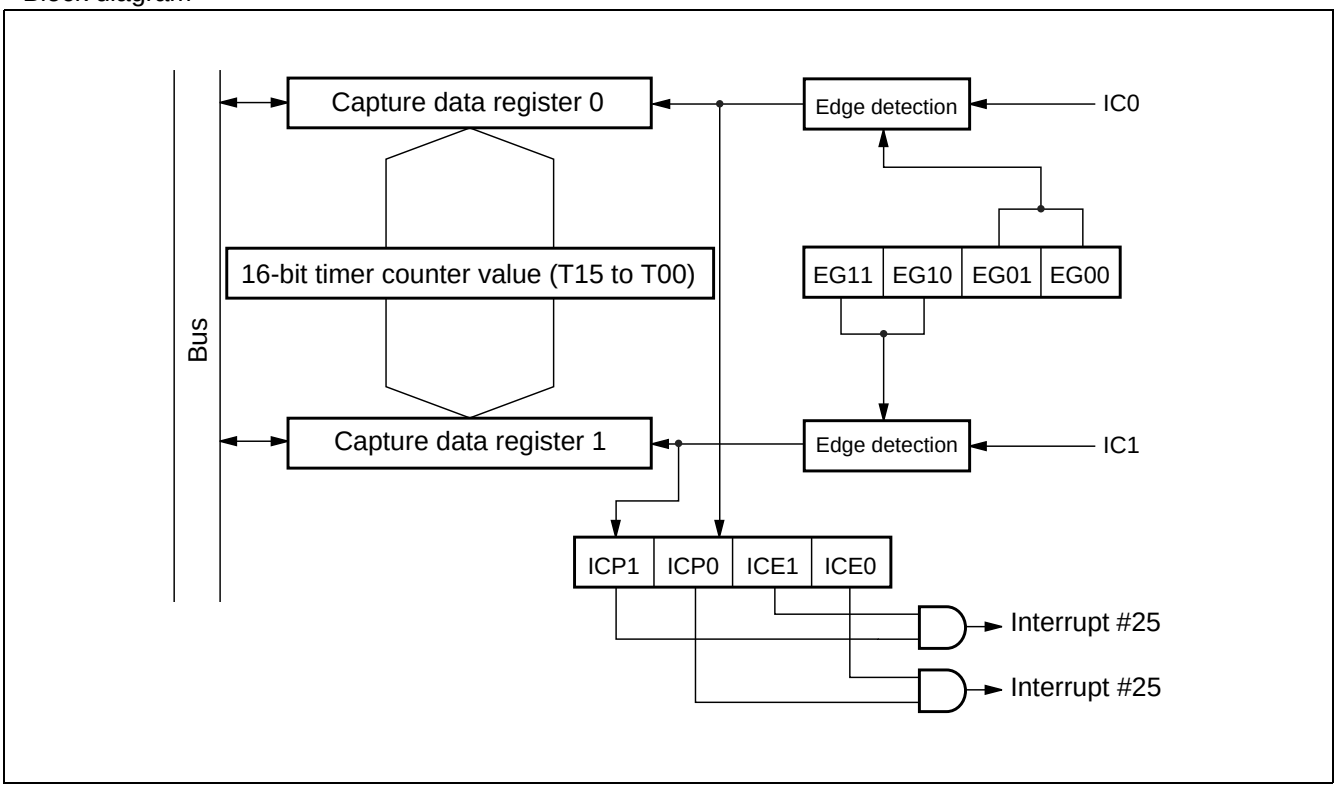
bit	15	14	13	12	11	10	9	8	Initial Value
00004F$_H$	—	—	—	CMOD	OTE1	OTE0	OTD1	OTD0	---00000$_B$
	—	—	—	R/W	R/W	R/W	R/W	R/W	Read/Write

Control register (OCSL)

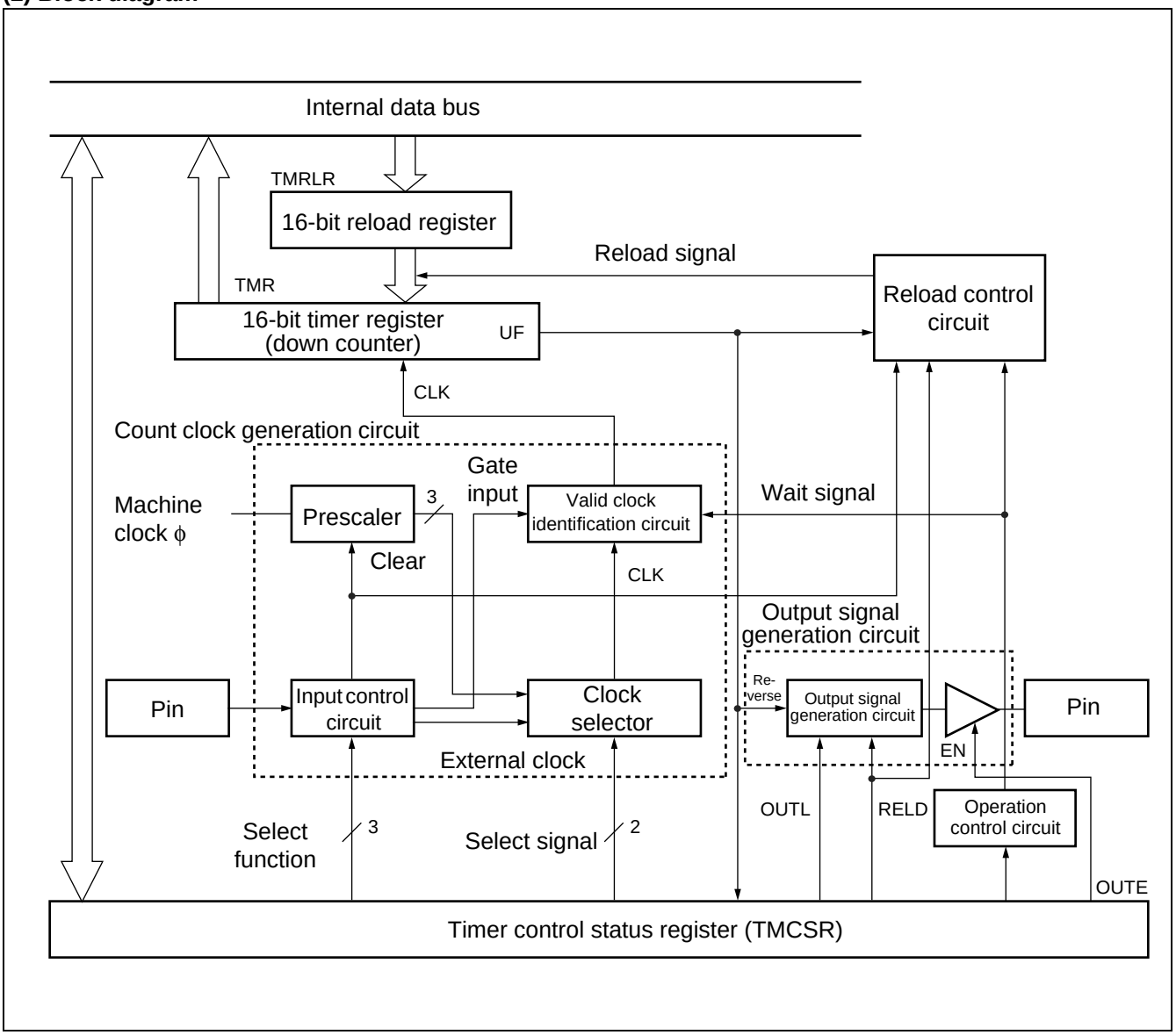
bit	7	6	5	4	3	2	1	0	Initial Value
00004E$_H$	IOP1	IOP0	IOE1	IOE0	—	—	CST1	CST0	0000--00$_B$
	R/W	R/W	R/W	R/W	—	—	R/W	R/W	Read/Write

- : Unused

• Block diagram



(2) Block diagram



15. Low power consumption mode

The low-power consumption mode has the following CPU operation modes by selecting the operation clock and operating the control of the clock.

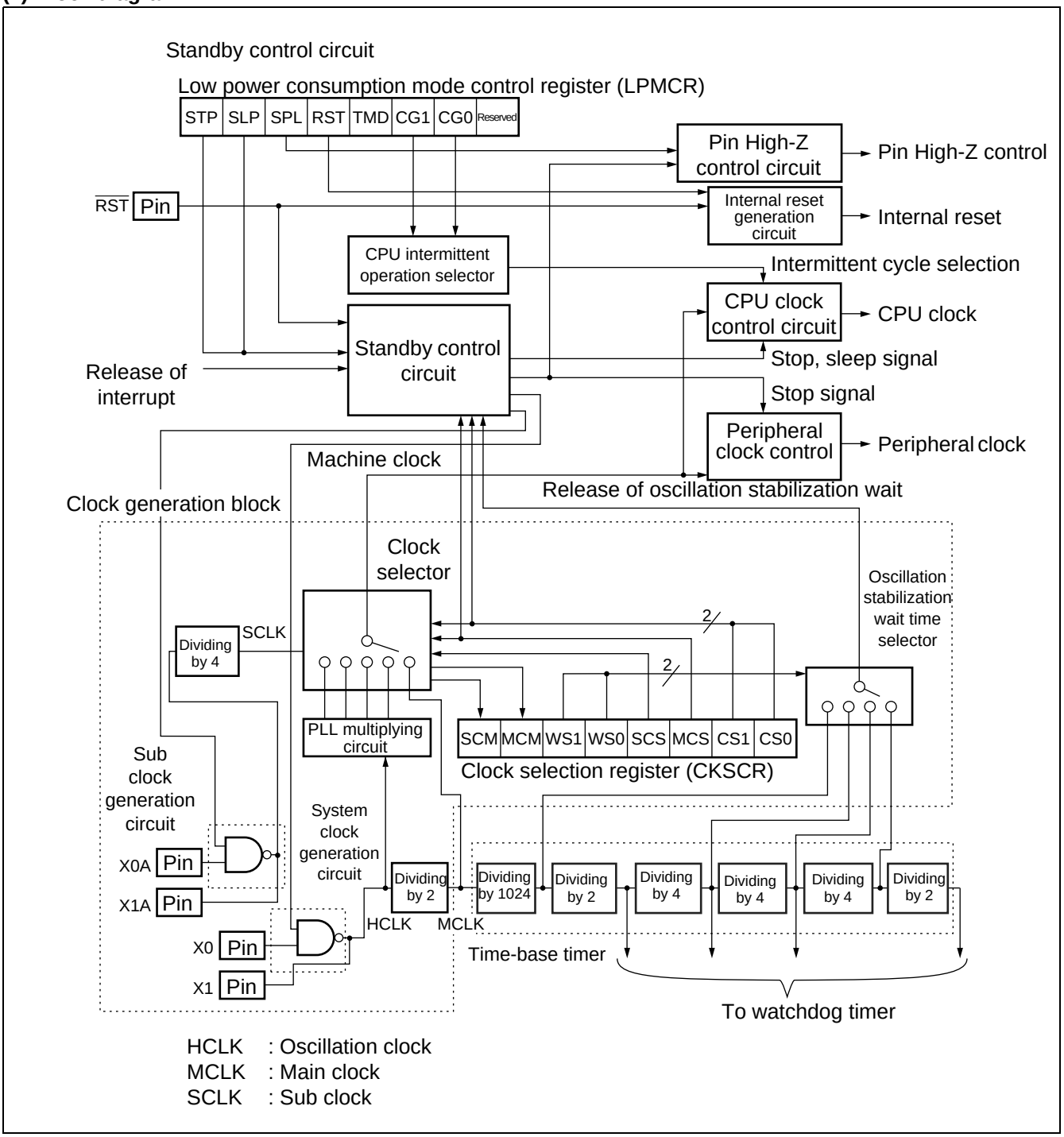
- Clock mode
  (PLL clock mode, main clock mode and sub clock mode)
- CPU intermittent operation mode
  (PLL clock intermittent operation mode, main clock intermittent operation mode and subclock intermittent operation mode)
- Standby mode
  (Sleep mode, time base timer mode, stop mode and watch mode)

(1) Register list

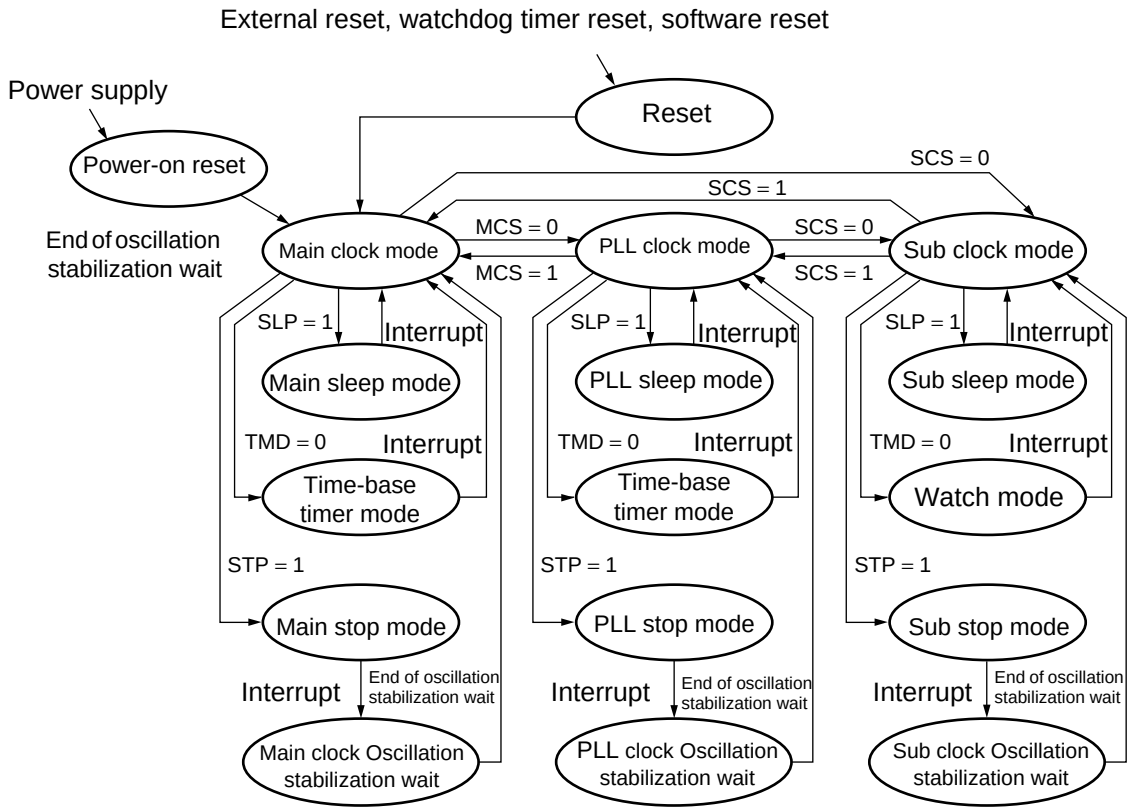
Low power consumption mode control register (LPMCR)

bit	7	6	5	4	3	2	1	0	Initial Value
0000A0H	STP	SLP	SPL	RST	TMD	CG1	CG0	Reserved	00011000B
	W	W	R/W	W	R/W	R/W	R/W	R/W	Read/Write

(2) Block diagram



(3) Figure of status transition



17. ROM mirroring function selection module

ROM mirroring function selection module provides the setting so that ROM data located in FF bank can be read by access to 00 bank.

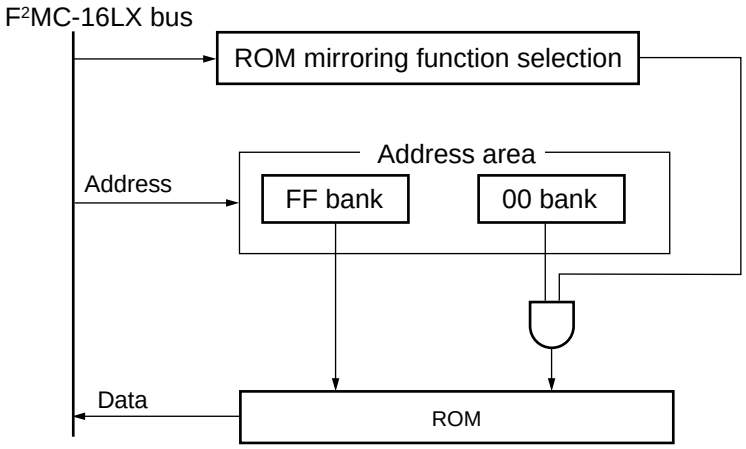
(1) Register list

ROM mirror function select register (ROMM)

bit	15	14	13	12	11	10	9	8	Initial Value
00006F$_H$	—	—	—	—	—	—	—	MI	XXXXXXX1$_B$
	—	—	—	—	—	—	—	R/W	Read/Write

- : Unused

(2) Block diagram



Note : Do not access to ROM mirroring function selection register in the middle of the operation of the address 008000$_H$ to 00FFFF$_H$.

19. LCD controller/driver

The LCD controller/driver contains 24 × 8-bit display data memory and controls the LCD display with four common output lines and 48 segment output lines. Three duty outputs can be selected to directly drive the LCD panel (liquid crystal display).

- Contains an LCD driving voltage split resistor. Moreover, the external division resistance can be connected.
- A maximum of four common output lines (COM0 to COM3) and 48 segment output lines (SEG0 to SEG47) are available.
- Contains 24-byte display data memory (display RAM).
- For the duty, 1/2, 1/3, or 1/4 can be selected (restricted by bias setting).
- The LCD can directly be driven.

Bias	1/2 duty	1/3 duty	1/4 duty
1/2 bias	○	×	×
1/3 bias	×	○	○

○ **: Recommended mode**

× **: Disable**

(1) Register list

• LCDC control register (upper) (LCRH)

bit	15	14	13	12	11	10	9	8	Initial Value
00005D$_H$	SS4	VS0	CS1	CS0	SS3	SS2	SS1	SS0	00000000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

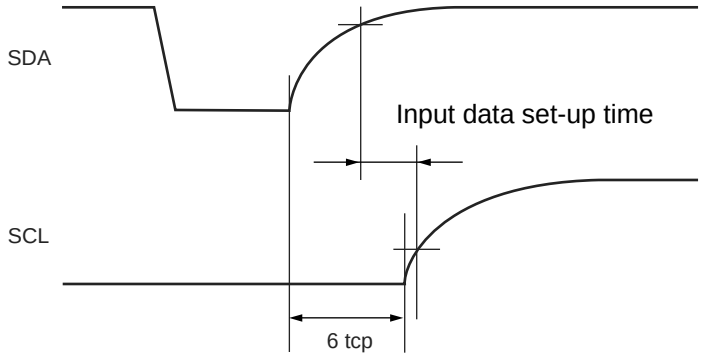
• LCDC control register (lower) (LCRL)

bit	7	6	5	4	3	2	1	0	Initial Value
00005C$_H$	CSS	LCEN	VSEL	BK	MS1	MS0	FP1	FP0	00010000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

• LCDC range register (LCRR)

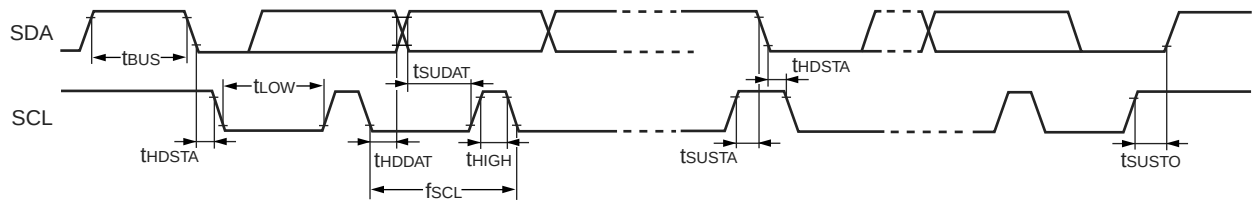
bit	7	6	5	4	3	2	1	0	Initial Value
00005E$_H$	Reserved	Reserved	SE4	SE3	SE2	SE1	SE0	LCR	00000000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

• Note of SDA and SCL set-up time



Note : The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.
Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.

• Timing definition

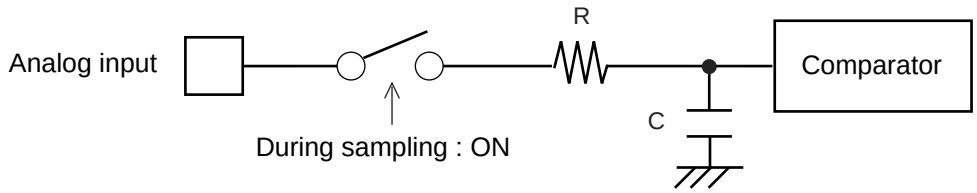


(2) Notes on Using A/D Converter

- **About the external impedance of analog input and its sampling time**

A/D converter with sample & hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relation-ship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. And, if the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- Analog input circuit model

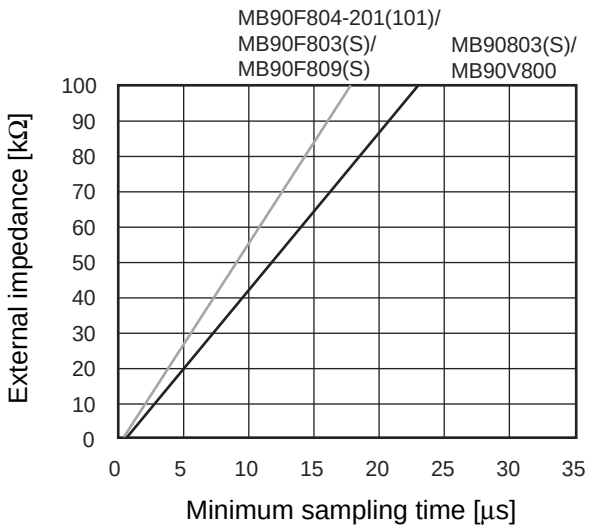


	R	C
MB90803 (S)	1.9 kΩ (Max)	32.3 pF (Max)
MB90F804-201(101)/F803(S)/F809(S)	1.9 kΩ (Max)	25.0 pF (Max)
MB90V800	1.9 kΩ (Max)	32.3 pF (Max)

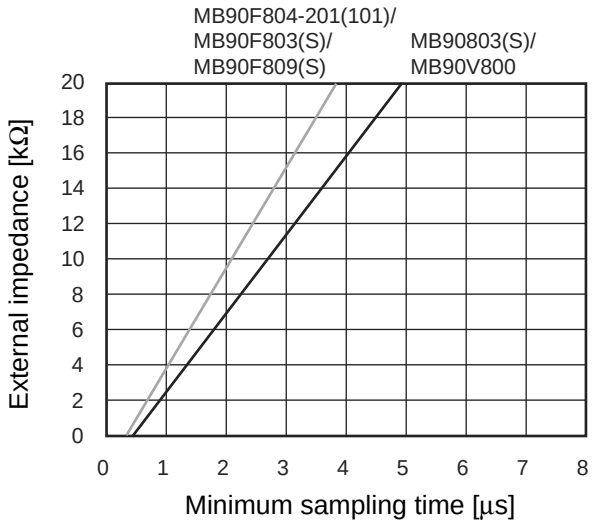
Note : The values are reference values.

- The relationship between external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



- **About errors**

As | AV_{CC} – AV_{SS} | becomes smaller, values of relative errors grow larger.