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What is "Embedded - Microcontrollers"?

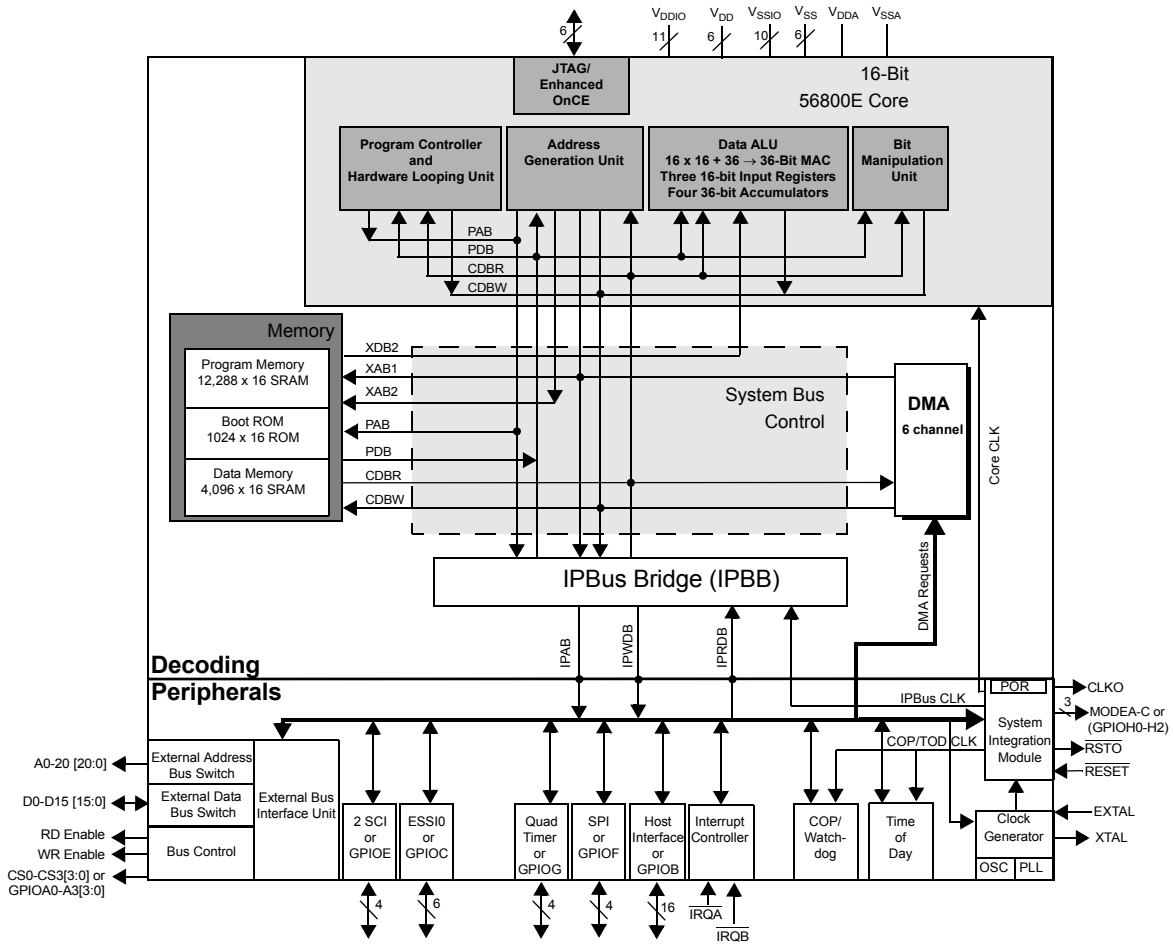
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	56800E
Core Size	16-Bit
Speed	120MHz
Connectivity	EBI/EMI, SCI, SPI, SSI
Peripherals	DMA, POR, WDT
Number of I/O	41
Program Memory Size	24KB (12K x 16)
Program Memory Type	SRAM
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	1.62V ~ 1.98V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56853fge

56853 General Description

- 120 MIPS at 120MHz
- 12K x 16-bit Program SRAM
- 4K x 16-bit Data SRAM
- 1K x 16-bit Boot ROM
- Access up to 2M words of program memory or 8M of data memory
- Chip Select Logic for glue-less interface to ROM and SRAM
- Six (6) independent channels of DMA
- Enhanced Synchronous Serial Interfaces (ESSI)
- Two (2) Serial Communication Interfaces (SCI)
- Serial Port Interface (SPI)
- 8-bit Parallel Host Interface
- General Purpose 16-bit Quad Timer
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Computer Operating Properly (COP)/Watchdog Timer
- Time-of-Day (TOD)
- 128 LQFP package
- Up to 41 GPIO



56853 Block Diagram

Part 1 Overview

1.1 56853 Features

1.1.1 Core

- Efficient 16-bit engine with dual Harvard architecture
- 120 Million Instructions Per Second (MIPS) at 120MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four (4) 36-bit accumulators including extension bits
- 16-bit bidirectional shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three (3) internal address buses and one (1) external address bus
- Four (4) internal data buses and one (1) external data bus
- Instruction set supports both DSP and controller functions
- Four (4) hardware interrupt levels
- Five (5) software interrupt levels
- Controller-style addressing modes and instructions for compact code
- Efficient C Compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced OnCE debug programming interface

1.1.2 Memory

- Harvard architecture permits up to three (3) simultaneous accesses to program and data memory
- On-Chip Memory
  - 12K × 16-bit Program SRAM
  - 4K × 16-bit Data SRAM
  - 1K × 16-bit Boot ROM
- Off-Chip Memory Expansion (EMI)
  - Access up to 2M words of program memory or 8M data memory
  - Chip Select Logic for glue-less interface to ROM and SRAM

1.1.3 Peripheral Circuits for 56853

- General Purpose 16-bit Quad Timer*
- Two (2) Serial Communication Interfaces (SCI)*
- Serial Peripheral Interface (SPI) Port*
- Enhanced Synchronous Serial Interface (ESSI) modules*
- Computer Operating Properly (COP)

- Watchdog Timer
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging
- Six (6) independent channels of DMA
- 8-bit Parallel Host Interface*
- Time-of-Day (TOD)
- 128 LQFP package
- Up to 41 GPIO

* Each peripheral I/O can be used alternately as a General Purpose I/O if not needed

1.1.4 Energy Information

- Fabricated in high-density CMOS with 3.3V, TTL-compatible digital inputs
- Wait and Stop modes available

1.2 56853 Description

The 56853 is a member of the 56800E core-based family of controllers. It combines, on a single chip, the processing power of a Digital Signal Processor (DSP) and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56853 is well-suited for many applications. The 56853 includes many peripherals that are especially useful for low-end Internet appliance applications and low-end client applications such as telephony; portable devices; Internet audio and point-of-sale systems, such as noise suppression; ID tag readers; sonic/subsonic detectors; security access devices; remote metering; sonic alarms.

The 56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C Compilers, enabling rapid development of optimized control applications.

The 56853 supports program execution from either internal or external memories. Two data operands can be accessed from the on-chip Data RAM per instruction cycle. The 56853 also provides two external dedicated interrupt lines, and up to 41 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The 56853 controller includes 12K words of Program RAM, 4K words of Data RAM, and 1K words of Boot ROM. It also supports program execution from external memory. The 56800 core can access two data operands from the on-chip Data RAM per instruction cycle.

This controller also provides a full set of standard programmable peripherals that include an 8-bit parallel Host Interface, Enhanced Synchronous Serial Interface (ESSI), one Serial Peripheral Interface (SPI), the option to select a second SPI or two Serial Communications Interfaces (SCIs), and Quad Timer. The Host Interface, ESSI, SPI, SCI, four chip selects and quad timer can be used as General Purpose Input/Outputs (GPIOs) if its primary function is not required.

1.5 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
“asserted”	A high true (active high) signal is high or a low true (active low) signal is low.
“deasserted”	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:

Signal/Symbol	Logic State	Signal State	Voltage[1]
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for VIL, VOL, VIH, and VOH are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the 56853 are organized into functional groups, as shown in **Table 2-1** and as illustrated in **Figure 2-1**. In **Table 3-1** each table row describes the package pin and the signal or signals present.

Table 2-1 56853 Functional Group Pin Allocations

Functional Group	Number of Pins
Power (V_{DD}, V_{DDIO}, or V_{DDA})	(6, 11, 1)[1]
Ground (V_{SS}, V_{SSIO},or V_{SSA})	(6, 10, 1)[1]
PLL and Clock	3
External Bus Signals	39
External Chip Select*	4
Interrupt and Program Control	7[2]
Host Interface (HI)*	16[3]
Enhanced Synchronous Serial Interface (ESSI0) Port*	6
Serial Communications Interface (SCI0) Ports*	2
Serial Communications Interface (SCI1) Ports*	2
Serial Peripheral Interface (SPI) Port*	4
Quad Timer Module Port*	4
JTAG/Enhanced On-Chip Emulation (EOnCE)	6

*Alternately, GPIO pins

1. V_{DD} = $V_{DD\ CORE}$, V_{SS} = $V_{SS\ CORE}$, V_{DDIO}= $V_{DD\ IO}$, V_{SSIO} = $V_{SS\ IO}$, V_{DDA} = $V_{DD\ ANA}$, V_{SSA} = $V_{SS\ ANA}$
2. MODA, MODB and MODC can be used as GPIO after the bootstrap process has completed.
3. The following Host Interface signals are multiplexed: HRWB to $\overline{\text{HRD}}$, $\overline{\text{HDS}}$ to $\overline{\text{HWR}}$, $\overline{\text{HREQ}}$ to $\overline{\text{HTRQ}}$ and $\overline{\text{HACK}}$ to HRRQ.

Table 3-1. 56853 Signal and Package Information for the 128-pin LQFP (Continued)

Pin No.	Signal Name	Type	Description
106	$\overline{\text{HACK}}$	**Input**	**Host Acknowledge ($\overline{\text{HACK}}$)**—When the HI08 is programmed for HRMS=0 functionality (typically used on a single-data-strobe bus), this input has two functions: (1) provide a Host Acknowledge signal for DMA transfers or (2) to control handshaking and provide a Host Interrupt Acknowledge compatible with the MC68000 family processors. These pins are disconnected internally.
	HRRQ	Open Drain Output	**Receive Host Request (HRRQ)**—This signal is the Receive Host Request output when the HI08 is programmed for HRMS=1 functionality and is typically used on a double-data-strobe bus.
	GPIOB15	Input/Output	**Port B GPIO(15)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
101	TIO0	**Input**/Output	**Timer Input/Outputs (TIO0)**—This pin can be independently configured to be either a timer input source or an output flag.
	GPIOG0	Input/Output	**Port G GPIOG0**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
99	TIO1	**Input**/Output	**Timer Input/Outputs (TIO1)**—This pin can be independently configured to be either a timer input source or an output flag.
	GPIOG1	Input/Output	**Port G GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
98	TIO2	**Input**/Output	**Timer Input/Outputs (TIO2)**—This pin can be independently configured to be either a timer input source or an output flag.
	GPIOG2	Input/Output	**Port G GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
97	TIO3	**Input**/Output	**Timer Input/Outputs (TIO3)**—This pin can be independently configured to be either a timer input source or an output flag.
	GPIOG3	Input/Output	**Port G GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
20	$\overline{\text{IRQA}}$	Input	**External Interrupt Request A and B**—The $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ inputs are asynchronous external interrupt requests that indicate that an external device is requesting service. A Schmitt trigger input is used for noise immunity. They can be programmed to be level-sensitive or negative-edge- triggered. If level-sensitive triggering is selected, an external pull-up resistor is required for Wired-OR operation.
21	$\overline{\text{IRQB}}$		
15	MODA	**Input**	**Mode Select (MODA)**—During the bootstrap process MODA selects one of the eight bootstrap modes.
	GPIOH0	Input/Output	**Port H GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin after the bootstrap process has completed.

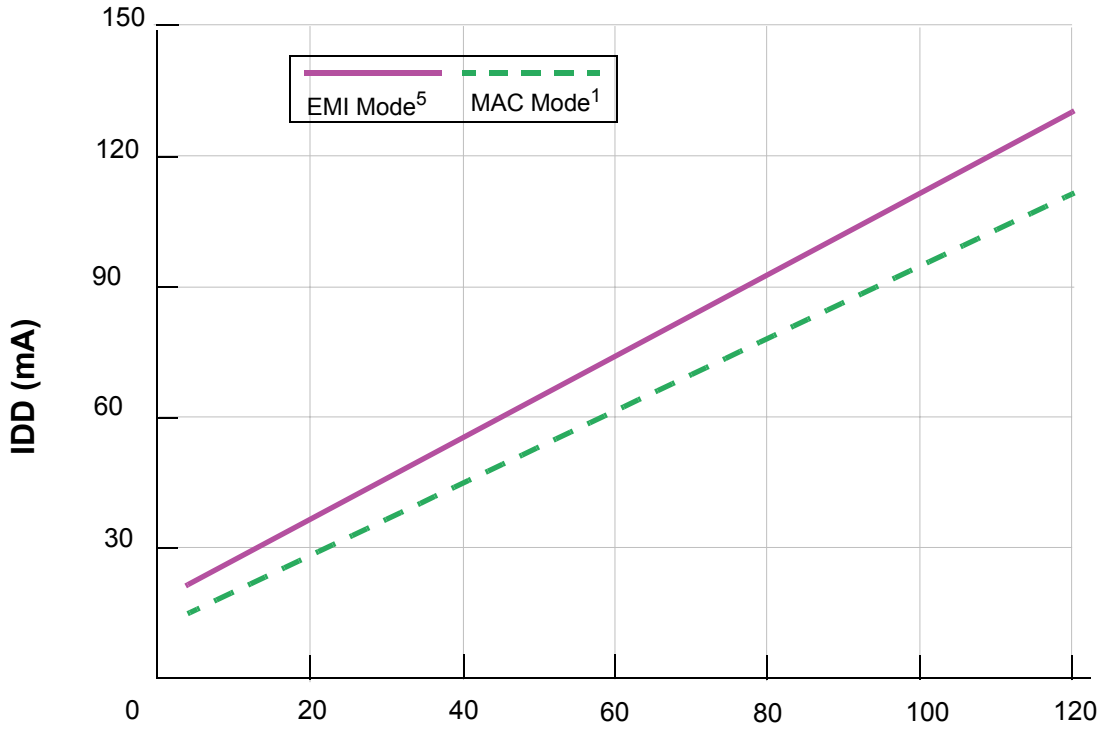


Figure 4-1 Maximum Run $I_{DDTOTAL}$ vs. Frequency (see Notes 1. and 5. in Table 4-4)

Table 4-6 PLL Timing

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
External reference crystal frequency for the PLL[1]	f_{osc}	2	4	4	MHz
PLL output frequency	f_{clk}	40	—	240	MHz
PLL stabilization time [2]	t_{plls}	—	1	10	ms

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 4MHz input crystal.
2. This is the minimum time required after the PLL setup is changed to ensure reliable operation.

4.6 External Memory Interface Timing

The External Memory Interface is designed to access static memory and peripheral devices. **Figure 4-10** shows sample timing and parameters that are detailed in **Table 4-7**.

The timing of each parameter consists of both a fixed delay portion and a clock related portion; as well as user controlled wait states. The equation:

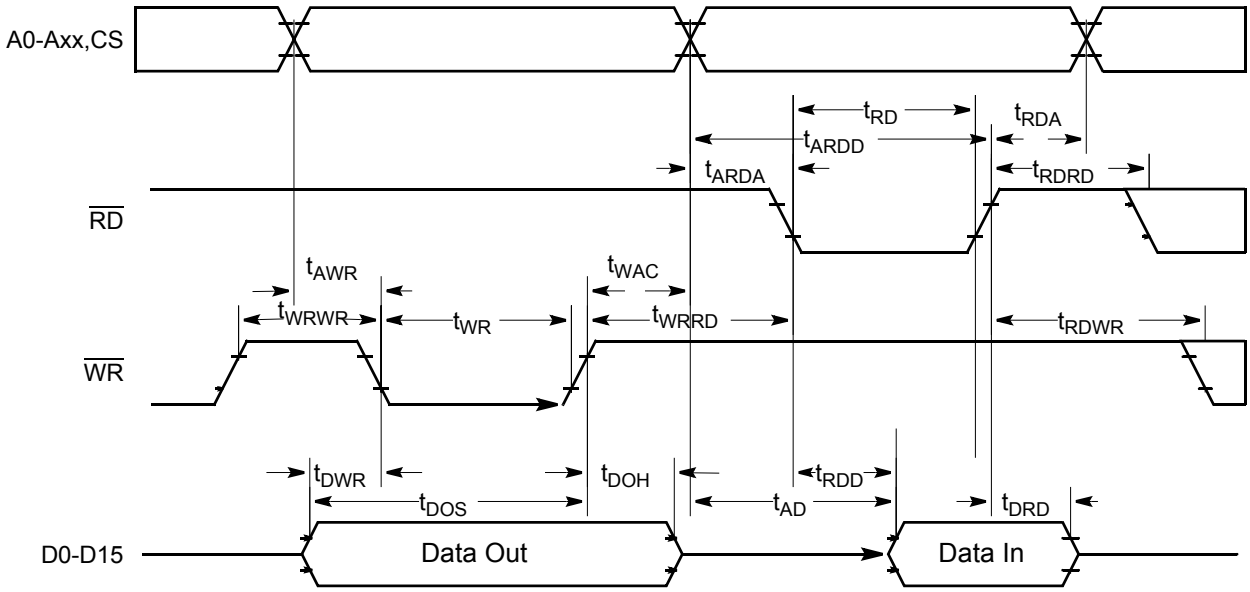
$$t = D + P * (M + W)$$

should be used to determine the actual time of each parameter. The terms in the above equation are defined as:

- t parameter delay time
- D fixed portion of the delay, due to on-chip path delays.
- P the period of the system clock, which determines the execution rate of the part (i.e. when the device is operating at 120 MHz, P = 8.33 ns).
- M Fixed portion of a clock period inherent in the design. This number is adjusted to account for possible clock duty cycle derating.
- W the sum of the applicable wait state controls. See the “Wait State Controls” column of **Table 4-7** for the applicable controls for each parameter. See the EMI chapter of the 83x Peripheral Manual for details of what each wait state field controls.

Some of the parameters contain two sets of numbers. These parameters have two different paths and clock edges that must be considered. Check both sets of numbers and use the smaller result. The appropriate entry may change if the operating frequency of the part changes.

The timing of write cycles is different when WWS = 0 than when WWS > 0. Therefore, some parameters contain two sets of numbers to account for this difference. The “Wait States Configuration” column of **Table 4-7** should be used to make the appropriate selection.



Note: During read-modify-write instructions and internal instructions, the address lines do not change state.

Figure 4-10 External Memory Interface Timing

Table 4-7 External Memory Interface Timing

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$ V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40\times$ to $+120\times$C, C_L £ 50pF, P = 8.333ns

Characteristic	Symbol	Wait States Configuration	D	M	Wait States Controls	Unit
Address Valid to $\overline{WR}$ Asserted	t_{AWR}	WWS=0	-0.79	0.50	WWSS	ns
		WWS>0	-1.98	0.69		
$\overline{WR}$ Width Asserted to $\overline{WR}$ Deasserted	t_{WR}	WWS=0	-0.86	0.19	WWS	ns
		WWS>0	-0.01	0.00		
Data Out Valid to $\overline{WR}$ Asserted	t_{DWR}	WWS=0	-1.52	0.00	WWSS	ns
		WWS=0	- 5.69	0.25		
		WWS>0	-2.10	0.19		
		WWS>0	-4.66	0.50		
Valid Data Out Hold Time after $\overline{WR}$ Deasserted	t_{DOH}		-1.47	0.25	WWSH	ns
Valid Data Out Set Up Time to $\overline{WR}$ Deasserted	t_{DOS}		-2.36	0.19	WWS,WWSS	ns
			-4.67	0.50		
Valid Address after $\overline{WR}$ Deasserted	t_{WAC}		-1.60	0.25	WWSH	

Table 4-7 External Memory Interface Timing (Continued)

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$ V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40\times$ to $+120\times$C, C_L £ 50pF, P = 8.333ns

Characteristic	Symbol	Wait States Configuration	D	M	Wait States Controls	Unit
$\overline{RD}$ Deasserted to Address Invalid	t_{RDA}		- 0.44	0.00	RWSH	ns
Address Valid to $\overline{RD}$ Deasserted	t_{ARDD}		-2.07	1.00	RWSS,RWS	ns
Valid Input Data Hold after $\overline{RD}$ Deasserted	t_{DRD}		0.00	N/A[1]	—	ns
$\overline{RD}$ Assertion Width	t_{RD}		-1.34	1.00	RWS	ns
Address Valid to Input Data Valid	t_{AD}		-10.27	1.00	RWSS,RWS	ns
			-13.5	1.19		
Address Valid to $\overline{RD}$ Asserted	t_{ARDA}		- 0.94	0.00	RWSS	ns
$\overline{RD}$ Asserted to Input Data Valid	t_{RDD}		-9.53	1.00	RWSS,RWS	ns
			-12.64	1.19		
$\overline{WR}$ Deasserted to $\overline{RD}$ Asserted	t_{WRRD}		-0.75	0.25	WWSH,RWSS	ns
$\overline{RD}$ Deasserted to $\overline{RD}$ Asserted	t_{RDRD}		-0.16[2]	0.00	RWSS,RWSH	ns
$\overline{WR}$ Deasserted to $\overline{WR}$ Asserted	t_{WRWR}	WWS=0	-0.44	0.75	WWSS, WWSH	ns
		WWS>0	-0.11	1.00		
$\overline{RD}$ Deasserted to $\overline{WR}$ Asserted	t_{RDWR}		0.14	0.50	MDAR, BMDAR, RWSH, WWSS	ns
			-0.57	0.69		

1. N/A since device captures data before it deasserts $\overline{RD}$
2. If RWSS = RWSH = 0, RD does not deassert during back-to-back reads and D=0.00 should be used.

4.7 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Table 4-8 Reset, Stop, Wait, Mode Select, and Interrupt Timing[1, 2]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
$\overline{RESET}$ Assertion to Address, Data and Control Signals High Impedance	t_{RAZ}	—	11	ns	4-11
Minimum $\overline{RESET}$ Assertion Duration[3]	t_{RA}	30	—	ns	4-11
$\overline{RESET}$ Deassertion to First External Address Output	t_{RDA}	—	120T	ns	4-11
Edge-sensitive Interrupt Request Width	t_{IRW}	1T + 3	—	ns	4-12

Figure 4-14 Interrupt from Wait State Timing

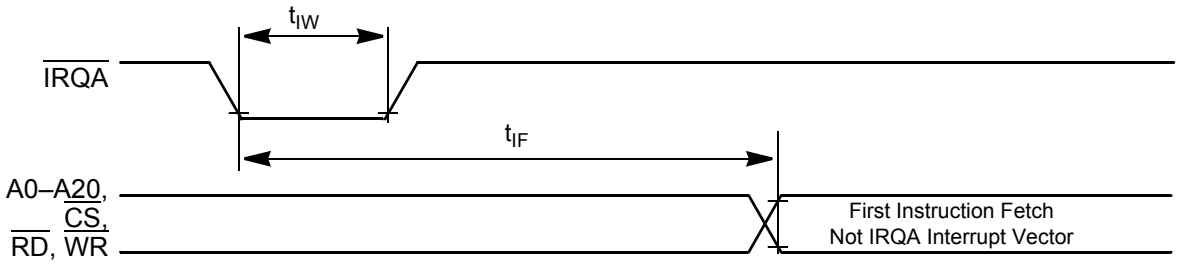


Figure 4-15 Recovery from Stop State Using Asynchronous Interrupt Timing

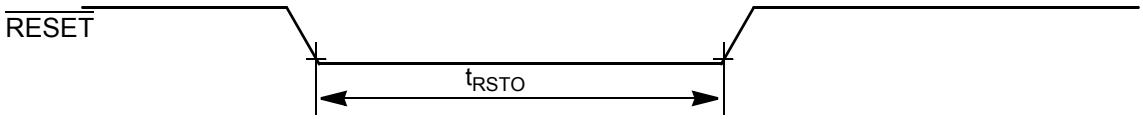


Figure 4-16 Reset Output Timing

4.8 Host Interface Port

Table 4-9 Host Interface Port Timing[1]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
Access time	TACKDV	—	13	ns	4-17
Disable time	TACKDZ	3	—	ns	4-17
Time to disassert	TACKREQH	3.5	9	ns	4-17, 4-20
Lead time	TREQACKL	0	—	ns	4-17 4-20

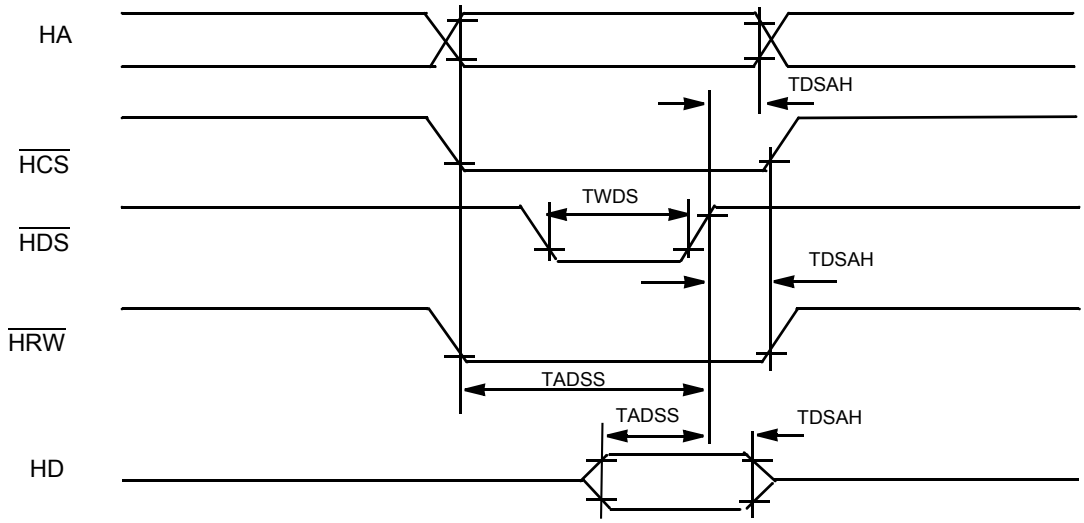


Figure 4-21 Single Strobe Write Mode

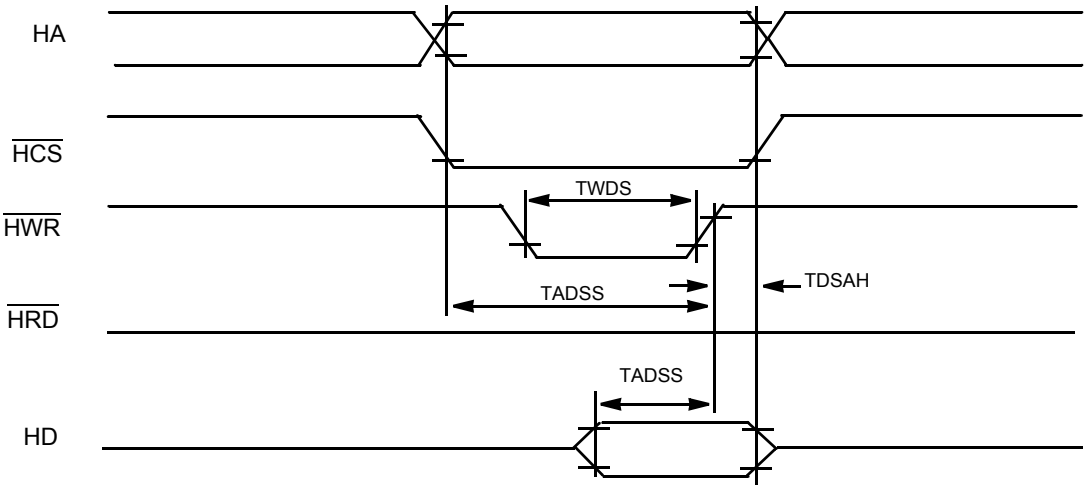


Figure 4-22 Dual Strobe Write Mode

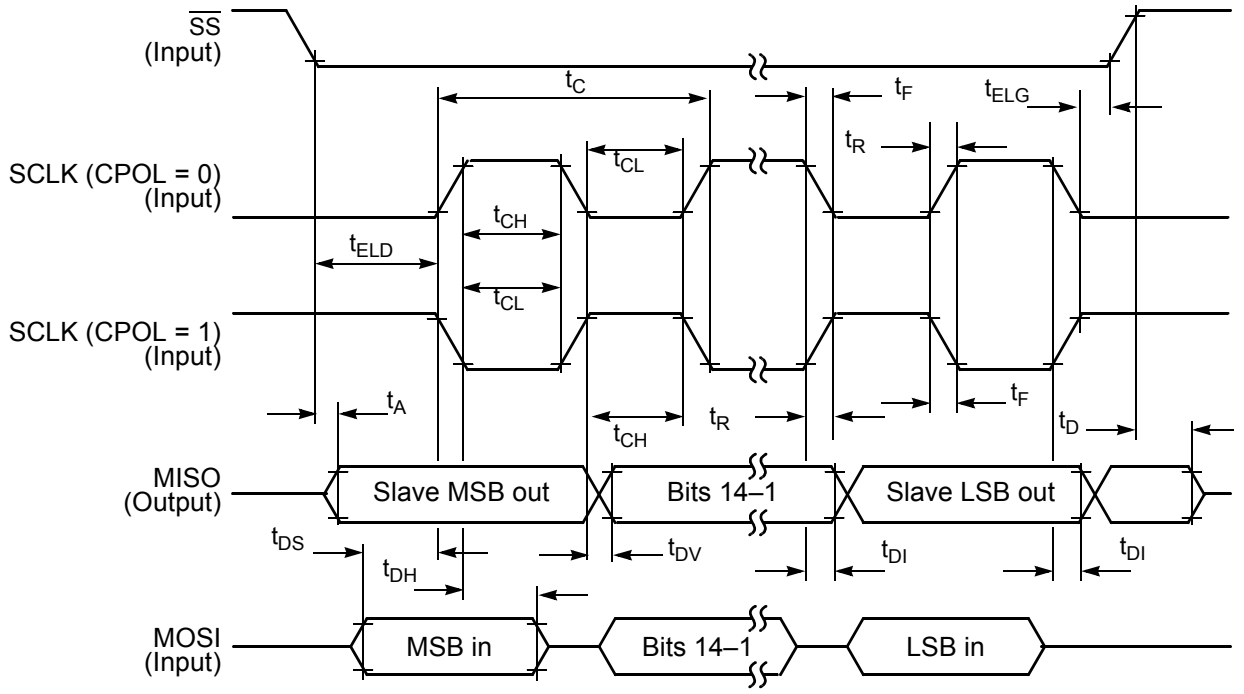


Figure 4-25 SPI Slave Timing (CPHA = 0)

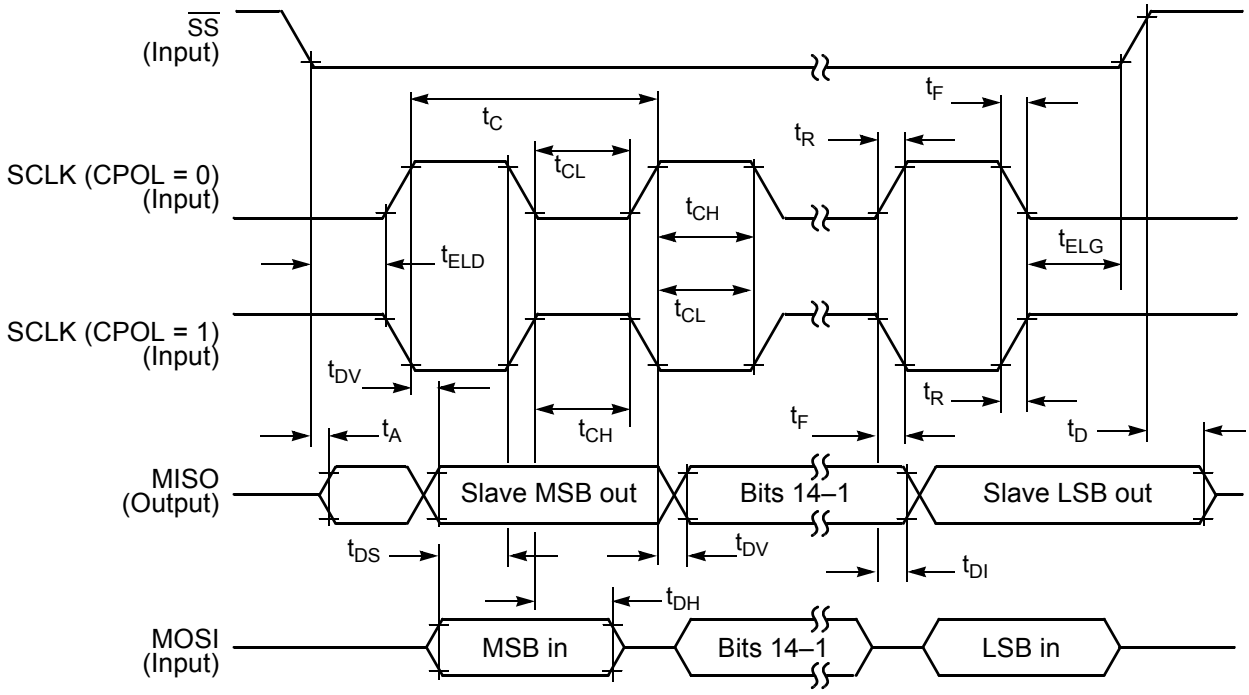


Figure 4-26 SPI Slave Timing (CPHA = 1)

4.10 Quad Timer Timing

Table 4-11 Quad Timer Timing[1, 2]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Max	Unit
Timer input period	P_{IN}	2T + 3	—	ns
Timer input high/low period	P_{INHL}	1T + 3	—	ns
Timer output period	P_{OUT}	2T - 3	—	ns
Timer output high/low period	P_{OUTHL}	1T - 3	—	ns

1. In the formulas listed, T = clock cycle. For $f_{op} = 120$MHz operation and fipb = 60MHz, T = 8.33ns.
2. Parameters listed are guaranteed by design.

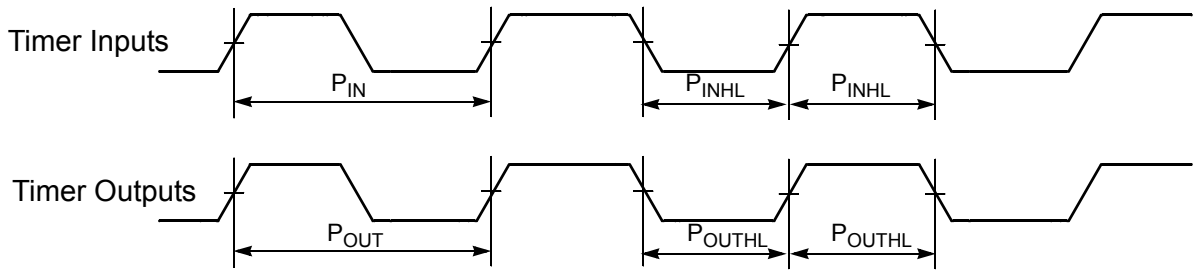


Figure 4-27 Timer Timing

4.11 Enhanced Synchronous Serial Interface (ESSI) Timing

Table 4-12 ESSI Master Mode[1] Switching Characteristics

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Parameter	Symbol	Min	Typ	Max	Units
SCK frequency	fs	—	—	15[2]	MHz
SCK period[3]	t_{SCKW}	66.7	—	—	ns
SCK high time	t_{SCKH}	33.4[4]	—	—	ns
SCK low time	t_{SCKL}	33.4[4]	—	—	ns
Output clock rise/fall time	—	—	4	—	ns
Delay from SCK high to SC2 (bl) high - Master[5]	t_{TFSBHM}	-1.0	—	1.0	ns

Table 4-12 ESSI Master Mode[1] Switching Characteristics (Continued)

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Parameter	Symbol	Min	Typ	Max	Units
Delay from SCK high to SC2 (wl) high - Master[5]	t_{TFSWHM}	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (bl) high - Master[5]	t_{RFSBHM}	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (wl) high - Master[5]	t_{RFSWHM}	-1.0	—	1.0	ns
Delay from SCK high to SC2 (bl) low - Master[5]	t_{TFSBLM}	-1.0	—	1.0	ns
Delay from SCK high to SC2 (wl) low - Master[5]	t_{TFSWLM}	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (bl) low - Master[5]	t_{RFSBLM}	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (wl) low - Master[5]	t_{RFSWLM}	-1.0	—	1.0	ns
SCK high to STD enable from high impedance - Master	t_{TXEM}	-0.1	—	2	ns
SCK high to STD valid - Master	t_{TXVM}	-0.1	—	2	ns
SCK high to STD not valid - Master	t_{TXNVM}	-0.1	—	—	ns
SCK high to STD high impedance - Master	t_{TXHIM}	-4	—	0	ns
SRD Setup time before SC0 low - Master	t_{SM}	4	—	—	ns
SRD Hold time after SC0 low - Master	t_{HM}	4	—	—	ns
Synchronous Operation (in addition to standard internal clock parameters)					
SRD Setup time before SCK low - Master	t_{TSM}	4	—	—	ns
SRD Hold time after SCK low - Master	t_{THM}	4	—	—	ns

1. Master mode is internally generated clocks and frame syncs
2. Max clock frequency is IP_clk/4 = 60MHz / 4 = 15MHz for an 120MHz part.
3. All the timings for the ESSI are given for a non-inverted serial clock polarity (TSCKP=0 in SCR2 and RSCKP=0 in SCSR) and a non-inverted frame sync (TFSI=0 in SCR2 and RFSI=0 in SCSR). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal SCK/SC0 and/or the frame sync SC2/SC1 in the tables and in the figures.
4. 50 percent duty cycle
5. bl = bit length; wl = word length

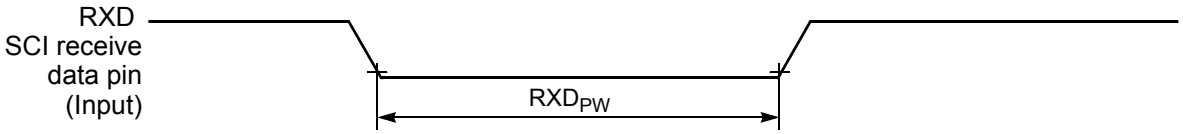


Figure 4-30 RXD Pulse Width

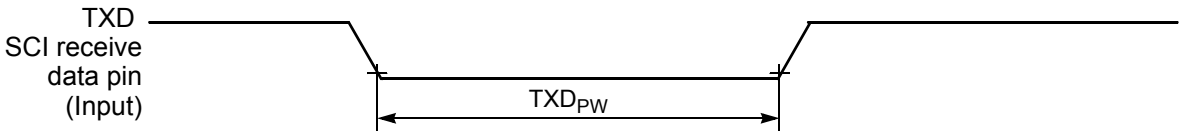


Figure 4-31 TXD Pulse Width

4.13 JTAG Timing

Table 4-15 JTAG Timing[1, 3]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Max	Unit
TCK frequency of operation[2]	f_{OP}	DC	30	MHz
TCK cycle time	t_{CY}	33.3	—	ns
TCK clock pulse width	t_{PW}	16.6	—	ns
TMS, TDI data setup time	t_{DS}	3	—	ns
TMS, TDI data hold time	t_{DH}	3	—	ns
TCK low to TDO data valid	t_{DV}	—	12	ns
TCK low to TDO tri-state	t_{TS}	—	10	ns
$\overline{\text{TRST}}$ assertion time	t_{TRST}	35	—	ns
$\overline{\text{DE}}$ assertion time	t_{DE}	4T	—	ns

1. Timing is both wait state and frequency dependent. For the values listed, T = clock cycle. For 120MHz operation, T = 8.33ns.
2. TCK frequency of operation must be less than 1/4 the processor rate.
3. Parameters listed are guaranteed by design.

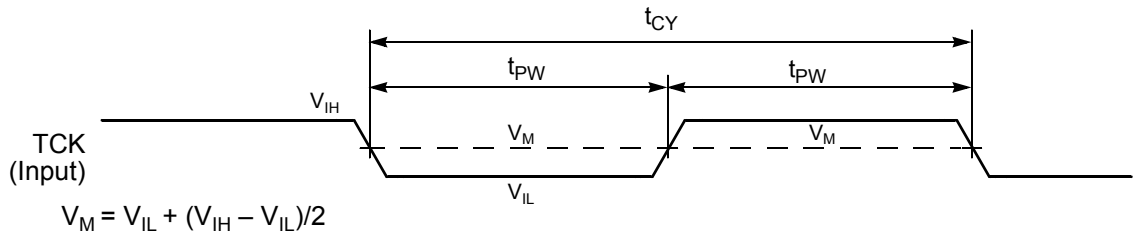


Figure 4-32 Test Clock Input Timing Diagram

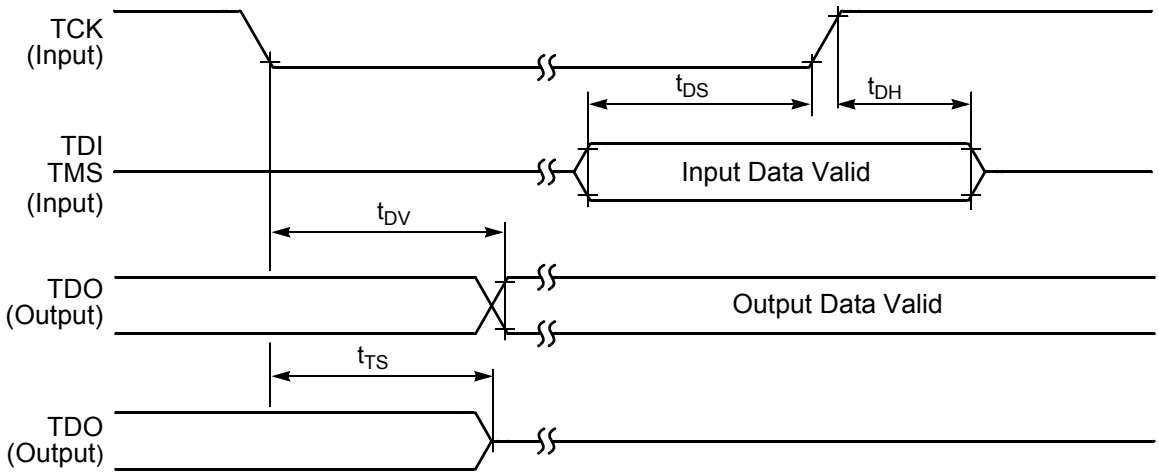


Figure 4-33 Test Access Port Timing Diagram

Figure 4-34 $\overline{\text{TRST}}$ Timing Diagram

Figure 4-35 Enhanced OnCE—Debug Event

Part 6 Design Considerations

6.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature °C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on the PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common definitions for determining the junction-to-case thermal resistance in plastic packages:

- Measure the thermal resistance from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink. This is done to minimize temperature variation across the surface.
- Measure the thermal resistance from the junction to where the leads are attached to the case. This definition is approximately equal to a junction to board thermal resistance.
- Use the value obtained by the equation $(T_J - T_T)/P_D$ where T_T is the temperature of the package case determined by a thermocouple.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case

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